# 54F/74F109

## Dual J$\overline{K}$ Positive Edge-Triggered Flip-Flop

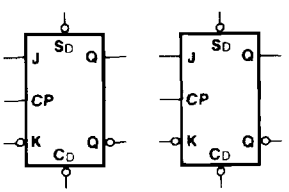
### Description

The 'F109 consists of two high-speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and $\overline{K}$ inputs.

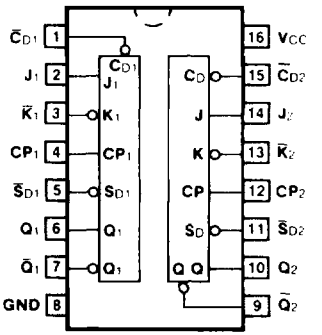
Asynchronous Inputs;
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

**Ordering Code:** See Section 5

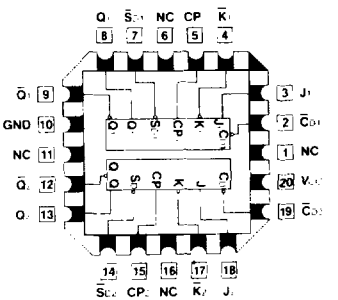
### Logic Symbol




### Connection Diagrams




**Pin Assignment for DIP and SOIC**




**Pin Assignment for LCC and PCC**

**Input Loading/Fan-Out:** See Section 3 for U.L. definitions

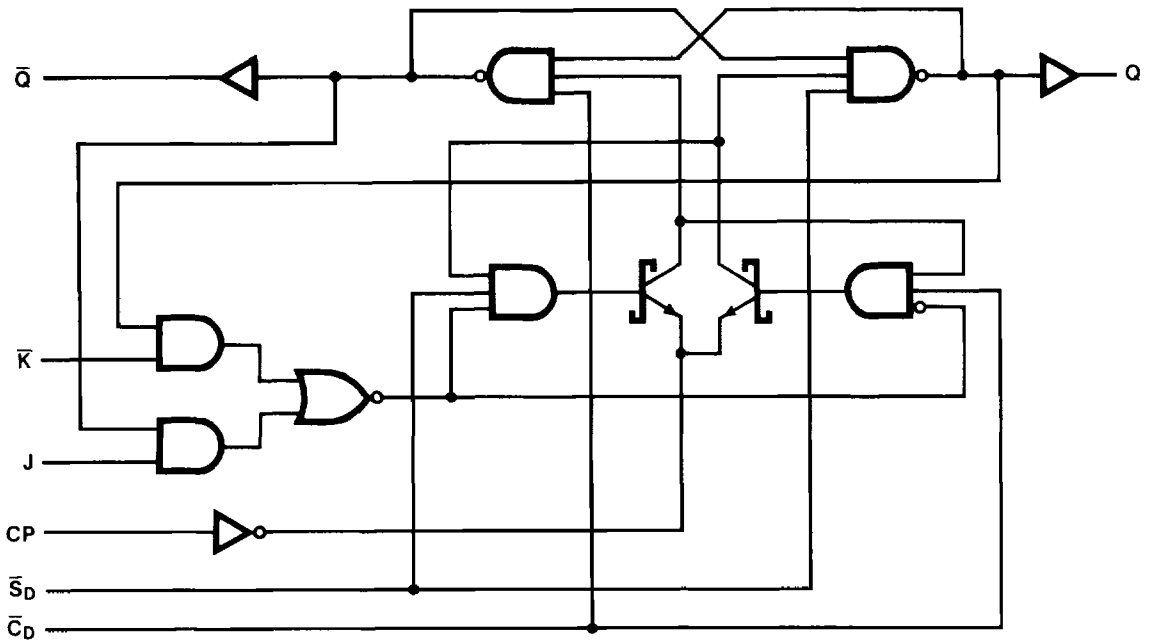
| Pin Names | Description | 54F/74F(U.L.) HIGH/LOW |
|---|---|---|
| $J_1$, $J_2$, $\overline{K}_1$, $\overline{K}_2$ | Data Inputs | 0.5/0.375 |
| $CP_1$, $CP_2$ | Clock Pulse Inputs (Active Rising Edge) | 0.5/0.375 |
| $\overline{C}_{D1}$, $\overline{C}_{D2}$ | Direct Clear Inputs (Active LOW) | 0.5/1.125 |
| $\overline{S}_{D1}$, $\overline{S}_{D2}$ | Direct Set Inputs (Active LOW) | 0.5/1.125 |
| $Q_1$, $Q_2$, $\overline{Q}_1$, $\overline{Q}_2$ | Outputs | 25/12.5 |

### Truth Table

| Inputs @ $t_n$ | | Outputs @ $t_{n+1}$ | |
|---|---|---|---|
| J | $\overline{K}$ | Q | $\overline{Q}$ |
| L | H | No Change | |
| L | L | L | H |
| H | H | H | L |
| H | L | Toggles | |

H = HIGH Voltage Level
L = LOW Voltage Level
$t_n$ = Bit Time before Clock Pulse
$t_{n+1}$ = Bit Time after Clock Pulse

**Logic Diagram** (one half shown)




Please note that this diagram is provided only for the understanding of logic operations and should not be used tc estimate propagation delays.

**DC Characteristics over Operating Temperature Range** (unless otherwise specified)

| Symbol | Parameter | 54F/74F | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $I_{CC}$ | Power Supply Current | | 11.7 | 17.0 | mA | $V_{CC}$ = Max, $V_{CP}$ = 0 V |

**AC Characteristics:** See Section 3 for waveforms and load configurations

| Symbol | Parameter | 54F/74F | | | 54F | | 74F | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$ | | | $T_A$, $V_{CC}$ = Mil $C_L = 50\ pF$ | | $T_A$, $V_{CC}$ = Com $C_L = 50\ pF$ | | | |
| | | Min | Typ | Max | Min | Max | Min | Max | | |
| $f_{max}$ | Maximum Clock Frequency | 100 | 125 | | 70 | | 90 | | MHz | 3-1 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$CP_n$ to $Q_n$ or $\overline{Q}_n$ | 3.8<br>4.4 | 5.3<br>6.2 | 7.0<br>8.0 | 3.8<br>4.4 | 9.0<br>10.5 | 3.8<br>4.4 | 8.0<br>9.2 | ns | 3-1<br>3-7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to<br>$Q_n$ or $\overline{Q}_n$ | 3.2<br>3.5 | 5.2<br>7.0 | 7.0<br>9.0 | 3.2<br>3.5 | 9.0<br>11.5 | 3.2<br>3.5 | 8.0<br>10.5 | ns | 3-1<br>3-9 |

**AC Operating Requirements:** See Section 3 for waveforms

| Symbol | Parameter | 54F/74F | | | 54F | | 74F | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $T_A = +25°C$ $V_{CC} = +5.0\ V$ | | | $T_A$, $V_{CC}$ = Mil | | $T_A$, $V_{CC}$ = Com | | | |
| | | Min | Typ | Max | Min | Max | Min | Max | | |
| $t_s(H)$<br>$t_s(L)$ | Setup Time, HIGH or LOW<br>$J_n$ or $\overline{K}_n$ to $CP_n$ | 3.0<br>3.0 | | | 3.0<br>3.0 | | 3.0<br>3.0 | | ns | 3-5 |
| $t_h(H)$<br>$t_h(L)$ | Hold Time, HIGH or LOW<br>$J_n$ or $\overline{K}_n$ to $CP_n$ | 1.0<br>1.0 | | | 1.0<br>1.0 | | 1.0<br>1.0 | | | |
| $t_w(H)$<br>$t_w(L)$ | $CP_n$ Pulse Width<br>HIGH or LOW | 4.0<br>5.0 | | | 4.0<br>5.0 | | 4.0<br>5.0 | | ns | 3-7 |
| $t_w(L)$ | $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width, LOW | 4.0 | | | 4.0 | | 4.0 | | ns | 3-9 |
| $t_{rec}$ | Recovery Time<br>$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP | 2.0 | | | 2.0 | | 2.0 | | ns | 3-11 |