CMOS Low Voltage SRAM

Fast Synchronous with Burst Counter

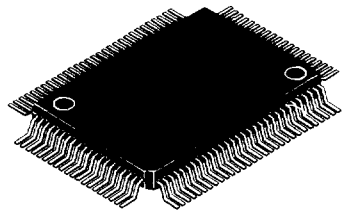
2M-BIT(64K X 32)

Advanced Information

N343632L

-K, -M, -N

■ Features



100pin TQFP

- CMOS SRAM organized as 65,536 X 32bits
- Single+3.3V Power Supply
- Fast Clock Access time : 5.5ns/100MHz, 6ns/90MHz, 7ns/75MHz, 8ns/66MHz, 10ns/60MHz, 12ns/50MHz
- Synchronous operation
- Burst Read/Write : Pentium™ Burst and Linear Burst Sequence
- Fully Registered Inputs and Outputs for Pipelined Operation
- All Registers triggered off Positive Clock Edge
- Asynchronous Output Enable : $\overline{OE}$
- Burst Mode Selectable : MODE
- Separate Byte Write Enable : $\overline{BW1}$ - $\overline{BW4}$, $\overline{BWE}$ and Global Write Enable : $\overline{GW}$
- Three Chip Enables for Easy Depth Expansion
- 2 Clock Enable and 1 Clock Disable to eliminate multiple bank bus contention
- Common I/O Using Three State Outputs
- 5V Tolerant Clock Pin (-K, -N Versions)
- Flow-Through Mode (-M, -N Versions)
- Sleep Mode (-M, -N Versions)
- Packages
  100 pin QFP
  100 pin TQFP(1.6mm Max.)

■ Description

The N343632L is a 65,536 X 32bits synchronous static RAM fabricated with advanced CMOS technology using double layer metal, triple-layer polysilicon technology.

This technology and unique peripheral circuits make the N343632L a high-speed device. The N343632L is suitable for applications which require high-speed device, low voltage, high-density memory and wide bit configuration, such as cache and buffer memory.

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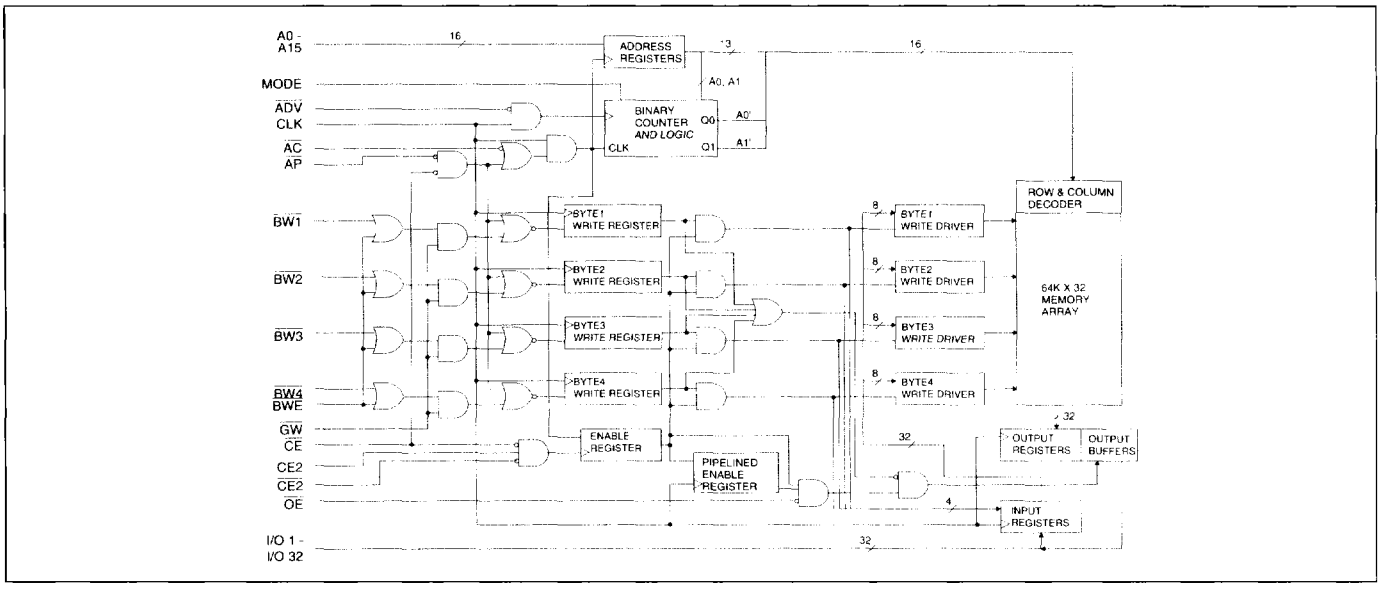
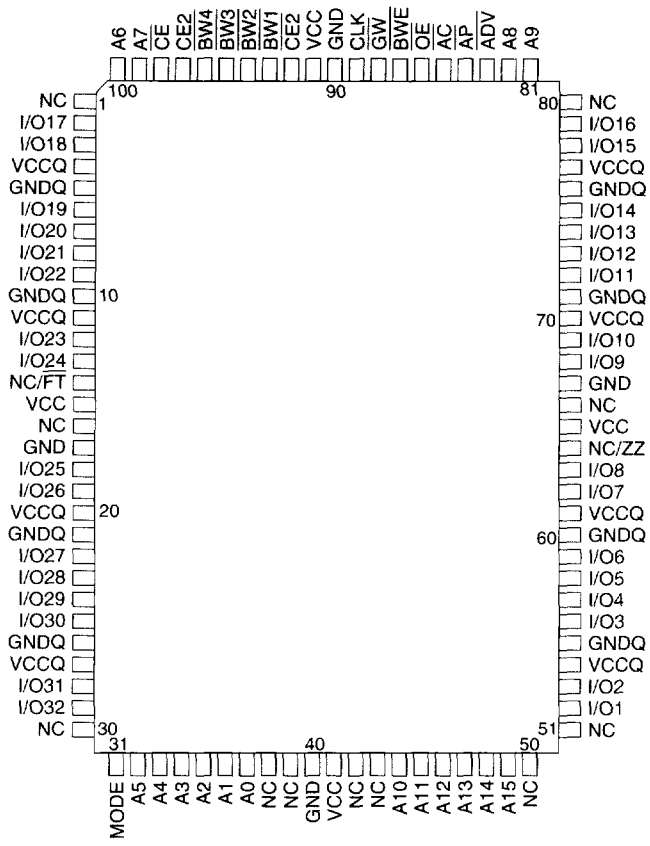
■ Functional Block Diagram



■ Pin Configuration

100 pin QFP/TQFP



■ Pin Description

SYMBOL	PIN NAME
A0-A15	Address input
I/O1 - I/O32	Data input/output
$\overline{ADV}$	Burst Address Advance
$\overline{AC}$	Controller Address Status
$\overline{AP}$	Processor Address Status
$\overline{CE}$	Chip Enable input
$\overline{CE2}$	Chip Enable input
CE2	Chip Enable input
$\overline{BW1}$ - $\overline{BW4}$,$\overline{BWE}$	Byte Write Enable, $\overline{BW1}$ controls I/O1-8, $\overline{BW2}$ controls I/O9-16, $\overline{BW3}$ controls I/O17-24, $\overline{BW4}$ controls I/O25-32
$\overline{GW}$	Global Write Enable
$\overline{OE}$	Output Enable input
CLK	System Clock input
MODE	Mode Select
$\overline{FT}$	Flow-Through Pin (-M, -N Versions)
ZZ	Sleep Mode Pin (-M, -N Versions)
VCC	Power Supply Pin(+3.3V)
GND	Ground Pin
VCCQ	Power Supply Pin for Outputs (+3.3V)
GNDQ	Ground Pin for Outputs
NC	No Connection

■ Pentium™ Burst Sequence Table (MODE = NC or VCC)

External Address	A15 - A2, A1, A0
1st Burst Address	A15 - A2, A1, $\overline{A0}$
2nd Burst Address	A15 - A2, $\overline{A1}$, A0
3rd Burst Address	A15 - A2, $\overline{A1}$, $\overline{A0}$

■ Linear Burst Sequence Table (MODE = GND)

External Address	A15 - A2, 0, 0	A15 - A2, 0, 1	A15 - A2, 1, 0	A15 - A2, 1, 1
1st Burst Address	A15 - A2, 0, 1	A15 - A2, 1, 0	A15 - A2, 1, 1	A15 - A2, 0, 0
2nd Burst Address	A15 - A2, 1, 0	A15 - A2, 1, 1	A15 - A2, 0, 0	A15 - A2, 0, 1
3rd Burst Address	A15 - A2, 1, 1	A15 - A2, 0, 0	A15 - A2, 0, 1	A15 - A2, 1, 0

NOTE : The burst sequence wraps around to its initial state upon completion.

MODE and $\overline{FT}$ are DC operated pins. Do not alter input state while device is operating.

■ Asynchronous Truth Table

(Standard, -K Versions)

Operation	$\overline{OE}$	I/O
Read Cycle	L	Dout
Read Cycle	H	Hi-Z
Write Cycle	X	Hi-Z - Din
Deselected	X	Hi-Z

(-M, -N Versions)

Operation	ZZ	$\overline{OE}$	$\overline{FT}$	I/O
Non-Pipelined Read Cycle	L	L	L	Dout
Non-Pipelined Read Cycle	L	H	L	Hi-Z
Pipelined Read Cycle	L	L	H	Dout
Pipelined Read Cycle	L	H	H	Hi-Z
Write Cycle	L	X	X	Hi-Z - Din
Deselected	L	X	X	Hi-Z
Sleep	H	X	X	Hi-Z

NOTE : (1) X means "don't care"

(2) For a write operation following a read operation, $\overline{OE}$ must be high before the input data required setup time and held through the input data hold time.

(3) Normally, $\overline{FT}$ is pulled to High or NC. $\overline{FT}$ = Low input is only used for a test mode.

■ Synchronous Truth Table

Operation	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{AP}$	$\overline{AC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address	I/O
Deselected	H	X	X	X	L	X	X	↑	N/A	Hi-Z
Deselected	L	X	L	L	X	X	X	↑	N/A	Hi-Z
Deselected	L	H	X	L	X	X	X	↑	N/A	Hi-Z
Deselected	L	X	L	H	L	X	X	↑	N/A	Hi-Z
Deselected	L	H	X	H	L	X	X	↑	N/A	Hi-Z
Read Cycle / Begin Burst	L	L	H	L	X	X	X	↑	External	Hi-Z
Read Cycle / Begin Burst	L	L	H	H	L	X	H	↑	External	Hi-Z
Read Cycle / Continue Burst	X	X	X	H	H	L	H	↑	Next	Data/Hi-Z
Read Cycle / Continue Burst	H	X	X	X	H	L	H	↑	Next	Data/Hi-Z
Read Cycle / Suspend Burst	X	X	X	H	H	H	H	↑	Current	Data/Hi-Z
Read Cycle / Suspend Burst	H	X	X	X	H	H	H	↑	Current	Data/Hi-Z
Write Cycle / Begin Burst	L	L	H	H	L	X	L	↑	External	Hi-Z
Write Cycle / Continue Burst	X	X	X	H	H	L	L	↑	Next	Hi-Z
Write Cycle / Continue Burst	H	X	X	X	H	L	L	↑	Next	Hi-Z
Write Cycle / Suspend Burst	X	X	X	H	H	H	L	↑	Current	Hi-Z
Write Cycle / Suspend Burst	H	X	X	X	H	H	L	↑	Current	Hi-Z

NOTE : (1) X means "don't care", $\overline{WRITE}$ = L means any one or more byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) and $\overline{BWE}$ are Low or $\overline{GW}$ is Low. $\overline{WRITE}$ = H means all byte write enables and $\overline{GW}$ are High.

(2) $\overline{ADV}$ must be High at the rising edge of the first clock after a $\overline{AP}$ cycle is initiated if a WRITE cycle is desired.(to ensure use of correct address)

(3) Data/Hi-Z means that the condition of the I/O's are controlled by $\overline{OE}$. I/O outputs data when $\overline{OE}$ = L , otherwise I/O = Hi-Z.

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■ Partial Truth Table for Write Enable

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read Cycle	H	H	X	X	X	X
Read Cycle	H	L	H	H	H	H
Write Cycle / Byte1 only	H	L	L	H	H	H
Write Cycle / All Bytes	H	L	L	L	L	L
Write Cycle / All Bytes	L	X	X	X	X	X

NOTE : (1) X means "don't care".

(2) Using $\overline{BWE}$ and $\overline{BW1}$ through $\overline{BW4}$, any one or more bytes may be written.

■ Absolute Maximum Ratings

Symbol	Rating		Min.	Max.	Unit	Note
VCC	Supply Voltage		GND - 0.5	4.6	V	
VTERM	Terminal Voltage with Respect to GND	CLK	GND - 0.5	VCC + 0.5 (Max. 4.6)	V	1
			GND - 0.5	VCC + 2.4 (Max. 6.0)	V	2
		All Other Pins	GND - 0.5	VCC + 0.5 (Max. 4.6)	V	
TA	Operating Temperature		0	70	°C	
TBIAS	Temperature Under Bias		-55	125	°C	
TSTG	Storage Temperature		-55	125	°C	

NOTICE
Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NOTE : (1) Standard, -M, Versions.

(2) -K, N Versions.

■ Recommended DC Operating Conditions

Recommended DC Operating Conditions (TA = 0 to 70°C)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Note
Vcc, Vccq	Supply Voltage		3.1	3.3	3.6	V	
GND	Supply Voltage		0	0	0	V	
VIH	Input High Voltage	I/O1 -I/O32,	2.0		Vccq + 0.3	V	
		CLK	2.0		Vcc + 0.3	V	1
			2.0		Vcc + 2.4 (Max. 5.5)	V	2
		All Other Pins	2.0		Vcc + 0.3	V	
VIL	Input Low Voltage		-0.3		0.8	V	3

NOTE : (1) Standard, -M, Versions.

(2) -K, N Versions.

(3) VIL(min.) = -2.0V for pulse width less than 10ns.

■ Capacitance

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VI/O = 0V	8	pF

■ DC Electrical Characteristics

(TA = 0 to 70°C, VCC = 3.3V + 0.3V/ - 0.2V)

Symbol	Parameter	100MHz	90MHz	75MHz	66MHz	60MHz	50MHz	Unit	Note
ICC	Operating Supply Current Device selected, VIN ≤ VIL or ≥ VIH, I(I/O) = 0	340	320	300	280	260	240	mA	
ISB	Standby Supply Current Device deselected, VIN ≤ VIL or ≥ VIH (0MHz)	20	20	20	20	20	20	mA	1
ISB1	Standby Supply Current Device deselected, VIN ≤ 0.2V or ≥ Vcc - 0.2V, VIN(I/O) ≥ Vccq -0.2V or ≤ 0.2V (0MHz)	2	2	2	2	2	2	mA	1
ISB2	Standby Supply Current Device deselected, VIN ≤ VIL or ≥ VIH	60	55	50	45	40	35	mA	1
ISB3	Sleep Mode Supply Current ZZ ≥ Vcc - 0.2V	2	2	2	2	2	2	mA	2

NOTE : (1) All Inputs Static

(2) -M, -N Versions only.

DC Electrical Characteristics(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
ILI	Input Leakage Current(1)	VIN = 0 to Vcc	-2	2	µA
ILO	I/O Leakage Current	VI/O = 0 to Vcc, Output Disabled	-2	2	µA
VOL	Output Low Voltage	IOL = 8mA	-	0.4	V
VOH	Output High Voltage	IOH = -5mA	2.4	-	V

NOTE : (1) MODE, $\overline{FT}$ and ZZ pin have an internal pull-up and exhibit an input leakage current of ± 400µA

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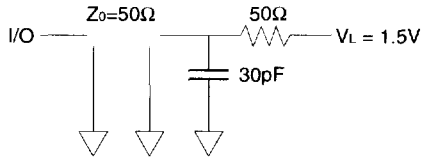
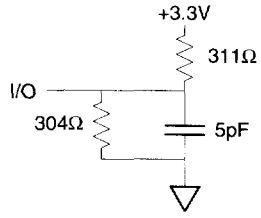
■ AC Test Conditions

Input pulse levels	GND to 3V
Input pulse rise and fall times	1.5ns
Input timing reference levels	1.5V
Output timing reference levels	1.5V
Output load	See figure 1 and 2



(Including scope and jig)

Figure 1. Output Load Equivalent



(Including scope and jig)

Figure 2. Output Load Equivalent
(for TDC1, TDC2, TOLZ, TOHZ, TCZ)

■ AC Electrical Characteristics

(TA = 0 to 70°C, VCC = 3.3V + 0.3V/ - 0.2V)

Read and Write Cycle

Parameter	Symbol		100MHz		90MHz		75MHz		66MHz		60MHz		50MHz		Unit
	Standard	Alternative	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Cycle Time	t_{KHKH}	t_{CYC}	10.0		11.1		13.3		15.0		16.7		20.0		ns
Clock Access Time (0pF load)	t_{KHQV0}	t_{CD0}		5.0		5.5		6.0		7.0		9.0		11.0	ns
Clock Access Time (Std load)	t_{KHQV}	t_{CD}		5.5		6.0		7.0		8.0		10.0		12.0	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		5.0		5.0		5.0		5.0		6.0		6.0	ns
Clock High to Output Active	t_{KHQX1}	t_{DC1}	2.0		2.0		2.0		2.0		2.0		2.0		ns
Clock High to Output Change	t_{KHQX2}	t_{DC2}	2.0		2.0		2.0		2.0		2.0		2.0		ns
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0.0		0.0		0.0		0.0		0.0		0.0		ns
Output Disable to Output Hi-Z	t_{GHQZ}	t_{OHZ}		5.0		5.0		5.0		5.0		5.0		5.0	ns
Clock High to Output Hi-Z	t_{KHQZ}	t_{CZ}	2.0	10.0	2.0	11.1	2.0	13.3	2.0	15.0	2.0	16.7	2.0	20.0	ns
Clock High Pulse Width	t_{KHKL}	t_{CH}	3.5		4.0		5.0		5.0		6.0		6.0		ns
Clock Low Pulse Width	t_{KLKH}	t_{CL}	3.5		4.0		5.0		5.0		6.0		6.0		ns
Setup Times : Address	t_{AVKH}	t_{AS}	2.5		2.5		2.5		2.5		2.5		2.5		ns
Address Status	t_{ADSVKH}	t_{SS}	2.5		2.5		2.5		2.5		2.5		2.5		ns
Data In	t_{DVKH}	t_{DS}	2.5		2.5		2.5		2.5		2.5		2.5		ns
Write Enable	t_{WVKH}	t_{WS}	2.5		2.5		2.5		2.5		2.5		2.5		ns
Address Advance	t_{ADVVKH}		2.5		2.5		2.5		2.5		2.5		2.5		ns
Chip Enable	t_{EVKH}		2.5		2.5		2.5		2.5		2.5		2.5		ns
Hold Times : Address	t_{KHAX}	t_{AH}	0.5		0.5		0.5		0.5		0.5		0.5		ns
Address Status	t_{KHADSX}	t_{SH}	0.5		0.5		0.5		0.5		0.5		0.5		ns
Data In	t_{KHDX}	t_{DH}	0.5		0.5		0.5		0.5		0.5		0.5		ns
Write Enable	t_{KHWX}	t_{WH}	0.5		0.5		0.5		0.5		0.5		0.5		ns
Address Advance	t_{KHADVX}		0.5		0.5		0.5		0.5		0.5		0.5		ns
Chip Enable	t_{KHEX}		0.5		0.5		0.5		0.5		0.5		0.5		ns
ZZ Standby Time	t_{ZZS}			100.0		100.0		100.0		100.0		100.0		100.0	ns
ZZ Recovery Time	t_{ZZREC}		100.0		100.0		100.0		100.0		100.0		100.0		ns

NOTE : tZZS and tZZREC is for -M, -N Versions only.

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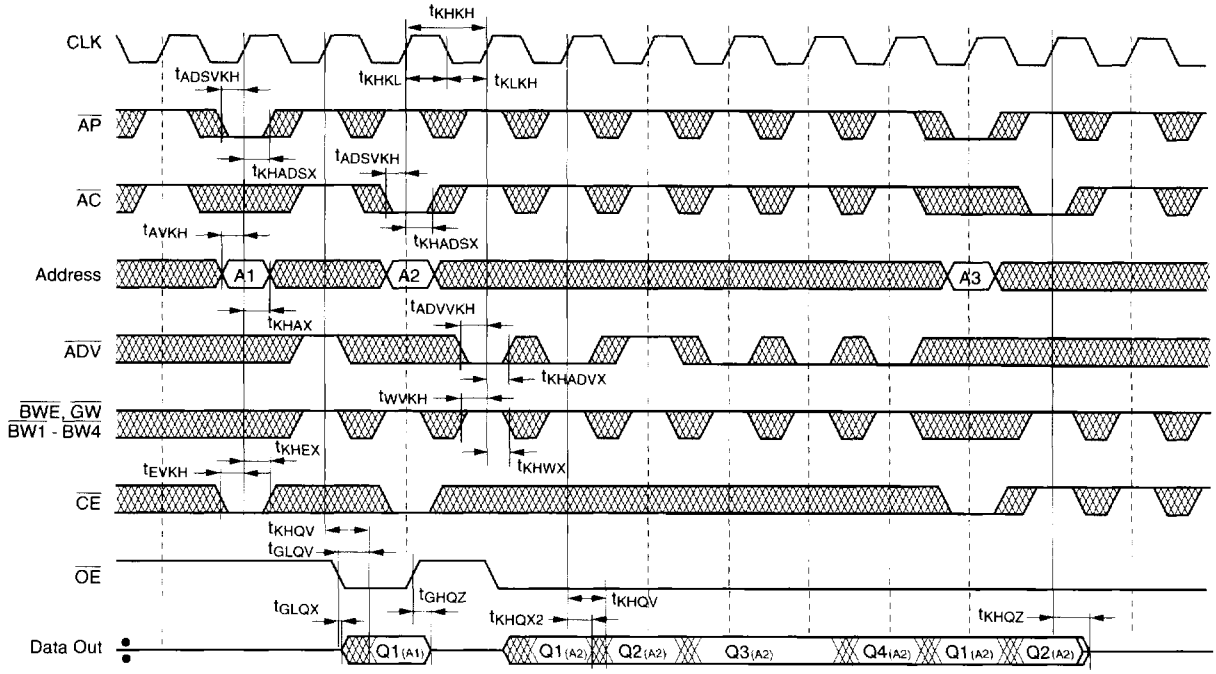
■ AC Timing Waveforms

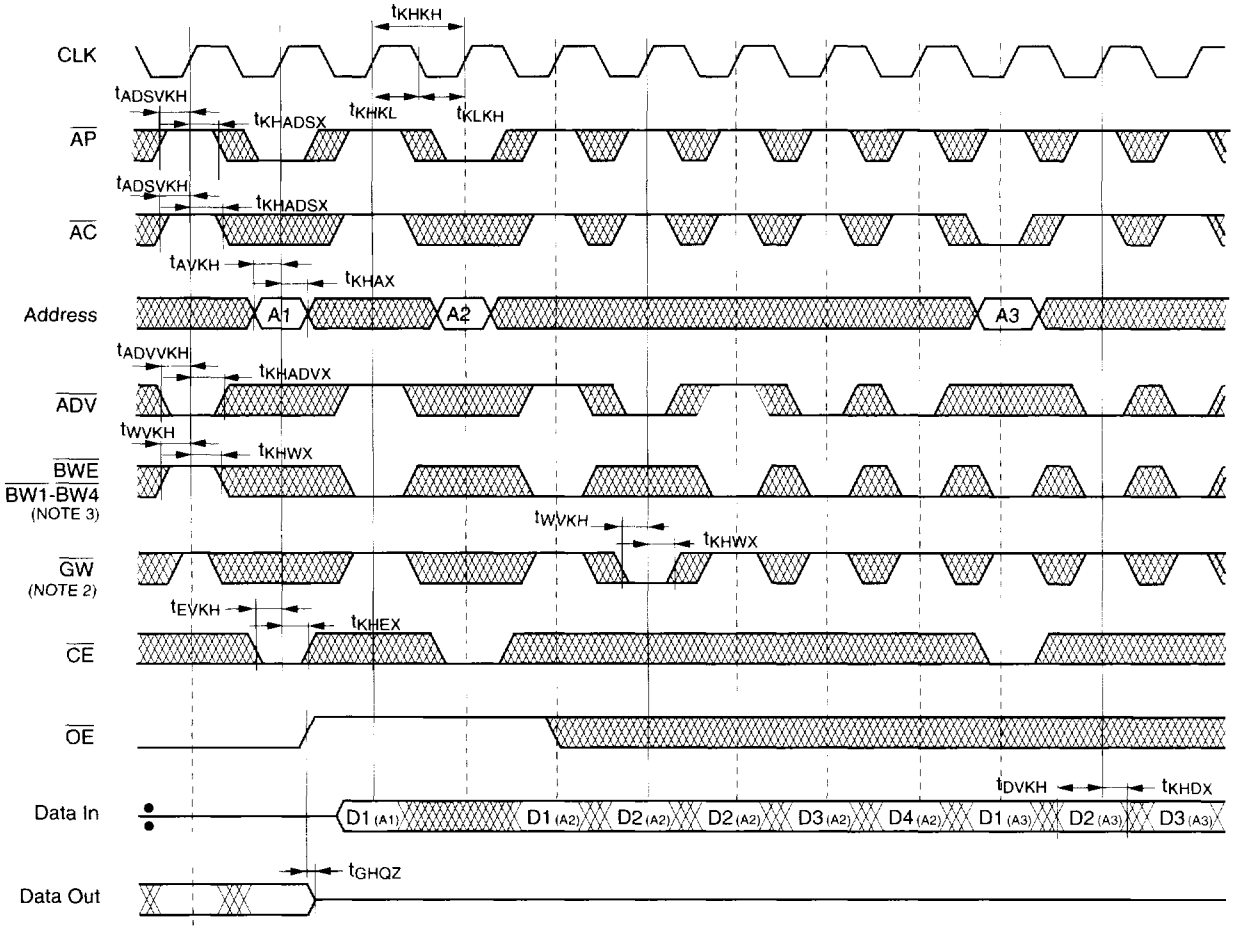
Read Cycle



NOT : (1) Qn(A2) refers to output from address A2. Q1 - Q4 refers to outputs according to burst sequence.

(2) $\overline{CE2}$ and CE2 have the same timing as $\overline{CE}$. In this timing, when $\overline{CE}$ is Low, $\overline{CE2}$ is Low and CE2 is High. When $\overline{CE}$ is High, $\overline{CE2}$ is High and CE2 is Low.

Write Cycle



NOTE : (1) $\overline{CE2}$ and CE2 have the same timing as $\overline{CE}$. In this timing, when $\overline{CE}$ is Low, $\overline{CE2}$ is Low and CE2 is High. When $\overline{CE}$ is High, $\overline{CE2}$ is High and CE2 is Low.

(2) All bytes WRITE can be initiated by $\overline{GW}$ Low or $\overline{GW}$ High and $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$ Low.

(3) $\overline{BWE}$ is low when any one or more Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BWE3}$, and $\overline{BW4}$) are low in this diagram.

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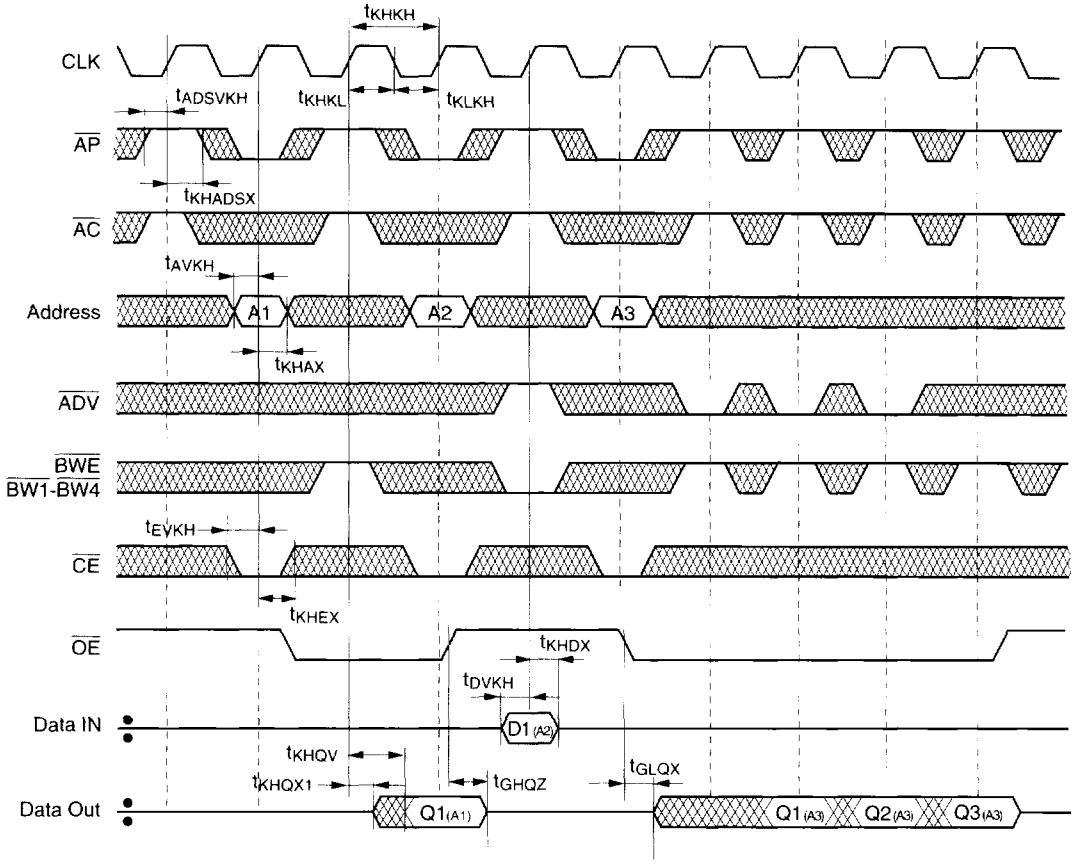
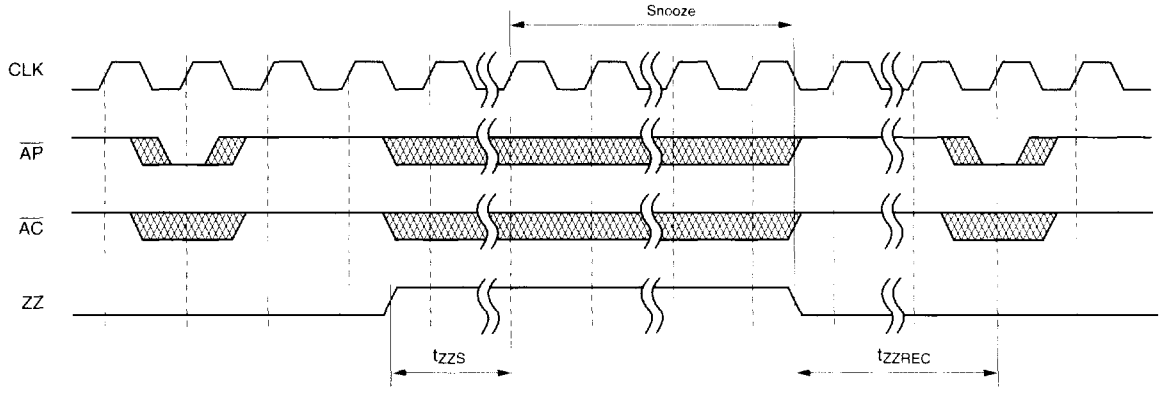
Read/Write Cycle



NOTE : (1) $\overline{CE2}$ and CE2 have the same timing as $\overline{CE}$. In this timing, when $\overline{CE}$ is Low, $\overline{CE2}$ is Low and CE2 is High. When $\overline{CE}$ is High, $\overline{CE2}$ is High and CE2 is Low.

(2) $\overline{GW}$ is High in this diagram.

Sleep Mode Cycle[4]



NOTE : (1) Data retention is guaranteed when ZZ is asserted and clock remains active.

(2) $\overline{AC}$ and $\overline{AP}$ must not be asserted for a least 100ns after leaving ZZ state.

(3) Do not assert ZZ during a write operation.

(4) -M, -N Versions only.

■ Ordering Information

N3 43632L Δ Δ - X X □

Device Type | Package | Speed | Function

Function	
Blank	Standard Type
K	5V tolerant Clock pin
M	Sleep mode/Flow Through
N	5V tolerant Clock pin/Sleep mode/Flow Through
Speed	
55 (5.5)	ns
6	
7	
8	
10	
12	
Package	
QF	QFP
TQ	TQFP
Device Type	
43632L	2Mbit Fast Synchronous SRAM with Burst Counter, Low Voltage 64K X 32

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PART NO.	Access Time (ns)	Clock Frequency (MHz)	Operating Current (mA)	Package
N343632LQF-55	5.5	100	340	100Pin QFP
N343632LTQ-55	5.5	100	340	100Pin TQFP
N343632LQF-6	6	90	320	100Pin QFP
N343632LTQ-6	6	90	320	100Pin TQFP
N343632LQF-7	7	75	300	100Pin QFP
N343632LTQ-7	7	75	300	100Pin TQFP
N343632LQF-8	8	66	280	100Pin QFP
N343632LTQ-8	8	66	280	100Pin TQFP
N343632LQF-10	10	60	260	100Pin QFP
N343632LTQ-10	10	60	260	100Pin TQFP
N343632LQF-12	12	50	240	100Pin QFP
N343632LTQ-12	12	50	240	100Pin TQFP

PART NO.	Access Time (ns)	Clock Frequency (MHz)	Operating Current (mA)	Package
N343632LQF-55K	5.5	100	340	100Pin QFP
N343632LTQ-55K	5.5	100	340	100Pin TQFP
N343632LQF-6K	6	90	320	100Pin QFP
N343632LTQ-6K	6	90	320	100Pin TQFP
N343632LQF-7K	7	75	300	100Pin QFP
N343632LTQ-7K	7	75	300	100Pin TQFP
N343632LQF-8K	8	66	280	100Pin QFP
N343632LTQ-8K	8	66	280	100Pin TQFP
N343632LQF-10K	10	60	260	100Pin QFP
N343632LTQ-10K	10	60	260	100Pin TQFP
N343632LQF-12K	12	50	240	100Pin QFP
N343632LTQ-12K	12	50	240	100Pin TQFP
N343632LQF-55M	5.5	100	340	100Pin QFP
N343632LTQ-55M	5.5	100	340	100Pin TQFP
N343632LQF-6M	6	90	320	100Pin QFP
N343632LTQ-6M	6	90	320	100Pin TQFP
N343632LQF-7M	7	75	300	100Pin QFP
N343632LTQ-7M	7	75	300	100Pin TQFP
N343632LQF-8M	8	66	280	100Pin QFP
N343632LTQ-8M	8	66	280	100Pin TQFP
N343632LQF-10M	10	60	260	100Pin QFP
N343632LTQ-10M	10	60	260	100Pin TQFP
N343632LQF-12M	12	50	240	100Pin QFP
N343632LTQ-12M	12	50	240	100Pin TQFP
N343632LQF-55N	5.5	100	340	100Pin QFP
N343632LTQ-55N	5.5	100	340	100Pin TQFP
N343632LQF-6N	6	90	320	100Pin QFP
N343632LTQ-6N	6	90	320	100Pin TQFP
N343632LQF-7N	7	75	300	100Pin QFP
N343632LTQ-7N	7	75	300	100Pin TQFP
N343632LQF-8N	8	66	280	100Pin QFP
N343632LTQ-8N	8	66	280	100Pin TQFP
N343632LQF-10N	10	60	260	100Pin QFP
N343632LTQ-10N	10	60	260	100Pin TQFP
N343632LQF-12N	12	50	240	100Pin QFP
N343632LTQ-12N	12	50	240	100Pin TQFP