National Semiconductor

MM54HC173/MM74HC173 TRI-STATE® Quad D Flip-Flop

General Description

The MM54HC173/MM74HC173 is a high speed TRI-STATE QUAD D TYPE FLIP-FLOP that utilizes advanced silicon-gate CMOS technology. It possesses the low power consumption and high noise immunity of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device. The outputs are buffered, allowing this circuit to drive 15 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

The four D TYPE FLIP-FLOPS operate synchronously from a common clock. The TRI-STATE outputs allow the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip flops to remain in the same state. Clearing is enabled by taking the CLEAR input to a logic "1" level. The data outputs change state on the positive going edge of the clock.

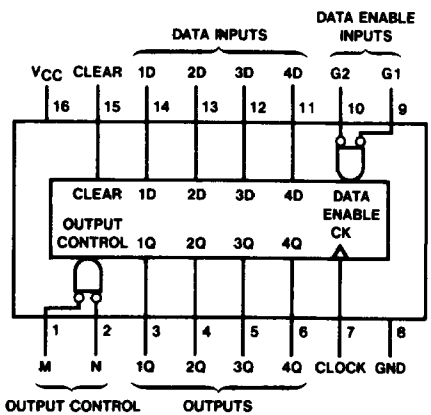
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating supply voltage range: 2–6V
- TRI-STATE outputs
- Low input current: 1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 6 mA minimum

Connection Diagram

Dual-In-Line Package



TL/F/5317–1

Top View

Order Number MM54HC173* or MM74HC173*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs					Output Q
Clear	Clock	Data Enable G1	Data Enable G2	Data D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state: however, sequential operation of the flip-flops is not affected.

H = high level (steady state)

L = low level (steady state)

↑ = low-to-high level transition

X = don't care (any input including transitions)

Q_0 = the level of Q before the indicated steady state input conditions were established

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND Enable = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=45$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay: Clock to Q			31	ns
t_{PHL}	Maximum Propagation Delay: Clear to Q		18	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	18	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	16	25	ns
t_S	Minimum Data Setup Time			20	ns
t_S	Minimum Data Enable Setup Time			20	ns
t_H	Minimum Data Hold Time			0	ns
t_H	Minimum Data Enable Hold Time			0	ns
t_W	Minimum Clock Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	55	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q	$C_L=50$ pF	2.0V	80	175	220	262	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	23	35	44	53	ns
		$C_L=150$ pF	4.5V	28	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	38	45	ns
		$C_L=150$ pF	6.0V	26	38	48	57	ns
t_{PHL}	Maximum Propagation Delay from Clear to Q	$C_L=50$ pF	2.0V	70	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	20	30	38	45	ns
		$C_L=150$ pF	4.5V	25	40	50	60	ns
		$C_L=50$ pF	6.0V	17	26	32	38	ns
		$C_L=150$ pF	6.0V	22	34	43	51	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	70	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	20	30	38	45	ns
		$C_L=150$ pF	4.5V	25	40	50	60	ns
		$C_L=50$ pF	6.0V	17	26	32	38	ns
		$C_L=150$ pF	6.0V	22	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	70	150	189	224	ns
			4.5V	20	30	38	45	ns
			6.0V	17	26	32	38	ns
t_S	Minimum Data or Data Enable Setup Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_{REM}	Minimum Removal Time		2.0V		90	112	135	ns
			4.5V		18	22	26	ns
			6.0V		15	19	22	ns
t_H	Minimum Data or Data Enable Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Clear or Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns

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AC Electrical Characteristics (Continued)

V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	5	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance	(per flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.