Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 32K (2K x 16-BIT)

IDT7133SA/LA
IDT7143SA/LA

FEATURES:

- High-speed access
  - — Military: 25/35/45/55/70/90ns (max.)
  - — Commercial: 20/25/35/45/55/70/90ns (max.)
- Low-power operation
  - — IDT7133/43SA
    Active: 500 mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7133/43LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in 68-pin ceramic PGA, Flatpack, and PLCC
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

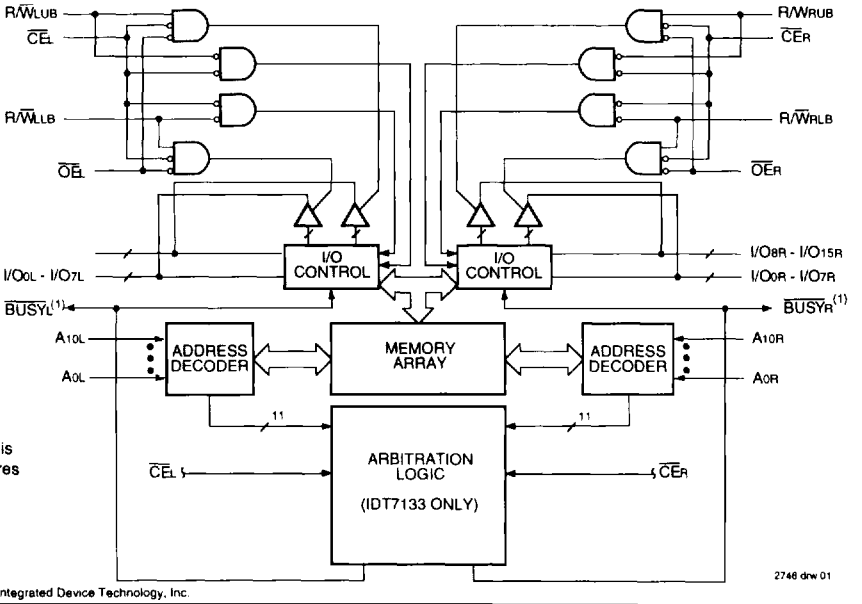
The IDT7133/7143 are high-speed 2K x 16 Dual-Port Static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7143 "SLAVE" Dual-Port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 500mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW for a 2V battery.

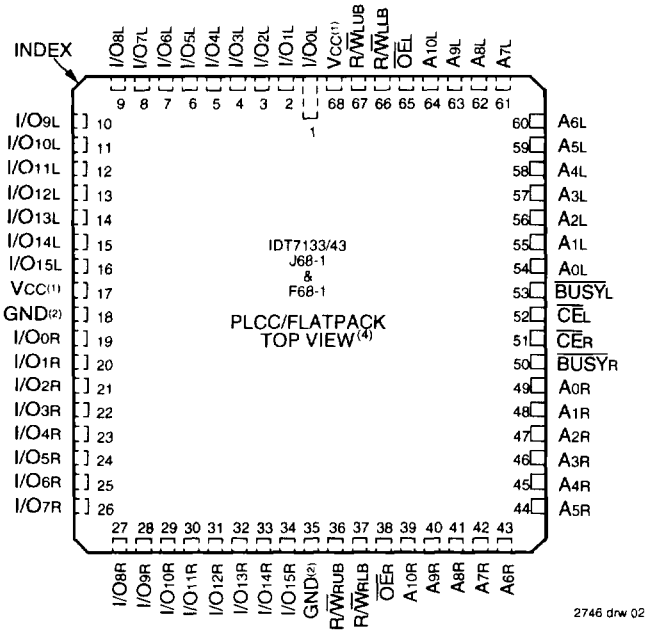
The IDT7133/7143 devices have identical pinouts. Each is packed in a 68-pin ceramic PGA, 68-pin flatpack, and 68-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

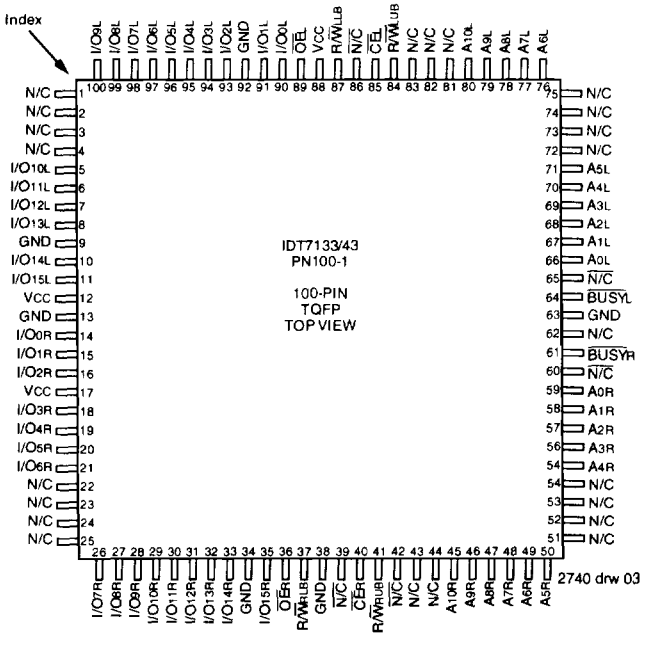
FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. IDT7133 (MASTER): BUSY is open drain output and requires pull-up resistor.
   IDT7143 (SLAVE): BUSY is input.
2. LB = LOWER BYTE
3. UB = UPPER BYTE

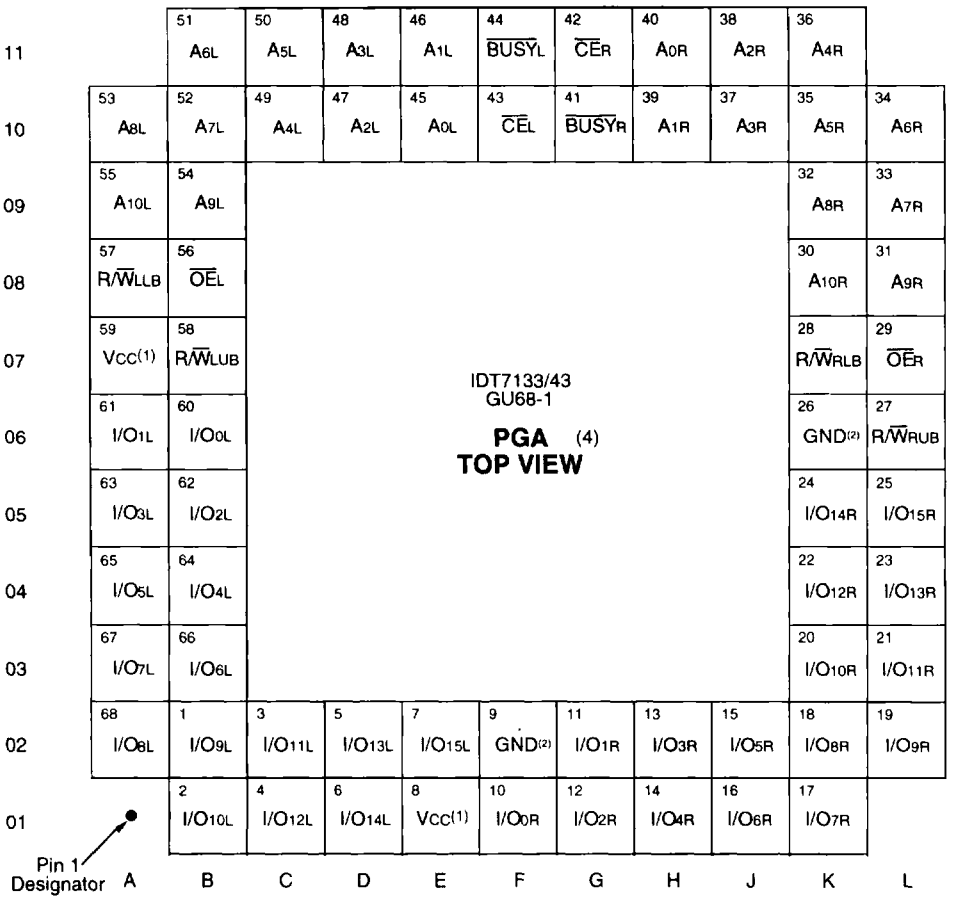
PIN CONFIGURATIONS[1,2,3]





NOTES:
1. Both Vcc pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte
4. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS (CONTINUED)[1,2,3]



2746 drw 03

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_{LUB}$	$R/\overline{W}_{RUB}$	Upper Byte Read/Write Enable
$R/\overline{W}_{LLB}$	$R/\overline{W}_{RLB}$	Lower Byte Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{10L}$	$A_{0R} - A_{10R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
V_{CC}		Power
GND		Ground

2746 tbl 01

NOTES:
1. Both Vcc pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte
4. This text does not indicate orientation of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T(3)	Power Dissipation	2.0	2.0	W
I_{OUT}	DC Output Current	50	50	mA

2746 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq$ Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	11	pF

2746 tbl 03

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2746 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2746 tbl 05

NOTES:
1. V_{IL} (min.) = -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Either port, Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7133SA IDT7143SA		IDT7133LA IDT7143LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	Vcc = 5.5V, V_{IN} = 0V to Vcc	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to Vcc	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_{15})	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2746 tbl 06

NOTES:
1. At Vcc < 2.0V, input leakages are undefined.

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DC ELECTRICAL CHARACTERISTICS
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT7133X20[1] IDT7143X20[1] Typ.[2]	Max.	IDT7133X25 IDT7143X25 Typ.[2]	Max.	IDT7133X35 IDT7143X35 Typ.[2]	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	S	250	350	250	330	240	325	mA
				L	230	310	230	300	220	295	
			COM'L.	S	250	310	250	300	240	295	
				L	230	280	230	270	210	250	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}[4]	MIL.	S	25	90	25	90	25	75	mA
				L	25	80	25	80	25	65	
			COM'L.	S	25	80	25	80	25	70	
				L	25	70	25	70	25	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5], f = f_{MAX}[4], Active Port Outputs Open	MIL.	S	140	230	140	230	120	200	mA
				L	120	210	100	190	100	180	
			COM'L.	S	140	200	140	200	120	180	
				L	120	180	100	170	100	160	
I_{SB3}	Full Standby Current (Both Ports — CMOS Level Inputs)	Both Ports $\overline{CE}_L$ & $\overline{CE}_R$ > V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or V_{IN} < 0.2V, f = 0[5]	MIL.	S	1	30	1	30	1	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1	15	1	15	1	15	
				L	0.2	5	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" < 0.2V and $\overline{CE}$"B" > V_{CC} - 0.2V[6] V_{IN} > V_{CC} - 0.2V or	MIL.	S	140	220	140	220	120	190	mA
				L	120	200	120	200	100	170	
		V_{IN} < 0.2V Active Port Outputs Open, f = f_{MAX}[4]	COM'L.	S	140	190	140	190	120	170	
				L	120	170	120	170	100	150	

OTES: 2746 tbl 07

1. Commercial only, 0°C to +70°C temperature range.
2. V_{CC} = 5V, T_A = +25°C for Typ., and are not production tested. I_{CCDC} = 180mA (Typ.)
3. "X" in part numbers indicates power rating (SA or LA)
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

DC ELECTRICAL CHARACTERISTICS
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT7133X45 IDT7143X45 Typ.[2]	IDT7133X45 IDT7143X45 Max.	IDT7133X55 IDT7143X55 Typ.[2]	IDT7133X55 IDT7143X55 Max.	IDT7133X70/90 IDT7143X70/90 Typ.[2]	IDT7133X70/90 IDT7143X70/90 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	S	230	320	230	315	230	310	mA
				L	210	290	210	285	210	280	
			COM'L.	S	230	290	230	285	230	280	
				L	210	260	210	255	210	250	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}[4]	MIL.	S	25	80	25	80	25	75	mA
				L	25	70	25	70	25	65	
			COM'L.	S	25	75	25	70	25	70	
				L	25	65	25	60	25	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5], f = f_{MAX}[4], Active Port Outputs Open	MIL.	S	120	210	120	210	120	200	mA
				L	100	190	100	190	100	180	
			COM'L.	S	120	190	120	180	120	180	
				L	100	170	100	160	100	160	
I_{SB3}	Full Standby Current (Both Ports — CMOS Level Inputs)	Both Ports $\overline{CE}_L$ & $\overline{CE}_R$ > V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or V_{IN} < 0.2V, f = 0[5]	MIL.	S	1	30	1	30	1	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1	15	1	15	1	15	
				L	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"}$ < 0.2V and $\overline{CE}_{"B"}$ > V_{CC} - 0.2V[6] V_{IN} > V_{CC} - 0.2V or V_{IN} < 0.2V Active Port Outputs Open, f = f_{MAX}[4]	MIL.	S	120	200	120	200	120	190	mA
				L	100	180	100	180	100	170	
			COM'L.	S	120	180	120	170	120	170	
				L	100	160	100	150	100	150	

NOTES:

2746 tbl 07

1. Commercial only, 0°C to +70°C temperature range.
2. V_{CC} = 5V, T_A = +25°C for Typ., and are not production tested. I_{CCDC} = 180mA (Typ.)
3. "X" in part numbers indicates power rating (SA or LA)
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

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DATA RETENTION CHARACTERISTICS

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

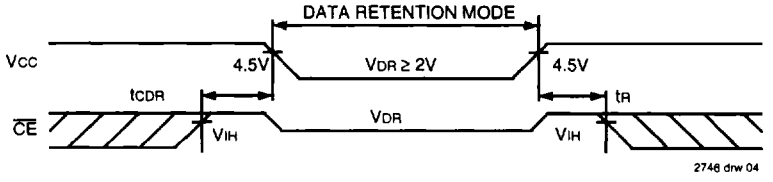
Symbol	Parameter	Test Condition		IDT7133LA/IDT7143LA Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES:

2746 tbl 08

1. V_{CC} = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but is not production tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2746 tbl 09

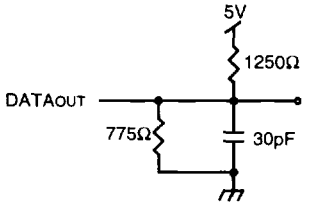


Figure 1. Output Load

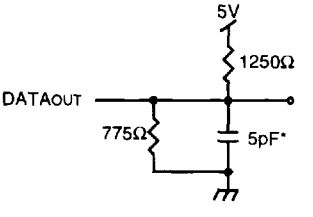


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig

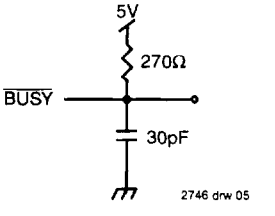


Figure 3. $\overline{BUSY}$ Output Load (IDT7133 only)

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4]

Symbol	Parameter	IDT7133X20[2] IDT7143X20[2] Min.	Max.	IDT7133X25 IDT7143X25 Min.	Max.	IDT7133X35 IDT7143X35 Min.	Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	20	—	25	—	35	—	ns
tAA	Address Access Time	—	20	—	25	—	35	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	ns
tAOE	Output Enable Access Time	—	12	—	15	—	20	ns
tOH	Output Hold from Address Change	3	—	0	—	0	—	ns
tLZ	Output Low-Z Time[1, 3]	3	—	0	—	0	—	ns
tHZ	Output High-Z Time[1, 3]	—	12	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[3]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[3]	—	20	—	50	—	50	ns

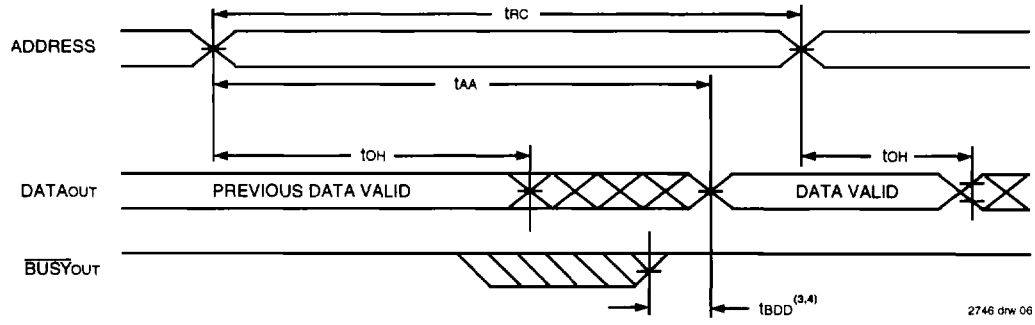
Symbol	Parameter	IDT7133X45 IDT7143X45 Min.	Max.	IDT7133X55 IDT7143X55 Min.	Max.	IDT7133X70/90 IDT7143X70/90 Min.	Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	45	—	55	—	70/90	—	ns
tAA	Address Access Time	—	45	—	55	—	70/90	ns
tACE	Chip Enable Access Time	—	45	—	55	—	70/90	ns
tAOE	Output Enable Access Time	—	25	—	30	—	40/40	ns
tOH	Output Hold from Address Change	0	—	0	—	0/0	—	ns
tLZ	Output Low-Z Time[1, 3]	0	—	5	—	5/5	—	ns
tHZ	Output High-Z Time[1, 3]	—	20	—	20	—	25/25	ns
tPU	Chip Enable to Power Up Time[3]	0	—	0	—	0/0	—	ns
tPD	Chip Disable to Power Down Time[3]	—	50	—	50	—	50/50	ns

2746 tbl 10

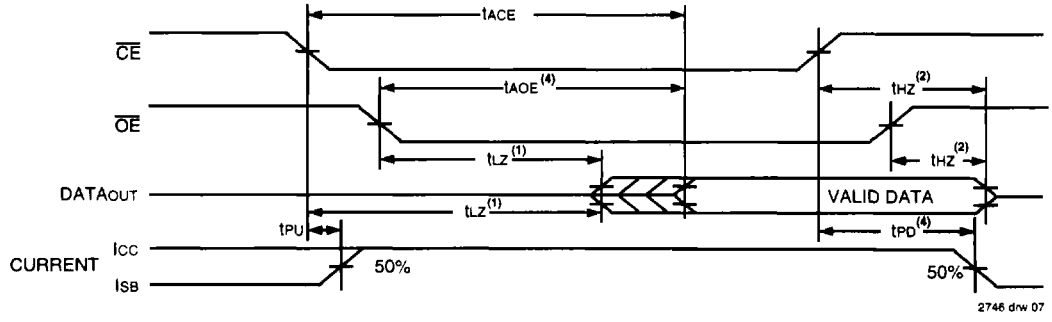
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed by device charactenzation, but is not production tested.
4. "X" in part number indicates power rating (SA or LA).

6

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deasserted last, $\overline{OE}$ or $\overline{CE}$.
3. tBDD delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultaneous read operations, $\overline{BUSY}$ has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last, tAOE, tACE, tAA, or tBDD.
5. $R/\overline{W} = V_{IH}$, and the address is valid prior to others coincidental with $\overline{CE}$ transition Low.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[7]

Symbol	Parameter	IDT7133x20[2] IDT7143X20[2] Min.	Max.	IDT7133x25 IDT7143x25 Min.	Max.	IDT7133x35 IDT7143x35 Min.	Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time[4]	20	—	25	—	35	—	ns
tEW	Chip Enable to End-of-Write	15	—	20	—	25	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	15	—	20	—	25	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	15	—	20	—	ns
tHZ	Output High-Z Time[1,3]	—	12	—	15	—	20	ns
tDH	Data Hold Time[5]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1,3]	—	12	—	15	—	20	ns
tOW	Output Active from End-of-Write[1,3,5]	3	—	0	—	0	—	ns

Symbol	Parameter	IDT7133x45 IDT7143X45 Min.	Max.	IDT7133x55 IDT7143x55 Min.	Max.	IDT7143x70/90 IDT7143x70/90 Min.	Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time[4]	45	—	55	—	70/90	—	ns
tEW	Chip Enable to End-of-Write	30	—	40	—	50/50	—	ns
tAW	Address Valid to End-of-Write	30	—	40	—	50/50	—	ns
tAS	Address Set-up Time	0	—	0	—	0/0	—	ns
tWP	Write Pulse Width[6]	30	—	40	—	50/50	—	ns
tWR	Write Recovery Time	0	—	0	—	0/0	—	ns
tDW	Data Valid to End-of-Write	20	—	25	—	30/30	—	ns
tHZ	Output High-Z Time[1,3]	—	20	—	20	—	25/25	ns
tDH	Data Hold Time[5]	5	—	5	—	5/5	—	ns
tWZ	Write Enable to Output in High-Z[1,3]	—	20	—	20	—	25/25	ns
tOW	Output Active from End-of-Write[1,3,5]	5	—	5	—	5/5	—	ns

NOTES:

2746 tbl 11

1. Transition is measured ± 500mV from Low- or High-impedence voltage from the Output Test Load.
2. 0° C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.
4. For MASTER/SLAVE combination, tWC = tBAA + tWR + tWP, since R/$\overline{W}$ = VIL must occur after tBAA
5. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will very over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
6. This parameter is determined by device characterization, but is not production tested. Transition is measured ±200mV from steady state with the Output Test Load (Figure 2).
7. "X" in part number indicates power rating (SA or LA).

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[7]

Symbol	Parameter	IDT7133x20[1] IDT7143X20[1] Min.	IDT7133x20[1] IDT7143X20[1] Max.	IDT7133x25 IDT7143x25 Min.	IDT7133x25 IDT7143x25 Max.	IDT7133x35 IDT7143x35 Min.	IDT7133x35 IDT7143x35 Max.	Unit
BUSY TIMING (For MASTER IDT7133)								
tBAA	$\overline{BUSY}$ Access Time from Address	---	20	—	20	—	30	ns
tBDA	$\overline{BUSY}$ Disable Time from Address	---	20	—	20	—	30	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable	---	20	—	20	—	25	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable	—	17	—	20	—	25	ns
tWDD	Write Pulse to Data Delay[2]	—	40	—	50	—	60	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	30	—	45	—	55	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	20	—	Note 3	—	Note 3	ns
tAPS	Arbitration Priority Set Up Time[4]	5	—	5	—	5/5	—	ns
BUSY INPUT TIMING (For SLAVE IDT7143)								
tWB	Write to $\overline{BUSY}$	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	20	—	20	—	25	—	ns
tWDD	Write Pulse to Data Delay[2]	—	40	—	60	—	80	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	30	—	45	—	55	ns

2746 tbl 12

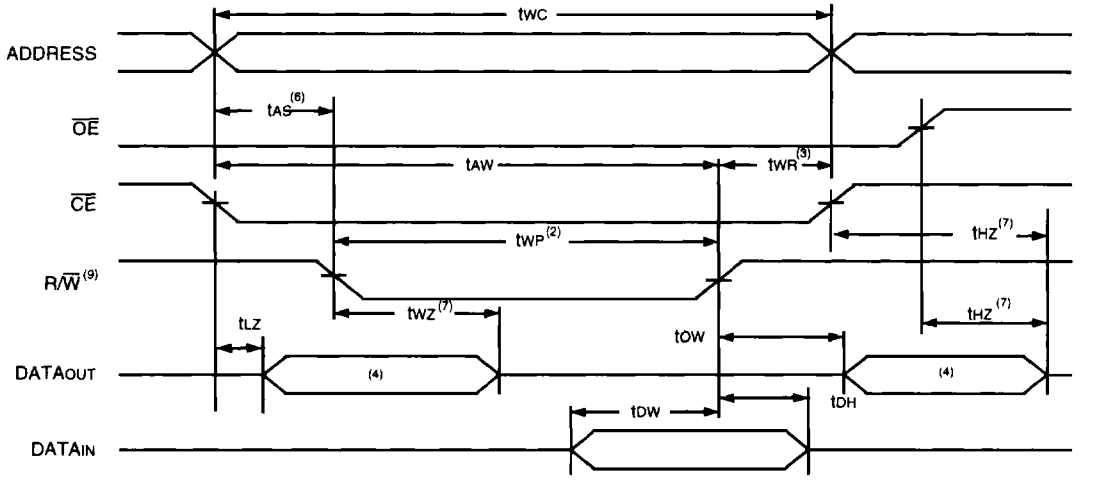
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[7]

Symbol	Parameter	IDT7133x45 IDT7143x45 Min.	IDT7133x45 IDT7143x45 Max.	IDT7133x55 IDT7143X55 Min.	IDT7133x55 IDT7143X55 Max.	IDT7133x70/90 IDT7143X70/90 Min.	IDT7133x70/90 IDT7143X70/90 Max.	Unit
BUSY TIMING (For MASTER IDT7133)								
tBAA	$\overline{BUSY}$ Access Time from Address	---	40	—	40	—	45/45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address	---	40	—	40	—	45/45	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable	---	30	—	35	—	35/35	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable	—	25	—	30	—	30/30	ns
tWDD	Write Pulse to Data Delay[2]	—	80	—	80	—	90/90	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	35	—	55	—	70/70	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 3	—	Note 3	—	Note 3	ns
tAPS	Arbitration Priority Set Up Time[4]	5	—	5	—	5/5	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	30	—	30	—	30/30	—	ns
BUSY INPUT TIMING (For SLAVE IDT7143)								
tWB	Write to $\overline{BUSY}$	0	—	0	—	0/0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	30	—	30	—	30/30	—	ns
tWDD	Write Pulse to Data Delay[2]	—	80	—	80	—	90/90	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	55	—	55	—	70/70	ns

2746 tbl 12

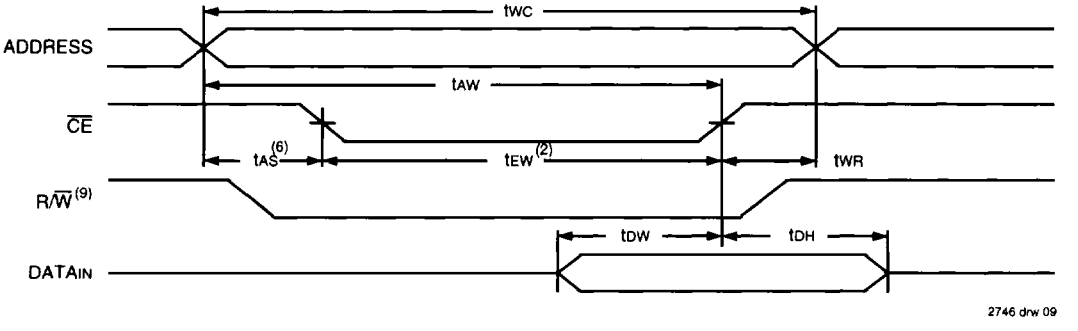
NOTES:
1. 0°C to +70°C temperature range only.
2. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and Busy".
3. t BDD is calculated parameter and is greater of 0, tWDD - tWP (actual) or tDDD - tDW (actual).
4. To ensure that the earlier of the two ports wins.
5. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
6. To ensure that a write cycle is completed on port "B" after contention on port "A".
7. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)[1, 5, 8]



2746 drw 08

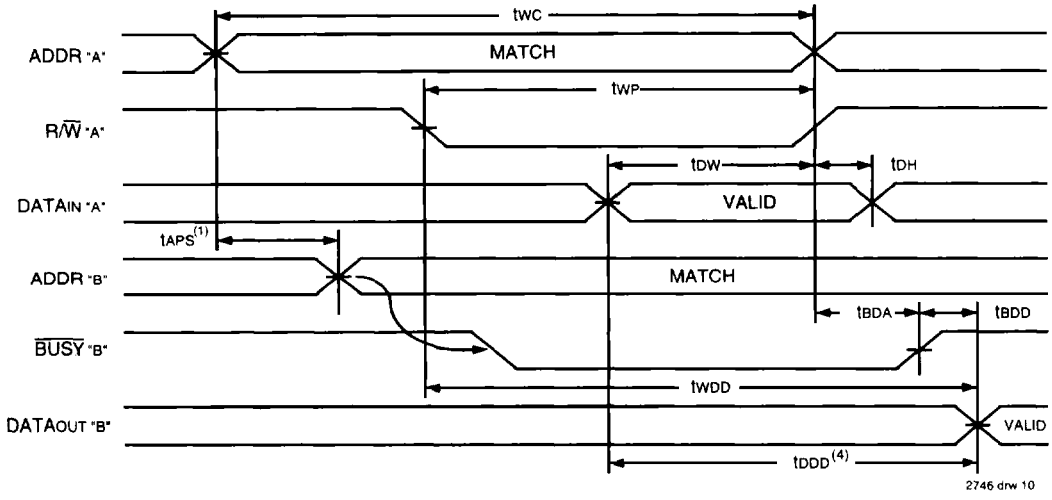
WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED TIMING)[1, 5]



2746 drw 09

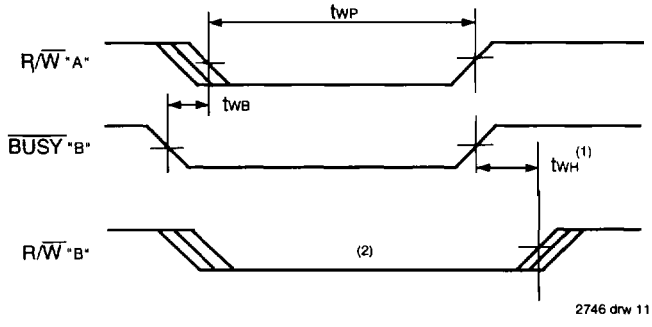
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a $\overline{CE}$ = VIL and a R/$\overline{W}$ = VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined by device characterization, but is not production tested. Transition is measured ± 200mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. R/$\overline{W}$ for either upper or lower byte.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (1, 2, 3)



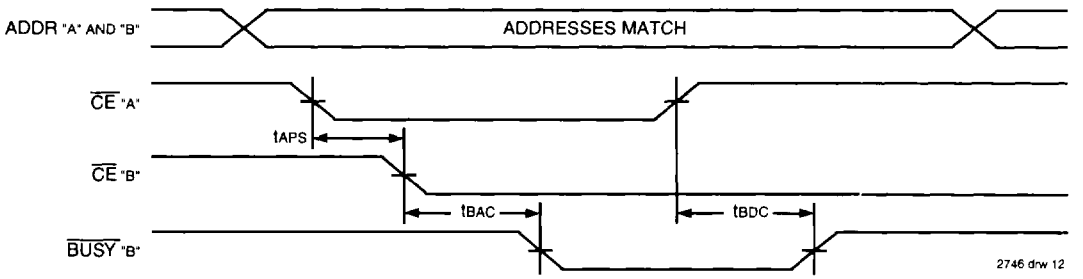
NOTES:
1. To ensure that the earlier of the two ports wins, tAPS is ignored for Slave (IDT7143).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (M/$\overline{S}$ = VIL)

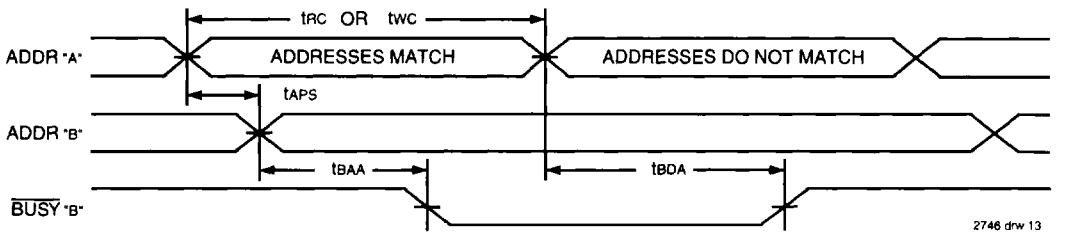


NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$ "B", until $\overline{BUSY}$ "B" goes High.
3. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING (1)



TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESSES (1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted (IDT7133 only).

6

FUNCTIONAL DESCRIPTION:

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7133/43 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Non-contention READ/WRITE conditions are illustrated in Table 1.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by using the IDT7143 (SLAVE). In the IDT7143, the busy pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low. The busy outputs on the IDT7133 RAM are open drain and require pull-up resistors.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7133/43 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7133 RAM the busy pin is an output and on the IDT7143 RAM, the busy pin is an input (see Figure 3).

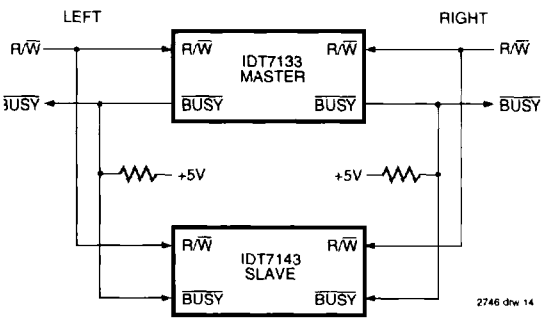


Figure 4. Busy and chip enable routing for both width and depth expansion with the IDT7133 (MASTER) and the IDT7143 (SLAVE).

Expanding the data bus width to 32 bits or more in a Dual-Port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will await indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding Dual-Port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all Dual-Port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLE I – NON-CONTENTION READ/WRITE CONTROL[4]

LEFT OR RIGHT PORT[1]						
$R/\overline{W}_{LB}$	$R/\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	Function
X	X	H	X	Z	Z	Port Disabled and in Power Down Mode, I_{SB2}, I_{SB4}
X	X	H	X	Z	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power Down Mode, I_{SB1} or I_{SB3}
L	L	L	X	$DATA_{IN}$	$DATA_{IN}$	Data on Lower Byte and Upper Byte Written into Memory[2]
L	H	L	L	$DATA_{IN}$	$DATA_{OUT}$	Data on Lower Byte Written into Memory[2], Data in Memory Output on Upper Byte[3]
H	L	L	L	$DATA_{OUT}$	$DATA_{IN}$	Data in Memory Output on Lower Byte[3], Data on Upper Byte Written into Memory[2]
L	H	L	H	$DATA_{IN}$	Z	Data on Lower Byte Written into Memory[2]
H	L	L	H	Z	$DATA_{IN}$	Data on Upper Byte Written into Memory[2]
H	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Data in Memory Output on Lower Byte and Upper Byte
H	H	L	H	Z	Z	High Impedance Outputs

NOTES: 2746 tbl 13

1. A_{0L} - $A_{10L} \neq A_{0R}$ - A_{10R}
2. If $\overline{BUSY}$ = LOW, data is not written.
3. If $\overline{BUSY}$ = LOW, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. "H" = HIGH, "L" = LOW, "X" = Don't Care, "Z" = High Impedance, "LB" = Lower Byte, "UB" = Upper Byte

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

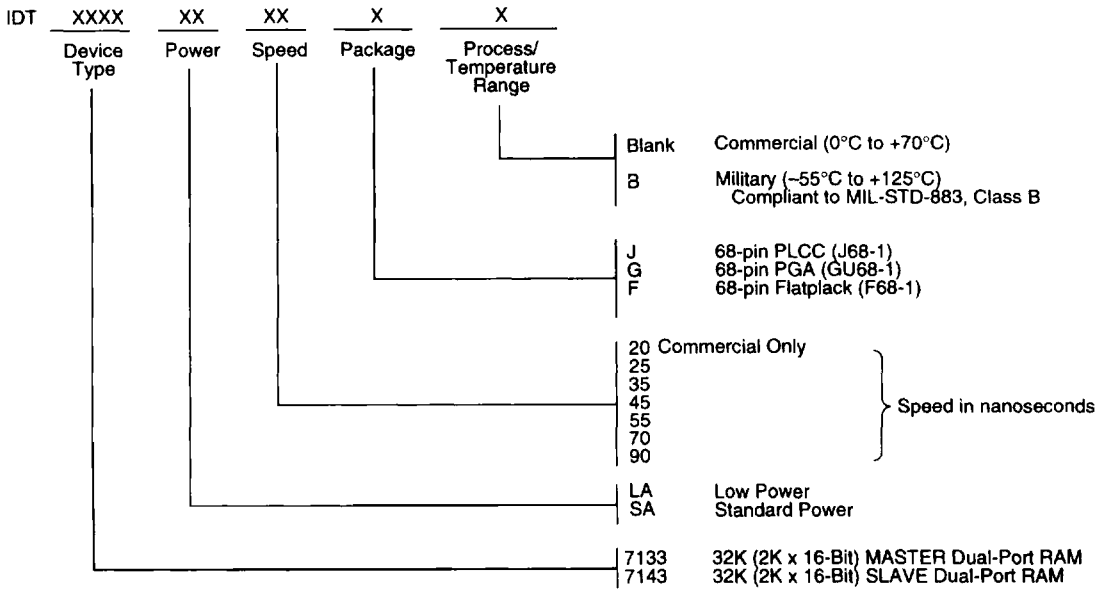
Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{10L} A_{0R}-A_{10R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

NOTES: 2746 tbl 14

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs on the IDT7133 (MASTER). Both are inputs on the IDT7143 (SLAVE). On Slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

6

ORDERING INFORMATION



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