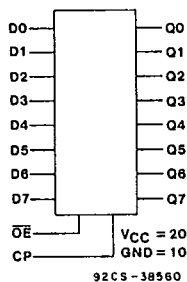


**CD54/74HC374, CD54/74HCT374
CD54/74HC574, CD54/74HCT574**

File Number 1663

HARRIS SEMICONDUCTOR SECTOR 27E D 4302271 0017803 7 HAS

High-Speed CMOS Logic



**Octal D-Type Flip-Flop, 3-State
Positive-Edge Triggered**

Type Features:

- Common 3-State Output Enable Control
- Buffered Inputs
- 3-State Outputs
- Bus Line Driving Capability
- Typical Propagation Delay (Clock to Q) = 15 ns @ $V_{CC} = 5 V, C_L = 15 pF, T_A = 25^\circ C$

FUNCTIONAL DIAGRAM

The RCA CD54/74HC374/574 and CD54/74HCT374/574 are Octal D-Type Flip-Flops with 3-State Outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The Output Enable (\overline{OE}) controls the 3-state outputs and is independent of the register operation. When Output Enable (\overline{OE}) is HIGH the outputs will be in the high impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

The CD54HC/HCT374/574 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD54HC/HCT374/574 are supplied in a 20-lead plastic dual-in-line package (E suffix) and in 20-lead plastic dual-in-line surface mount plastic packages (M suffix). The CD54HC/HCT374/574 are also supplied in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to $+85^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Sigmetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 30\%, N_{IH} = 30\% \text{ of } V_{CC} @ V_{CC} = 5 V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8 V \text{ Max.}, V_{IH} = 2 V \text{ Min.}$
CMOS Input Compatibility
 $I_I \leq 1 \mu A @ V_{OL}, V_{OH}$

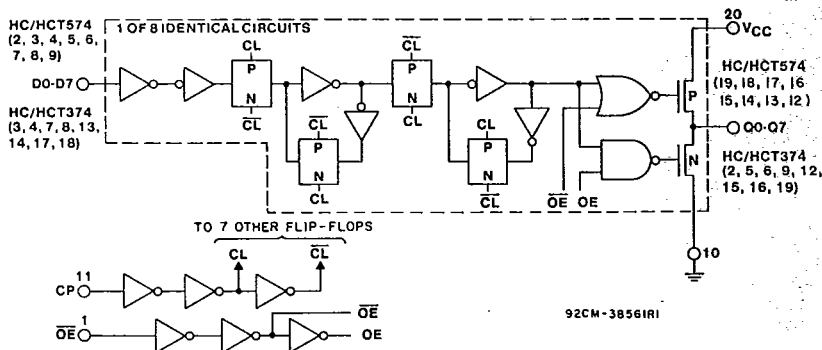


Fig. 1 - Logic diagram.

**CD54/74HC374, CD54/74HCT374
CD54/74HC574, CD54/74HCT574**

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) -0.5 to +7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR V_i < -0.5 V OR V_i > V_{CC} + 0.5V) ±20mA

DC OUTPUT DIODE CURRENT, I_{OK} (FOR V_o < -0.5 V OR V_o > V_{CC} + 0.5V) ±20mA

DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < V_o < V_{CC} + 0.5V) ±35mA

DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC}) ±70mA

POWER DISSIPATION PER PACKAGE (P_o):

For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW

For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 8 mW/°C to 300 mW

For T_A = -55 to +100°C (PACKAGE TYPE F, H) 500 mW

For T_A = +100 to +125°C (PACKAGE TYPE F, H) Derate Linearly at 8 mW/°C to 300 mW

For T_A = -40 to +70°C (PACKAGE TYPE M) 400 mW

For T_A = +70 to +125°C (PACKAGE TYPE M) Derate Linearly at 6 mW/°C to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H -55 to +125°C

PACKAGE TYPE E, M -40 to +85°C

STORAGE TEMPERATURE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265°C

Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range) V _{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V _i , V _o	0	V _{CC}	V
Operating Temperature T _A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t _r , t _f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

TRUTH TABLE			
INPUTS			OUTPUTS
OE	CP	Dn	Qn
L	↗	H	H
L	↗	L	L
L	L	X	Q0
H	X	X	Z

HC/HCT374,574

H = high level (steady state)
 L = low level (steady state)
 X = don't care
 ↗ = transition from low to high level
 Q0 = the level of Q before the indicated steady-state input conditions were established.
 Z = high impedance

HARRIS SEMICONDUCTOR 27E D 430227J 0017804 9 HAS

CD54/74HC374, CD54/74HCT374
CD54/74HC574, CD54/74HCT574

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC374/CD54HC374 CD74HC574/CD54HC574										CD74HCT374/CD54HCT374 CD74HCT574/CD54HCT574										UNITS			
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES			54HC SERIES			TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES				54HCT SERIES		
	V _i V	I _o mA	V _{cc} V	+25°C			-40/ +85°C			-55/ +125°C			V _i V	V _{cc} V	+25°C			-40/ +85°C				-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min		Max		
High-Level Input Voltage V _{oh}			2	1.5	—	—	1.5	—	1.5	—	—	—	4.5	to	2	—	—	2	—	2	—	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	—	5.5											
			6	4.2	—	—	4.2	—	4.2	—	—	—												
Low-Level Input Voltage V _{ol}			2	—	—	0.5	—	0.5	—	0.5	—	—	4.5	to	—	—	0.8	—	0.8	—	0.8	—	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	—	5.5											
			6	—	—	1.8	—	1.8	—	1.8	—	—												
High-Level Output Voltage V _{oh}	V _{ih}		2	1.9	—	—	1.9	—	1.9	—	—	V _{ih}	4.5										V	
or	-0.02		4.5	4.4	—	—	4.4	—	4.4	—	—	or	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	V	
CMOS Loads	V _{ih}		6	5.9	—	—	5.9	—	5.9	—	—	V _{ih}												
TTL Loads (Bus Driver)	V _{ih}											V _{ih}	4.5	3.98	—	—	3.84	—	3.7	—	—	—	V	
or	-6		4.5	3.98	—	—	3.84	—	3.7	—	—	or												
	V _{ih}		6	5.48	—	—	5.34	—	5.2	—	—	V _{ih}												
Low-Level Output Voltage V _{ol}	V _{oh}		2	—	—	0.1	—	0.1	—	0.1	—	V _{oh}	4.5										V	
or	0.02		4.5	—	—	0.1	—	0.1	—	0.1	—	or												
CMOS Loads	V _{oh}		6	—	—	0.1	—	0.1	—	0.1	—	V _{oh}												
TTL Loads (Bus Driver)	V _{oh}											V _{oh}	4.5										V	
or	6		4.5	—	—	0.26	—	0.33	—	0.4	—	or												
	V _{oh}		7.8	6	—	—	0.26	—	0.33	—	0.4	V _{oh}												
Input Leakage Current I _i	V _{cc}		6	—	—	±0.1	—	±1	—	±1	—	Any Voltage Between V _{cc} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	±1	μA	
or	Gnd																							
Quiescent Device Current I _{cc}	V _{cc}		0	6	—	—	8	—	80	—	160	V _{cc}	5.5	—	—	8	—	80	—	160	—	160	μA	
or	Gnd											or												
Additional Quiescent Device Current per input pin, 1 unit load ΔI _{cc} *												V _{cc} -2.1	4.5	to	—	100	360	—	450	—	490	—	μA	
												5.5												
3-State Leakage Current	V _{ih}	V _o = V _{cc}	6	—	—	±0.5	—	±5.0	—	±10	—	V _{ih}	5.5	—	—	±0.5	—	±5.0	—	±10	—	±10	μA	
or	V _o											or												
	V _o	Gnd										V _{ih}												

*For dual-supply systems theoretical worst case (V_i = 2.4 V, V_{cc} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*	
	HCT374	HCT574
D0-D7	0.3	0.4
CP	0.9	0.75
OE	1.3	0.6

*Unit Load is ΔI_{cc} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

HARRIS SEMICONDUCTOR 27E D 430227J 0017805 0 HAS

CD54/74HC374, CD54/74HCT374 CD54/74HC574, CD54/74HCT574

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r = 6\text{ ns}$)

CHARACTERISTIC	C_L (pF)	TYPICAL		UNITS
		HC	HCT	
Propagation Delay Clock to Q	t_{PLH} t_{PHL}	15	15	ns
Propagation Delay Output Disable to Q	t_{PLZ} t_{PHZ}	11	11	ns
Propagation Delay Output Enable to Q	t_{PZL} t_{PZH}	12	12	ns
Max Clock Frequency	f_{max}	60	60	MHz
Power Dissipation Capacitance	C_{PD}^*	39	47	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_o C_L$ where

f_i = input frequency,

f_o = output frequency,

C_L = output load capacitance

V_{CC} = supply voltage

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	V_{CC} V	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
	4.5	30	—	30	—	25	—	25	—	20	—	20	—	
	6	35	—	—	—	29	—	—	—	23	—	—	—	
Clock Pulse Width Fig. 2	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time Data to Clock Fig. 3	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
	4.5	12	—	12	—	15	—	15	—	18	—	18	—	
	6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time Data to Clock Fig. 3	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
	4.5	5	—	5	—	5	—	5	—	5	—	5	—	
	6	5	—	—	—	5	—	—	—	5	—	—	—	

**CD54/74HC374, CD54/74HCT374
CD54/74HC574, CD54/74HCT574**

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = 6$ ns)

CHARACTERISTIC	V_{CC} V	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Clock to Output Fig. 2	t_{PLH} t_{PHL} 6	— — —	165 33 28	— — —	— — —	205 41 35	— — —	— — —	41 35	— — —	250 50 43	— — —	50	ns
Propagation Delay Output Disable to Q Fig. 4	t_{PLZ} t_{PHZ} 6	— — —	135 27 23	— — —	— — —	170 34 29	— — —	— — —	35 35	— — —	205 41 35	— — —	42	ns
Propagation Delay Output Enable to Q Fig. 4	t_{PZL} t_{PZH} 6	— — —	150 30 26	— — —	— — —	190 38 33	— — —	— — —	38 38	— — —	225 45 38	— — —	45	ns
Output Transition Time Fig. 2	t_{TLH} t_{THL} 6	— — —	60 12 10	— — —	— — —	75 15 13	— — —	— — —	15 15	— — —	90 18 15	— — —	18	ns
Input Capacitance	C_i	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_o	—	20	—	20	—	20	—	20	—	20	—	20	pF

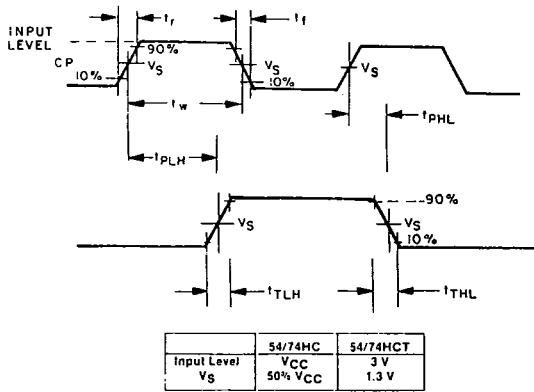


Fig. 2 — Clock to output delays and clock pulse width.

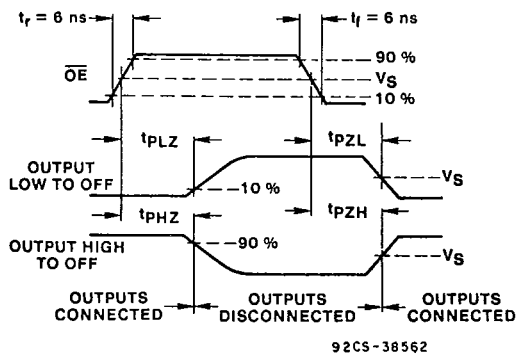


Fig. 4 — Transition times and propagation delay times.

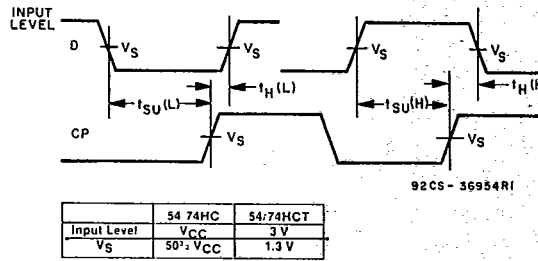
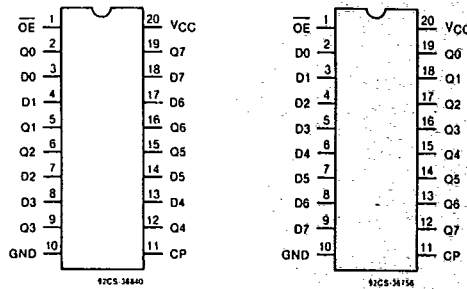


Fig. 3 — Data set-up and hold times.

Input Level V_S	54/74HC V_{CC} 50% V_{CC}	54/74HCT 3 V 1.3 V

Input Level V_S	54/74HC V_{CC}	54/74HCT 3 V 1.3 V



CD54/74HC, HCT374 Types
TERMINAL ASSIGNMENT

CD54/74HC, HCT574 Types
TERMINAL ASSIGNMENT

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

HARRIS SEMICONDUCTOR 27E D 430227J 0017807 4 HAS