

SN54F86, SN74F86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SDFS019B – JANUARY 1989 – REVISED JANUARY 1997

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

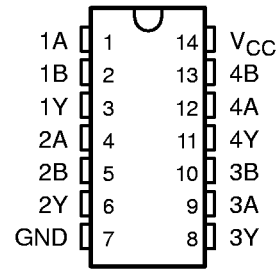
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN54F86 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74F86 is characterized for operation from 0°C to 70°C .

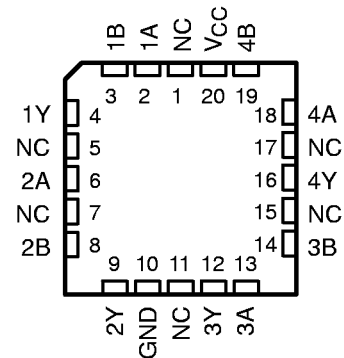
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

SN54F86 . . . J PACKAGE
SN74F86 . . . D OR N PACKAGE
(TOP VIEW)

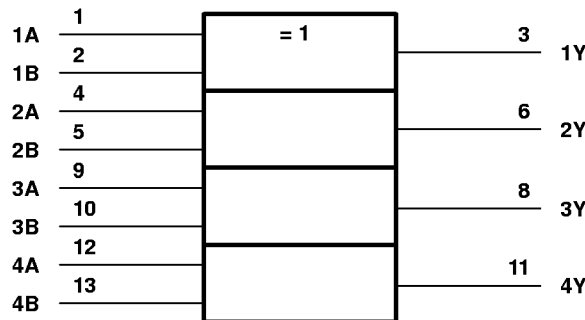


SN54F86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.



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**TEXAS
INSTRUMENTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F86			SN74F86			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$	-1.2			-1.2			V
V_{OH}	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -1\text{ mA}$	2.5	3.4		2.5	3.4		V
	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -1\text{ mA}$				2.7			
V_{OL}	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 20\text{ mA}$	0.3 0.5			0.3 0.5			V
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$	0.1			0.1			mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$	20			20			μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$	-0.6			-0.6			mA
I_{OS}^\ddagger	$V_{CC} = 5.5\text{ V}$,	$V_O = 0$	-60		-150	-60		-150	mA
I_{CCH}	$V_{CC} = 5.5\text{ V}$,	See Note 3	15		23	15		23	mA
I_{CCL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 4.5\text{ V}$	18		28	18		28	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: I_{CCH} is measured with outputs open, and the A or B input (not both) at 4.5 V. Remaining inputs are grounded.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = \text{MIN to MAX}^\S$				UNIT
			F86			SN54F86		SN74F86		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B (other input low)	Y	3	4	5.5	3	7	3	6.5	ns
t_{PHL}			3	4.2	5.5	2.6	8	3	6.5	
t_{PLH}	A or B (other input high)	Y	3.5	5.3	7	3.5	10	3.5	8	ns
t_{PHL}			3	4.7	6.5	3	8	3	7.5	

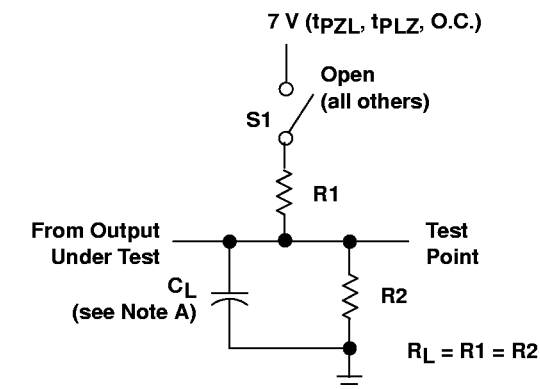
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



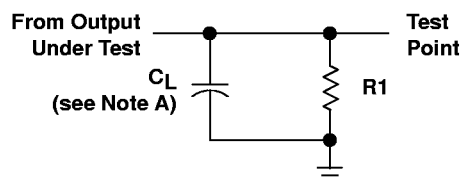
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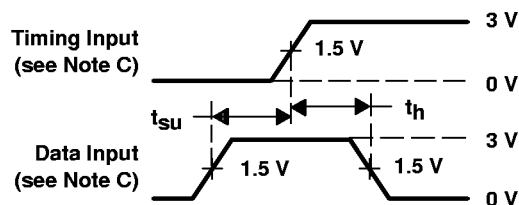
PARAMETER MEASUREMENT INFORMATION



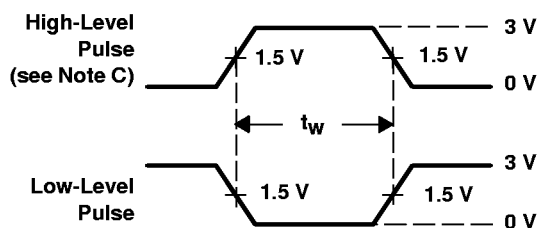
LOAD CIRCUIT FOR 3-STATE AND OPEN-COLLECTOR OUTPUTS



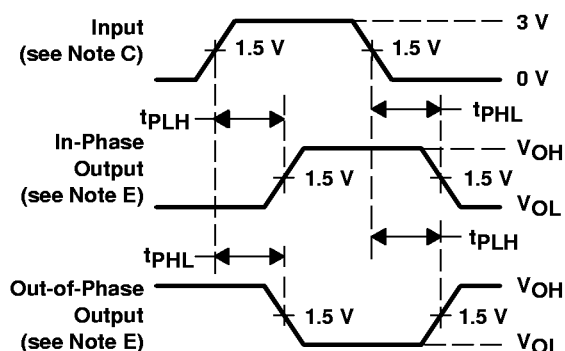
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



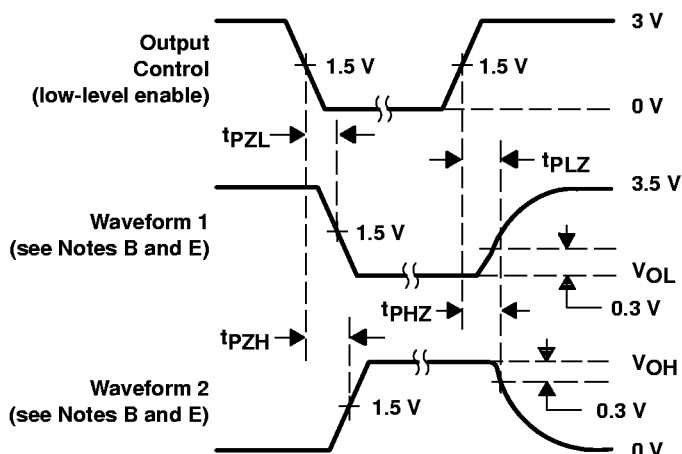
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is open.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms