FEMTOCLOCKS™ CRYSTAL-TO-LVDS FREQUENCY SYNTHESIZER

ICS844002

GENERAL DESCRIPTION

The ICS844002 is a 2 output LVDS Synthesizer optimized to generate Fibre Channel reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 26.5625MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 212.5MHz, 187.5MHz, 159.375MHz, 106.25MHz and 53.125MHz. The ICS844002 uses IDT's 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Fibre Channel jitter requirements. The ICS844002 is packaged in a small 20-pin TSSOP package.

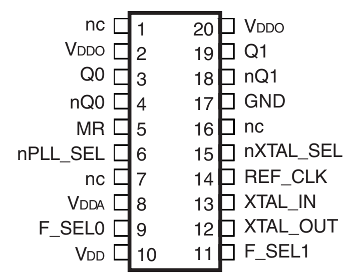
FEATURES

- Two LVDS outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 212.5MHz, 187.5MHz, 159.375MHz, 106.25MHz and 53.125MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 212.5MHz, using a 26.5625MHz crystal (637kHz - 10MHz): 0.65ps (typical)
- Full 3.3V or 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

FREQUENCY SELECT FUNCTION TABLE

Inputs						Output Frequency (MHz)
Input Frequency (MHz)	F_SEL1	F_SEL0	M Divider Value	N Divider Value	M/N Divider Value	
26.5625	0	0	24	3	8	212.5 (default)
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
23.4375	0	0	24	3	8	187.5 (default)

PIN ASSIGNMENT



ICS844002
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

BLOCK DIAGRAM

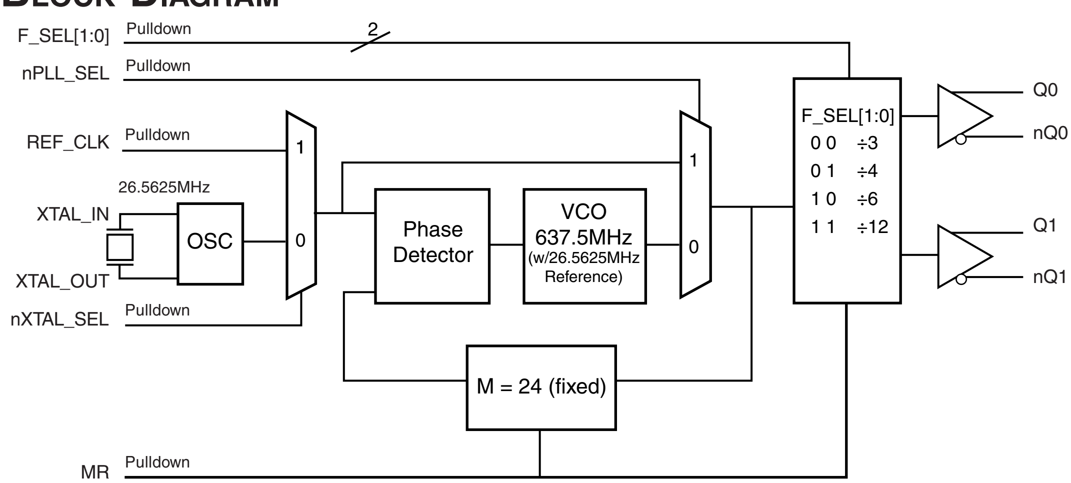


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 7	nc	Unused		No connect.
2, 20	V_{DDO}	Power		Output supply pins.
3, 4	Q0, nQ0	Ouput		Differential output pair. LVDS interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	nPLL_SEL	Input	Pulldown	Selects between the PLL and REF_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8	V_{DDA}	Power		Analog supply pin.
9, 11	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
10	V_{DD}	Power		Core supply pins.
12, 13	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
14	REF_CLK	Input	Pulldown	LVCMOS/LVTTL reference clock input.
15	nXTAL_SEL	Input	Pulldown	Selects between crystal or REF_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels.
16	nc	Unused		No connect.
17	GND	Power		Power supply ground.
18, 19	nQ1, Q1	Output		Differential output pair. LVDS interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				105	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				120	mA

Table 3B. Power Supply DC Characteristics, $V_{DD} = V_{DDO}$ = 2.5V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				95	mA
I_{DDA}	Analog Supply Current				10	mA
I_{DDO}	Output Supply Current				90	mA

Table 3C. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5% or 2.5V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	REF_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL,	$V_{DD} = V_{IN}$ = 3.465 or 2.5V			150	µA
I_{IL}	Input Low Current	REF_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL,	V_{DD} = 3.465V or 2.5V, V_{IN} = 0V	-150			µA

TABLE 3D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	450	600	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.4	1.525	1.65	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 3E. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	400	550	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.0		1.4	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		23.33	26.5625	28.33	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	186.67		226.66	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] = 11	46.67		56.66	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				15	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	212.5MHz, (637kHz - 10MHz)		0.65		ps
		159.375MHz, (637kHz - 10MHz)		0.61		ps
		106.25MHz, (637kHz -10MHz)		0.74		ps
		53.125MHz, (637kHz - 10MHz)		0.64		ps
		187.5MHz, (637kHz - 10MHz)		0.80		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		500	ps
odc	Output Duty Cycle	F_SEL[1:0] ≠ ÷3	48		52	%
		F_SEL[1:0] = ÷3	45		55	%

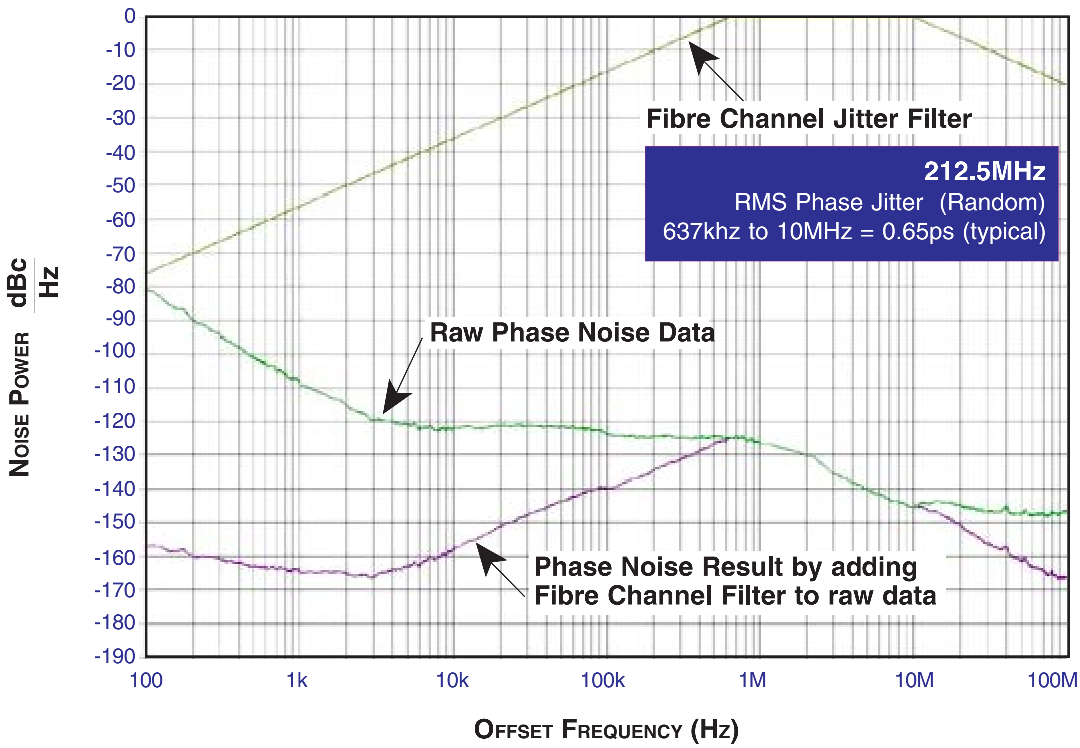
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 2.5V±5%, TA = 0°C TO 70°C

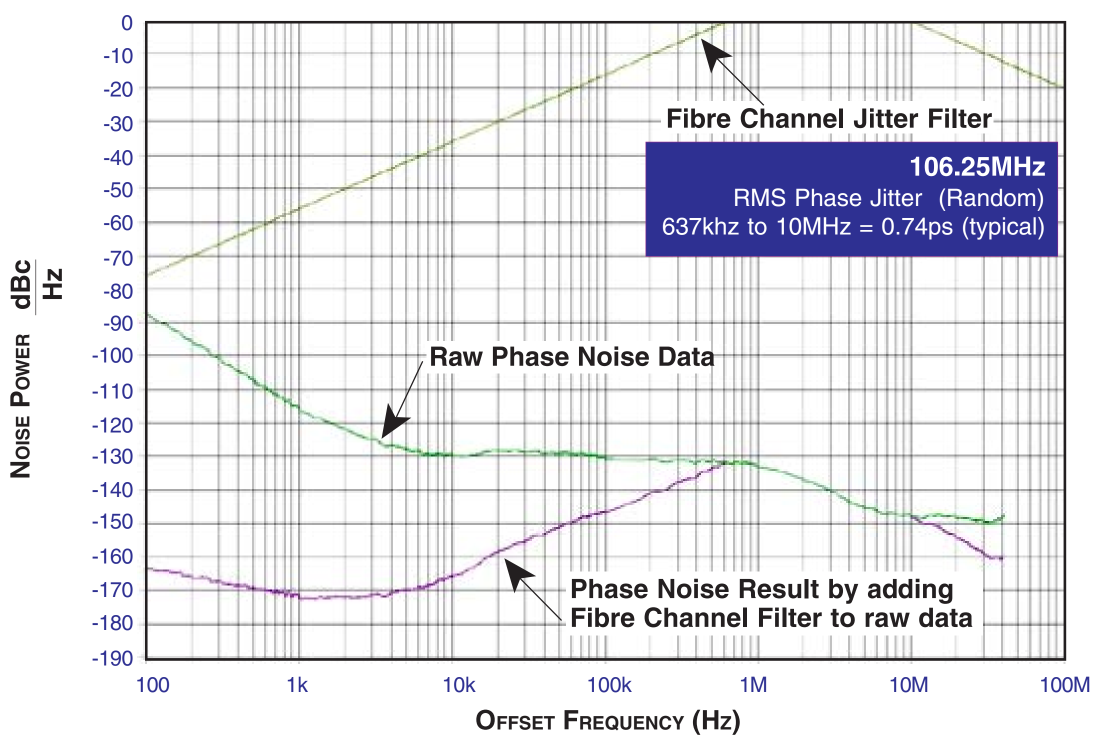
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	186.67		226.66	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] = 11	46.67		56.66	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				15	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	212.5MHz, (637kHz - 10MHz)		0.65		ps
		159.375MHz, (637kHz - 10MHz)		0.61		ps
		106.25MHz, (637kHz -10MHz)		0.74		ps
		53.125MHz, (637kHz - 10MHz)		0.64		ps
		187.5MHz, (637kHz - 10MHz)		0.80		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		500	ps
odc	Output Duty Cycle	F_SEL[1:0] ≠ ÷3	48		52	%
		F_SEL[1:0] = ÷3	45		55	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

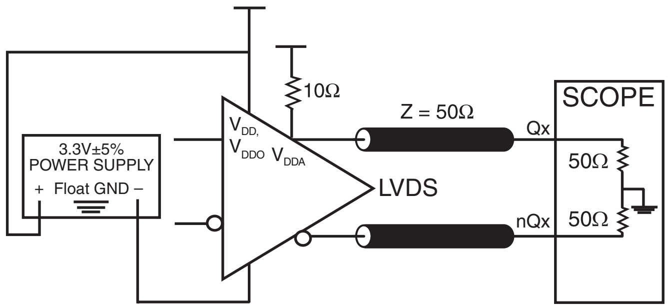
Typical Phase Noise at 212.5MHz



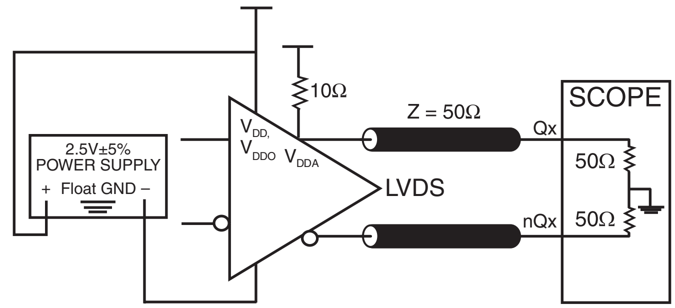
Typical Phase Noise at 106.25MHz



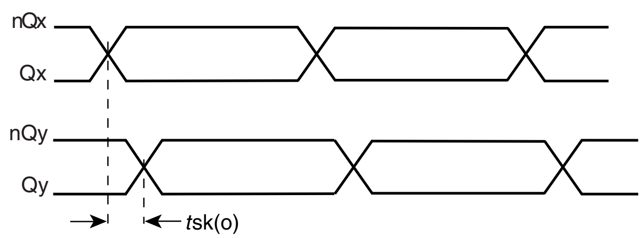
Parameter Measurement Information



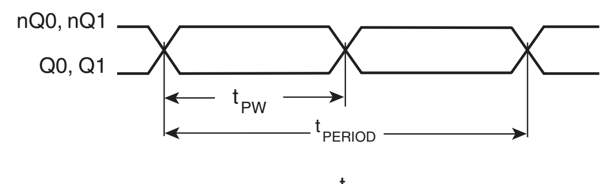
3.3V Core/3.3V Output Load AC Test Circuit



2.5V Core/2.5V Output Load AC Test Circuit

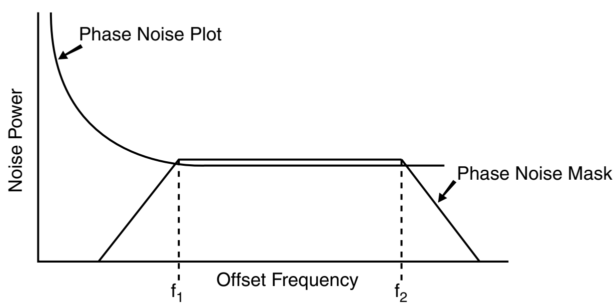


Output Skew



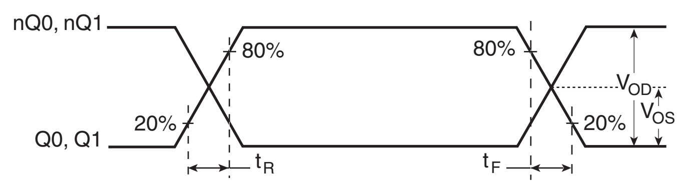
$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period

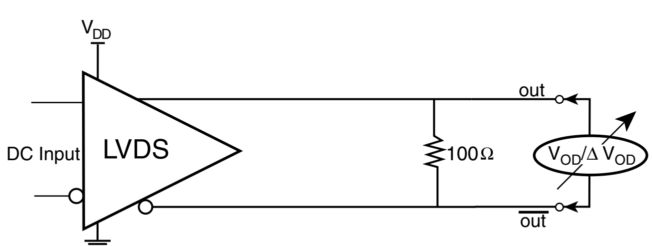


RMS Jitter = $\sqrt{\text{Area Under the Masked Phase Noise Plot}}$

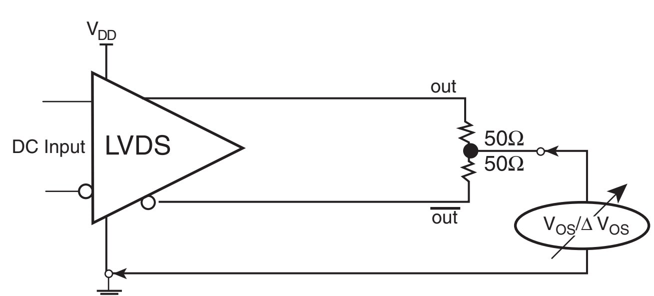
RMS Phase Jitter



Output Rise/Fall Time



Differential Output Voltage Setup



Offset Voltage Setup

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844002 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

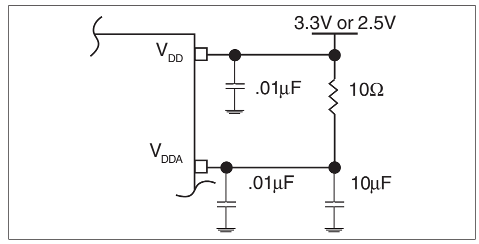


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS844002 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

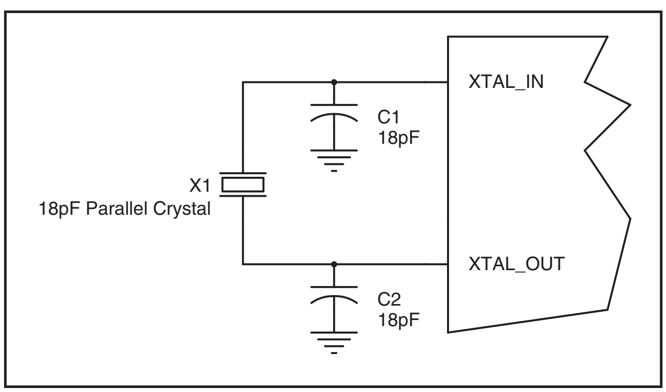


Figure 2. Crystal Input Interface

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

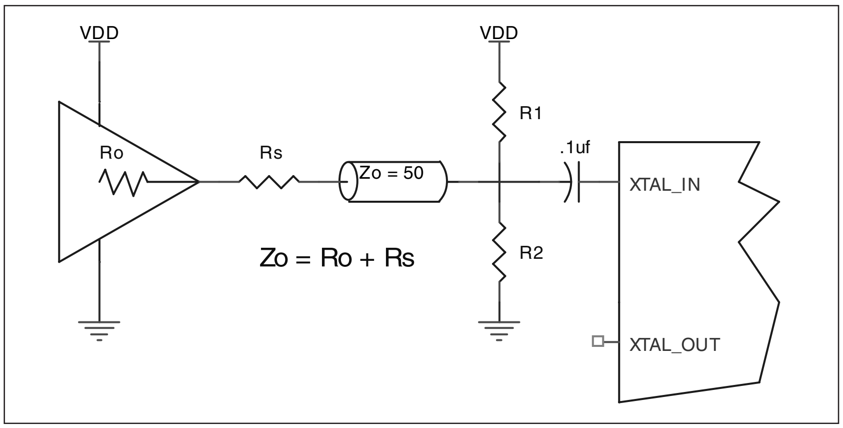


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS
All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVDS OUTPUTS
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

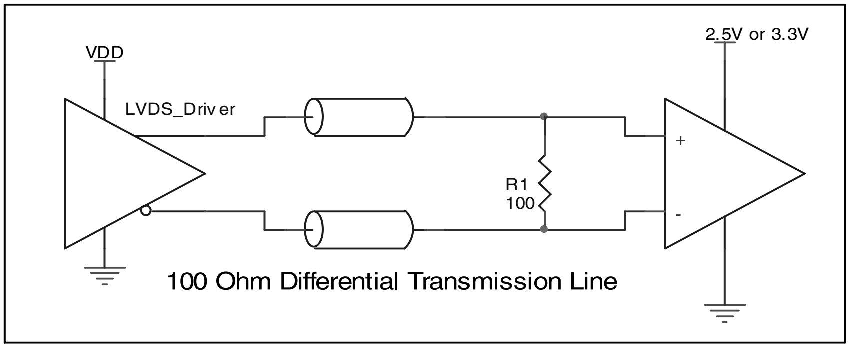


Figure 4. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844002. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS844002 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (105mA + 12mA) = **405.4mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 120mA = **415.8mW**

Total Power$_{_MAX}$ = 405.4mW + 415.8mW = **821.2mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

q_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.821W * 66.6°C/W = 124.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20-Lead TSSOP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS844002 is: 2914

Package Outline - G Suffix for 20 Lead TSSOP

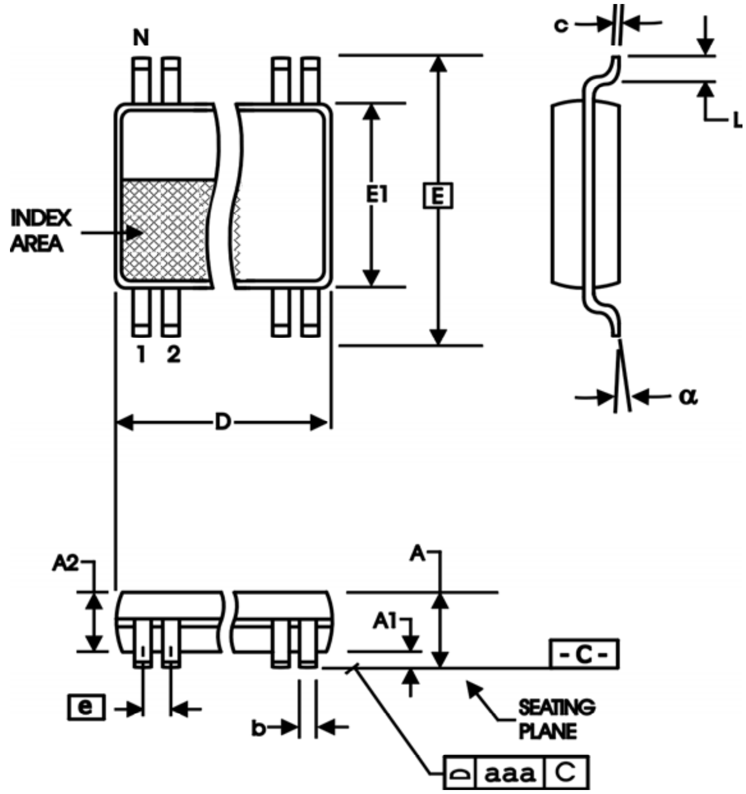


Table 8. Package Dimensions

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844002AG	ICS844002AG	20 Lead TSSOP	tube	0°C to 70°C
844002AGT	ICS844002AG	20 Lead TSSOP	2500 tape & reel	0°C to 70°C
844002AGLF	ICS844002AGL	20 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
844002AGLFT	ICS844002AGL	20 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A		6	Added Phase Noise Plots.	7/24/06
A		11	Power Consideraitons - corrected sentence after the Tj calculation.	1/19/07
A	T1	1 2	Pin Assignment - corrected Pin 16 from V_{DD} to nc. Pin Description Table - deleted number 16 from VDD row and added row Pin 16 as a "nc".	9/28/07
B	T3A, T3B T5A, T5B	3 5 7 8 8	Power Supply DC Characteristics Tables - changed VDDA max. from 3.465V to V_{DD}. AC Characteristics Tables - corrected NOTE 1. Corrected Output Rise/Fall Time Diagram. Updated Power Supply Filtering Technqiue paragraph text. Corrected Crystal Input Interface Diagram from 33/27p to 18/18p.	7/2/08

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