

Hi-Rel Thin Film Chip Resistors



TNPS ESCC high-reliability thin film chip resistors are the premium choice for design and manufacture of equipment, where matured technology and proven reliability are of utmost importance. They are regularly used in communication and research satellites and fit equally well into aircraft and military electronic systems.

Approval of the TNPS ESCC products is granted by the European Space Components Coordination and registered in the ESCC Qualified Parts List, REP005.

FEATURES

- High-reliability product
- ESA approved to ESCC 4001/029
- · Advanced thin film technology
- SnPb termination plating, minimum 6 % Pb

APPLICATIONS

- Aerospace
- Avionics
- Military

METRIC SIZE				
IMPERIAL	0603	0805	1206	
METRIC	RR1608M	RR2012M	RR3216M	

TECHNICAL SPECIFICATIONS					
DESCRIPTION	TNPS0603 ESCC	TNPS0805 ESCC	TNPS1206 ESCC		
Metric size	RR1608M	RR2012M	RR3216M		
Resistance range	10.0 Ω to 221 k Ω	10.0 Ω to 422 k Ω	10.0 Ω to 1.00 MΩ		
Resistance tolerance	± 1 %; ± 0.5 %; ± 0.1 %				
Temperature coefficient	± 50) ppm/K; ± 25 ppm/K; ± 15 pp	om/K		
Rated dissipation P70	0.1 W	0.125 W	0.25 W		
Operating voltage, Umax. ACRMS or DC	75 V 150 V		200 V		
Permissible film temperature, 9 _{F max.}		125 °C			
Operating temperature range		- 55 °C to 125 °C			
Max. resistance change at P_{70} , $ \Delta R $ max., after:					
1000 h	≤ (0.05 % <i>R</i> + 10 mΩ)				
2000 h	≤ (0.1 % <i>R</i> + 20 mΩ)				
Permissible voltage against ambient (insulation)	100 V	200 V	300 V		
Storage temperature range	- 55 °C to 125 °C				

Note

• These resistors do not feature a limited lifetime when operated within the permissible limits. However, resistance value drift increasing over operating time may result in exceeding a limit acceptable to the specific application, thereby establishing a functional lifetime.

TEMPERATURE COEFFICIENT AND RESISTANCE RANGE					
DESCRIPTION RESISTANCE RANGE					
TCR	TOLERANCE	TNPS0603 ESCC	TNPS0805 ESCC	TNPS1206 ESCC	
± 50 ppm/K	±1%	10.0 Ω to 221 k Ω	10.0 Ω to 422 k Ω	10.0 Ω to 1.00 M Ω	
± 25 ppm/K	± 0.5 %	10.0 Ω to 221 k Ω	10.0 Ω to 422 k Ω	10.0 Ω to 1.00 M Ω	
	± 0.1 %	10.0 Ω to 221 k Ω	10.0 Ω to 422 k Ω	10.0 Ω to 1.00 M Ω	
± 15 ppm/K	± 0.1 %	10.0 Ω to 221 k Ω	10.0 Ω to 422 k Ω	10.0 Ω to 1.00 $M\Omega$	

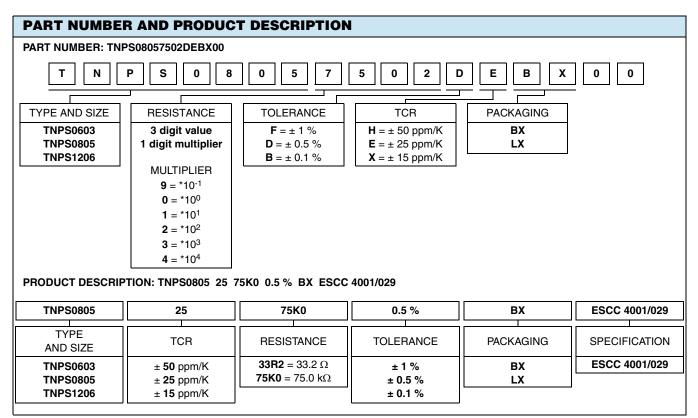
Notes

• The indicated combinations of TCR, tolerance and resistance range are a subset of those combinations approved to ESCC 4001/029

· According to ESCC 4001/029, resistance values are to be selected from the E96 series only

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Note

· Products can be ordered using either the PART NUMBER or the PRODUCT DESCRIPTION

Example of the component number and electrical character 400102902 7502D2	cteristics for a resistor: TNPS0805 25 75K0 0.5 % ESCC 4001/029
The elements used in the component number have the f	ollowing meaning:
4001029 02	Detail specification number, ESCC 4001/029 Type variant, used for identification of chip size: 01 0603 02 0805 03 1206
ne elements used in the electrical characteristics have	the following meaning:
7502 D 2	Resistance acc. IEC 60062, four-character code system Tolerance on rated resistance acc. IEC 60062 Temperature coefficient of resistance: 3 ± 50 ppm/K 2 ± 25 ppm/K 1

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PACKAGING							
ТҮРЕ	CODE	QUANTITY ⁽¹⁾	PACKAGING STYLE	WIDTH	PITCH	PACK. DIMENSIONS	
TURGASSA	вх	100 to 499	Antistatic blister tape acc. IEC 60286-3 ⁽²⁾	8 mm	2 mm	Box	
TNPS0603 TNPS0805	DA .	500 to 3000	Type II	8 mm	2 mm	Reel Ø 180 mm	
TNPS1206	LX	1 to 100	Matrix tray ⁽³⁾	-	4.2 mm x 4.2 mm	55 mm x 51 mm x 11 mm	

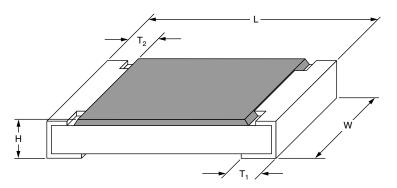
Notes

⁽¹⁾ Minimum order quantity is 100 pieces, except for samples for lot validation testing

⁽²⁾ Leader is extended to 500 mm cover tape, including 200 mm carrier tape with empty compartments

⁽³⁾ Matrix tray (waffle tray) packaging, code LX, is available only for samples for lot validation testing

DIMENSIONS

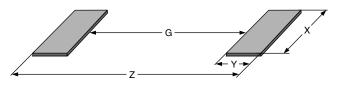


DIMENSIONS AND MASS						
ТҮРЕ	L (mm)	W (mm)	H (mm)	T ₁ , T ₂ (mm)	MASS (mg)	
TNPS0603	1.60 ± 0.10	0.85 ± 0.10	0.45 ± 0.10	0.30 ± 0.20	≤2	
TNPS0805	2.00 ± 0.15	1.25 ± 0.15	0.45 ± 0.10	0.40 ± 0.20	≤ 5	
TNPS1206	3.20 ± 0.15	1.60 ± 0.15	0.55 ± 0.10	0.50 ± 0.25	≤ 10	

Note

 Alphanumeric coding of the resistance value is applied, using the four-character code of IEC 60062 ⁽¹⁾, where the character R is used instead of the decimal point for values below 100 Ω

PATTERN STYLES FOR CHIP RESISTORS



RECOMMENDED SOLDER PAD DIMENSIONS

Recommended Solder FAD dimensions								
		WAVE SO	LDERING		REFLOW SOLDERING			
ТҮРЕ	G (mm)	Y (mm)	X (mm)	Z (mm)	G (mm)	Y (mm)	X (mm)	Z (mm)
TNPS0603	0.55	1.05	1.10	2.65	0.90	0.70	0.95	2.30
TNPS0805	0.80	1.20	1.55	3.20	1.10	0.85	1.40	2.80
TNPS1206	1.40	1.50	1.90	4.40	1.80	1.15	1.75	4.10

Note

• The given solder pad dimensions reflect the considerations for board design and assembly as outlined e.g. in standards IEC 61188-5-x, or in publication IPC-7351. They do not guarantee any supposed thermal properties, however, they will be found adequate for most general applications.

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DESCRIPTION

Production is strictly controlled and follows an extensive set instructions established for reproducibility. of Α homogeneous film of metal alloy is deposited on a high grade ceramic substrate (Al₂O₃) and conditioned to achieve the desired temperature coefficient. Specially designed inner contacts are deposited on both sides. A special laser is used to achieve the target value by smoothly fine trimming resistive layer without damaging the ceramics. A further conditioning is applied in order to stabilize the trimming result. The resistor elements are covered by a protective coating designed for electrical, mechanical and climatic protection. The terminations receive a final SnPb plating, controlled for a minimum lead contents of 6 %. The resistance value is stamped on the coating with a four-character code system according to IEC 60062 ⁽¹⁾. The result of the determined production is verified by an extensive testing procedure performed on 100 % of the individual chip resistors. Only accepted products are placed into a special matrix case packaging or into antistatic blister tape in accordance with IEC 60286-3 (1).

ASSEMBLY

The resistors are suitable for processing on automatic SMD assembly systems. They are suitable for automatic soldering using wave, reflow or vapour phase as shown in **IEC 61760-1** ⁽¹⁾. The encapsulation is resistant to all cleaning solvents commonly used in the electronics industry, including alcohols, esters and aqueous solutions. The suitability of conformal coatings, if applied, shall be qualified by appropriate means to ensure the long-term stability of the whole system. Solderability is specified for 2 years after production. The permitted storage time is 20 years.

APPROVALS

The resistors are approved to **ESCC 4001/029**. Conformity is indicated by the **ESCC Qualified Components** logo on the package label. Approval is granted by the European Space Components Coordination and registered in the ESCC Qualified Parts List, REP005.

The detail specification **ESCC 4001/029** has been established after successful completion of an **Evaluation Test Programme** according to **ESCC 2264000**.

SCREENING TESTS

These products are subjected to a screening test according to the ruling of the generic specification **ESCC 4001** and the detail specification **ESCC 4001/029**.

The production is succeeded by production test sequences for resistance, plating properties, solderability and dimensions. This sequence is followed by screening tests for overload, non-linearity, temperature coefficient, resistance at room temperature and a visual inspection. A Certificate of Conformity provides summary information by reporting the numbers of rejects for each test or inspection.

LOT VALIDATION TESTS

Execution of Lot Validation Tests according to the ruling of **ESCC 4001** is available as a separate order item. This is to be combined with the dedicated order line for the required amount of samples, using packaging code "LX".

The applicable scope of the Lot Validation Tests, graduated to Group 1, Group 2, and Group 3 is illustrated further below with the number of samples required for each level.

Deliverable item to the Lot Validation Tests is the test report together with the used samples, shipped in waffle tray package.



Waffle Tray

Note

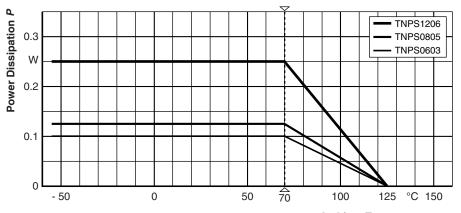
⁽¹⁾ The quoted IEC standards are also released as EN standards with the same number and identical contents

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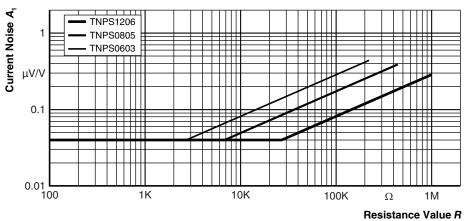


FUNCTIONAL PERFORMANCE



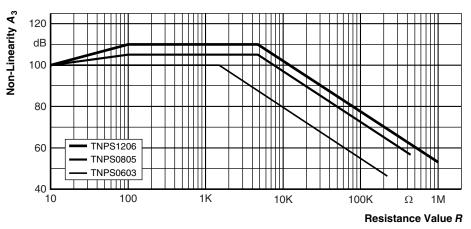
Ambient Temperature ϑ_{amb}





In accordance with IEC 60195





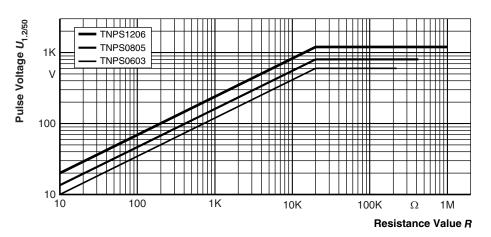
In accordance with IEC/TR 60440

Non-linearity - A₃

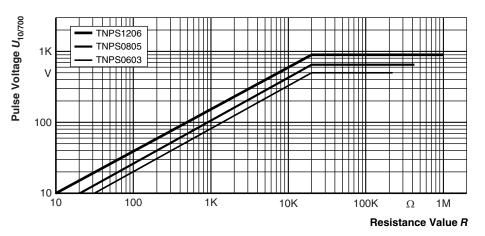
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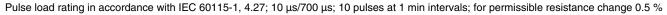


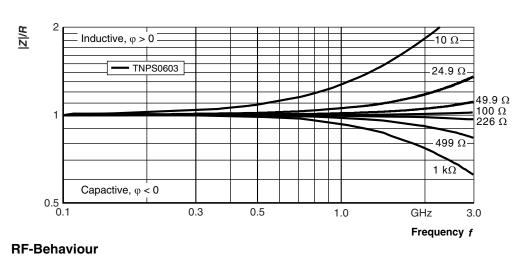


Pulse load rating in accordance with IEC 60115-1, 4.27; 1.2 µs/50 µs; 5 pulses at 12 s intervals; for permissible resistance change 0.5 %



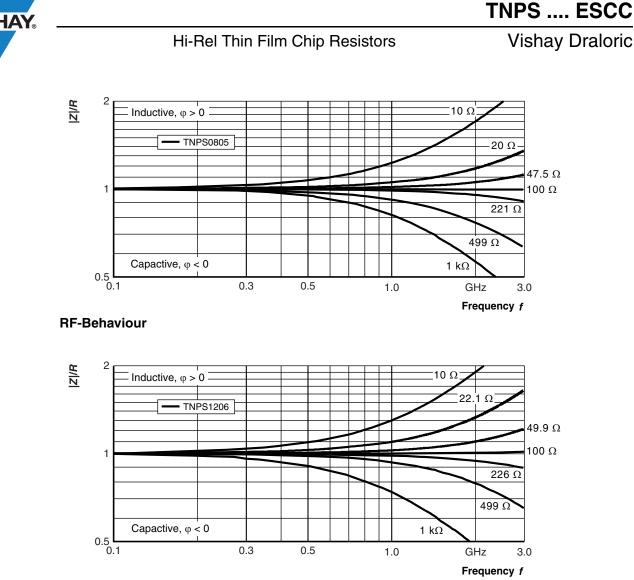
1.2/50 Pulse







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RF-Behaviour

TESTS AND REQUIREMENTS

All tests are carried out in accordance with the following specifications:

ESCC 4001, generic specification, issue 3 (2010)

ESCC 4001/029, detail specification, issue 2 (2010)

The components are approved within the ESCC system. For the full test schedule refer to the documents listed above.

The tests are carried out in accordance with the stated specifications.

Unless otherwise specified the following standard atmospheric conditions apply:

Temperature: 15 °C to 35 °C

Relative humidity: 45 % to 75 %

Air pressure: 86 kPa to 106 kPa (860 mbar to 1060 mbar)

The components are mounted for testing on printed-circuit boards in accordance with IEC 60115-1, 4.31, unless otherwise specified.



ESCC 4001	ESCC 4001/029			REQUIREMENTS
PARAGRAPH	PARAGRAPH	TEST	PROCEDURE	PERMISSIBLE CHANGE (AR)
			Stability for product types:	
			TNPS0603	10.0 Ω to 221 k Ω
			TNPS0805	10.0 Ω to 422 k Ω
			TNPS1206	10.0 Ω to 1.00 M Ω
	N CONTROL (CHART F			
8.3.2	2.5.1 (ESCC 23500)	Resistance	(22 ± 3) °C	± 1 % <i>R</i> ; ± 0.5 % <i>R</i> ; ± 0.1 % <i>R</i>
4.5	(E300 23500)	Plating - Thickness - Pb contents	X-ray fluorescence analysis	SnPb layer ≥ 3 μm ≥ 6 % Pb
8.14	(IEC 60068-2-20, Ta)	Solderability	Solder bath method; SnPb40; non-activated flux; (235 ± 5) °C; (2 ± 0.5) s	Good tinning (≥ 95 % covered); No visible damage; ± (0.02 % <i>R</i> + 10 mΩ)
8.6	1.6	Dimension check	-	-
SCREENING	TESTS (CHART F3)			
8.1	2.1.1.1 1.5	Overload	$U = \sqrt{k \times P_{70} \times R}$ 1 ms Style k 0603 30 0805 32 1206 32	± (0.05 % <i>R</i> + 10 mΩ)
-	(IEC/TR 60440) 2.5.1	Non-linearity (3 rd harmonic attenuation)	-	$A_3 \ge A_{3 \text{ min.}}$ according to diagram non-linearity
8.3.3	2.5.2	Resistance at high and low temperature	- (55 ± 3) °C (125 ± 3) °C	± 50 ppm/K; ± 25 ppm/K; ± 15 ppm/
8.3.2	2.5.1	Resistance	(22 ± 3) °C	± 1 % <i>R</i> ; ± 0.5 % <i>R</i> ; ± 0.1 % <i>R</i>
8.6	- ON AND PERIODIC TE	External visual inspection	-	-
8.8	(IEC 60068-2-14, Na); 1.5	Rapid change of temperature	- 55 °C; 30 min; 125 °C; 30 min; 10 cycles	± (0.1 % <i>R</i> + 10 mΩ)
8.11.2		Robustness of terminations:		
8.11.2.1	(IEC 60115-1, 4.32)	Adhesion (shear test)	5 N; 10 s	No visible damage ± (0.05 % R + 10 m Ω)
	2.3	Bend strength of the end face plating (substrate bending test)	Depth 2 mm; 5 s; 10 times	No visible damage ± (0.05 % R + 10 m Ω)
8.12	(IEC 60068-2-20, Tb) 2.4	Resistance to soldering heat	Solder bath method; (260 ± 5) °C; (10 ± 1) s	No visible damage ± (0.02 % R + 10 m Ω)
8.10	1.5	Climatic sequence:		± (0.1 % <i>R</i> + 20 mΩ) <i>R</i> _{ins} ≥ 1 GΩ
8.10.2	(IEC 60068-2-2, Ba)	Dry heat	125 °C; 16 h	
8.10.3	(IEC 60068-2-30, Db)	Damp heat, cyclic	55 °C; ≥ 90 % RH;	
8.10.4	(IEC 60068-2-1, Aa)	Cold	24 h; 1 cycle - 55 °C; 1 h off; 0.75 h on	4
8.10.5	(IEC 60068-2-13, M)	Low air pressure	$\frac{2 \text{ kPa; } (25 \pm 10) \text{ °C; 1 h;}}{U = \sqrt{P_{70} \times R} \le U_{\text{max.}}}$	
8.10.6	(IEC 60068-2-30, Db)	Damp heat, cyclic	55 °C; ≥ 90 % RH; 24 h; 5 cycles	
8.10.7	-	DC load	$U = \sqrt{P_{70} \times R} \le U_{\text{max.}};$ 1 min	
8.3.1.2.2	(IEC 60115-1, 4.6.1.4)	Insulation resistance	Test jig for flat chips U = 100 V; 1 min	$R_{ins} \ge 1 \ G\Omega$

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ESCC 4001 PARAGRAPH	ESCC 4001/029 PARAGRAPH	TEST	PROCEDURE	REQUIREMENTS PERMISSIBLE CHANGE (∆ <i>R</i>)
	I		Stability for product types:	
			TNPS0603	10.0 Ω to 221 k Ω
			TNPS0805	10.0 Ω to 422 k Ω
			TNPS1206	10.0 Ω to 1.00 MΩ
8.3.1.3.2	(IEC 60115-1, 4.7) 1.5	Voltage proof	Test jig for flat chips $U_{\text{RMS}} = 1.4 \text{ x } U_{\text{ins RMS}};$ $f = (50 \pm 10) \text{ Hz}; 5 \text{ s}$	No breakdown; no flashover
8.13	2.7 1.5	Endurance at operating life	$U = \sqrt{P_{70} \times R} \le U_{\text{max}};$ 70 °C; 1000 h; 1.5 h on; 0.5 h off 70 °C; 1000 h 70 °C; 2000 h	± (0.05 % <i>R</i> + 10 mΩ) ± (0.1 % <i>R</i> + 20 mΩ) <i>R</i> _{ins} ≥ 1 GΩ
8.14	(IEC 60068-2-20, Ta)	Solderability	y Solder bath method; SnPb40; non-activated flux (235 ± 5) °C; (2 ± 0.5) s Good tinning (\ge no visible $\pm (0.02 \%)$	
8.15	(ESCC 24800)	Permanence of marking	a) Ethyl alcohol b) Isopropyl alcohol 25 °C; 3 x 1 min hard toothbrush; 3 x 10 strokes	Marking legible; no visible damage

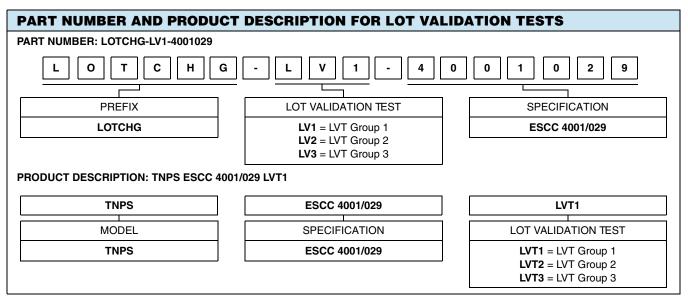
LOT VALIDATION TESTS

Execution of Lot Validation Tests is available as a separate order item. Deliverable item to the Lot Validation Tests is the test report together with the used samples. The samples need to be ordered as a separate item.

GROUP 1	ENVIRON	IENTAL AND	MECHANICAL			48 samples	
	Robustness	of terminatio	ns: Shear (adhesion)	ESCC 4001, 8.11.2.1		(6 samples)	
	Robustness	of terminatio	ns: Substrate bending	ESCC 4001, 8.11.2.2			
	Resistance	to soldering h	eat	ESCC 4001, 8.12		(6 samples)	
	Climatic sequence			ESCC 4001, 8.10)	(12 samples)	
	GROUP 2	ENDURAN	CE	36 sai	nples		
		Endurance	at operating life, 2000 h	ESCC 4001, 8.13			
		GROUP 3	ELECTRICAL AND ASSEMBLY		21 samples		
			Insulation resistance	ESCC 4001, 8.3.1.2.2	(15 samples)		
			Voltage proof	ESCC 4001, 8.3.1.3.2			
			Solderability	ESCC 4001, 8.14	(6 samples)		
			Permanence of marking	ESCC 4001, 8.15			

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Note

• Execution of Lot Validation Tests can be ordered using either the PART NUMBER or the PRODUCT DESCRIPTION

ORDER	ORDER TEXT EXAMPLE						
	f a Lot Validation T he example below:	Fests shall be combined with a dedicated order line for the requ	ired amount of samples, using packaging code				
POS	QTY	ITEM					
0030	950	TNPS0805 25 75K0 0.5 % BX ESCC 4001/029 400102902 7502D2	{Quantity for consumption}				
0031	36	TNPS0805 25 75K0 0.5 % LX ESCC 4001/029 400102902 7502D2	{Quantity for LVT samples}				
0032	1	TNPS ESCC 4001/029 LVT2	{Lot Validation Test, Group 2}				



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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