Comlinear
A National Semiconductor Company

Ultra Low Noise Wideband Op Amp

CLC425

APPLICATIONS:

- instrumentation sense amplifiers
- ultrasound pre-amps
- magnetic tape & disk pre-amps
- photo-diode transimpedance amplifiers
- wide band active filters
- low noise figure RF amplifiers
- professional audio systems
- low-noise loop filters for PLLs

DESCRIPTION

The CLC425 combines a wide bandwidth (**1.9GHz GBW**) with very low input noise (**1.05nV/√Hz, 1.6pA/√Hz**) and low dc errors (**100μV V_{OS}, 2μV/°C drift**) to provide a very precise, wide dynamic-range op amp offering closed-loop gains of ≥10.

Singularly suited for very wideband high-gain operation, the CLC425 employs a traditional voltage-feedback topology providing all the benefits of balanced inputs, such as low offsets and drifts, as well as a 96dB open-loop gain, a 100dB CMRR and a 95dB PSRR.

The CLC425 also offers great flexibility with its externally adjustable supply current, allowing designers to easily choose the optimum set of power, bandwidth, noise and distortion performance. Operating from ±5V power supplies, the CLC425 defaults to a 15mA quiescent current, or by adding one external resistor, the supply current can be adjusted to less than 5mA.

The CLC425's combination of ultra-low noise, wide gain-bandwidth, high slew rate and low dc errors will enable applications in areas such as medical diagnostic ultrasound, magnetic tape & disk storage, communications and opto-electronics to achieve maximum high-frequency signal-to-noise ratios.

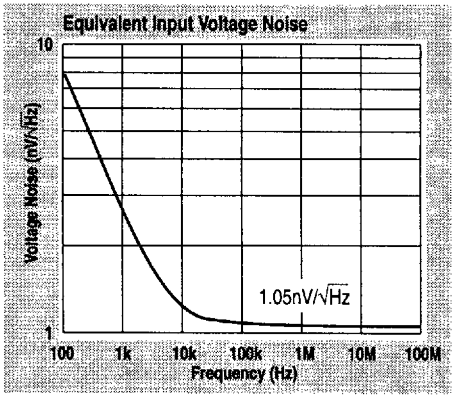
The CLC425 is available in the following versions.

CLC425AJP	-40°C to +85°C	8-pin PDIP
CLC425AJE	-40°C to +85°C	8-pin SOIC
CLC425AIB	-40°C to +85°C	8-pin CerDIP
CLC425A8B	-55°C to +125°C	8-pin CerDIP, MIL-STD-883 Level B
CLC425ALC	-55°C to +125°C	dice
CLC425AMC	-55°C to +125°C	dice, MIL-STD-883 Level B

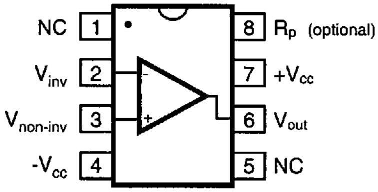
Contact factory for other packages; DESC SMD number 5962-93259.

FEATURES:

- 1.9GHz gain-bandwidth product
- 1.05nV/√Hz input voltage noise
- 0.8pA/√Hz @ Icc ≤ 5mA
- 100μV input offset voltage, 2μV/°C drift
- 350V/μs slew rate
- 15mA to 5mA adjustable supply current
- gain range ±10 to ±1,000V/V
- evaluation boards and simulation macromodel
- 0.9dB NF @ R_S = 700Ω

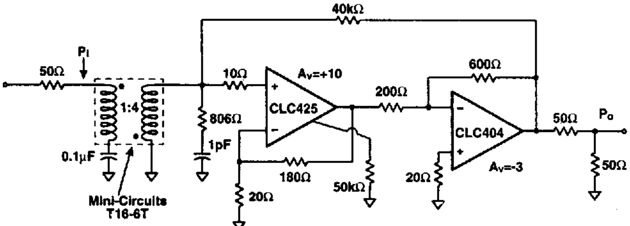


Pinout
DIP & SOIC



TYPICAL APPLICATION

Very Low Noise Figure Amplifier



Gain = $\frac{P_o}{P_I}$ = 35.6dB

CLC425 Electrical Characteristics ($V_{cc} = \pm5V$; $A_V = +20$; $R_f = 499\Omega$; $R_g = 26.1\Omega$; $R_L = 100\Omega$; unless noted)

PARAMETERS	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC425 AJ/AI	+25˚C	-40˚C	+25˚C	+85˚C		
Ambient Temperature	CLC425 A8/AM/AL	+25˚C	-55˚C	+25˚C	+125˚C		
FREQUENCY DOMAIN RESPONSE							
gain bandwidth product	$V_{out} < 0.4V_{pp}$	1.9	1.5	1.5	1.0	GHz	GBW
†-3dB bandwidth	$V_{out} < 0.4V_{pp}$	95	75	75	50	MHz	SSBW
	$V_{out} < 5.0V_{pp}$	40	30	30	20	MHz	LSBW
gain flatness	$V_{out} < 0.4V_{pp}$						
†peaking	DC to 30MHz	0.3	0.7	0.5	0.7	dB	GFP
†rolloff	DC to 30MHz	0.1	0.7	0.5	0.7	dB	GFR
linear phase deviation	DC to 30MHz	0.7	1.5	1.5	2.5	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	0.4V step	3.7	4.7	4.7	7.0	ns	TRS
settling time to 0.2%	2V step	22	30	30	40	ns	TSS
overshoot	0.4V step	5	12	10	12	%	OS
slew rate	2V step	350	250	250	200	V/µs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	$1V_{pp}$, 10MHz	- 53	48	48	46	dBc	HD2
†3rd harmonic distortion	$1V_{pp}$, 10MHz	- 75	65	65	60	dBc	HD3
3rd order intermodulation intercept	10MHz	35				dBm	IMD
equivalent noise input							
voltage	1MHz to 100MHz	1.05	1.25	1.25	1.8	nV/√Hz	VN
current	1MHz to 100MHz	1.6	4.0	2.5	2.5	pA/√Hz	ICN
noise figure	$R_s = 700\Omega$	0.9				dB	NF
STATIC DC PERFORMANCE							
open-loop gain	DC	96	77	86	86	dB	AOL
*input offset voltage		± 100	± 1000	± 800	± 1000	µV	VIO
average drift		± 2	8	—	4	µV/°C	DVIO
*input bias current		12	40	20	20	µA	IB
average drift		- 100	- 250	—	- 120	nA/°C	DIB
input offset current		± 0.2	3.4	2.0	2.0	µA	IIO
average drift		± 3	± 50	—	± 25	nA/°C	DIIO
†power supply rejection ratio	DC	95	82	88	86	dB	PSRR
♠common mode rejection ratio	DC	100	88	92	90	dB	CMRR
*supply current	$R_L = \infty$	15	18	16	16	mA	ICC
MISCELLANEOUS PERFORMANCE							
input resistance	common-mode	2	0.6	1.6	1.6	MΩ	RINC
	differential-mode	6	1	3	3	kΩ	RIND
input capacitance	common-mode	2.5	3	3	3	pF	CINC
	differential-mode	14				pF	CIND
output resistance	closed loop	5	50	10	10	mΩ	ROUT
output voltage range	$R_L = \infty$	± 3.8	± 3.5	± 3.7	± 3.7	V	VO
	$R_L = 100\Omega$	± 3.4	± 2.8	± 3.2	± 3.2	V	VOL
input voltage range	common mode	± 3.8	± 3.4	± 3.5	± 3.5	V	CMIR
output current	source -55°C/-40°C	90	60/70	70	70	mA	IOP
	sink -55°C/-40°C	90	40/55	55	55	mA	ION

V_{cc}	±7V
I_{out} short circuit protected to ground, however maximum reliabiliy is obtained if I_{out} does not exceed...	150mA
common-mode input voltage	$\pm V_{cc}$
differential input current diode protected	±25mA
maximum junction temperature	+175˚C
operating temperature range	
AJ/AI	-40°C to +85°C
A8/AM/AL:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Recommended gain range ±10 to ±1,000V/V

Notes:

* AJ,AI : 100% tested at +25°C, sample at +85°C.
† AJ : Sample tested at +25°C.
† AI : 100% tested at +25°C.
* A8 : 100% tested at +25°C, -55°C, +125°C.
† A8 : 100% tested at +25°C, sample at -55°C, +125°C
* AL, AM : 100% wafer probed +25°C to +25°C min/max specs.
♠ SMD : Sample tested at +25°C, -55°C and +125°C.

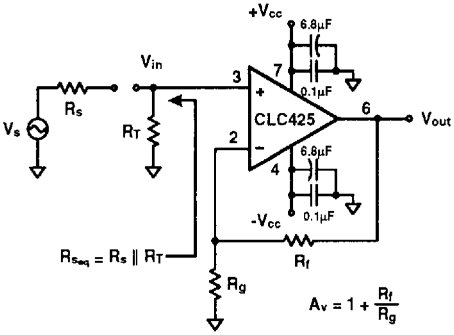


Figure 1: Non-inverting Amplifier Configuration

Introduction

The CLC425 is a very wide gain-bandwidth, ultra-low noise voltage feedback operational amplifier which enables application areas such as medical diagnostic ultrasound, magnetic tape & disk storage and fiber-optics to achieve maximum high-frequency signal-to-noise ratios. The set of characteristic plots located in the "Typical Performance" section illustrates many of the performance trade-offs. The following discussion will enable the proper selection of external components in order to achieve optimum device performance.

Bias Current Cancellation

In order to cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain-setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance ($R_{s_{eq}}$) as defined in Figure 1. Combining this constraint with the non-inverting gain equation also seen in Figure 1, allows both R_f and R_g to be determined explicitly from the following equations: $R_f = A_v R_{s_{eq}}$ and $R_g = R_f/(A_v-1)$. When driven from a 0Ω source, such as that from the output of an op amp, the non-inverting input of the CLC425 should be isolated with at least a 25Ω series resistor.

As seen in Figure 2, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input ($R_f \| (R_g + R_s)$). R_b is recommended to be no less than 25Ω for best CLC425 performance. The additional noise contribution of R_b can be minimized through the use of a shunt capacitor.

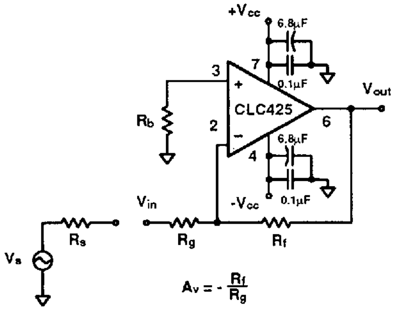
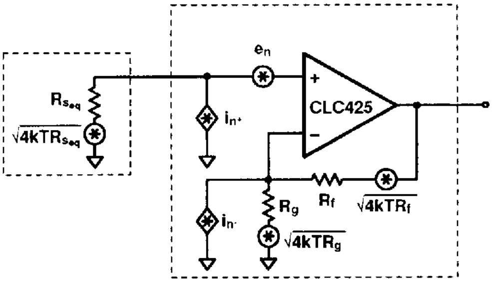


Figure 2: Inverting Amplifier Configuration

Total Input Noise vs. Source Resistance

In order to determine maximum signal-to-noise ratios from the CLC425, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary.

Figure 3 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_{n+} = i_{n-}$) sources, there also exists thermal voltage noise ($e_t = \sqrt{4kTR}$) associated with each of the external resistors. Equation 1 provides the general form for total equivalent input voltage noise density (e_{ni}). Equation 2 is a simplification of Equation 1 that assumes $R_f \| R_g = R_{s_{eq}}$ for bias current cancellation. Figure 4 illustrates the equivalent noise model using this assumption. Figure 5 is a plot of e_{ni} against equivalent source resistance ($R_{s_{eq}}$) with all of the contributing voltage noise sources of Equation 2 shown. This plot gives the expected e_{ni} for a given $R_{s_{eq}}$ which assumes $R_f \| R_g = R_{s_{eq}}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is $e_{ni} * A_v$.



$4kT = 16.4e-21$ Joules @ 25°C

Figure 3: Non-inverting Amplifer Noise Model

$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+}R_{s_{eq}}\right)^2 + 4kTR_{s_{eq}} + \left(i_{n-}\left(R_f \| R_g\right)\right)^2 + 4kT\left(R_f \| R_g\right)}$$

Equation 1: General Noise Equation

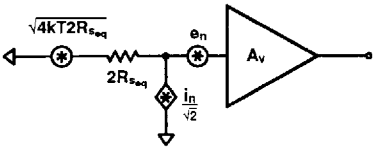


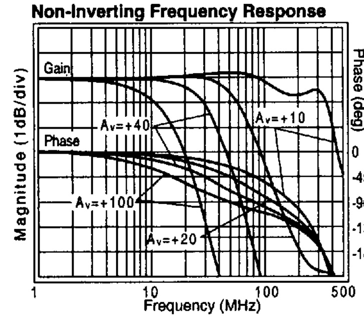
Figure 4: Noise Model with $R_f \| R_g = R_{s_{eq}}$

$$e_{ni} = \sqrt{e_n^2 + 2\left(i_n R_{s_{eq}}\right)^2 + 4kT\left(2R_{s_{eq}}\right)}$$

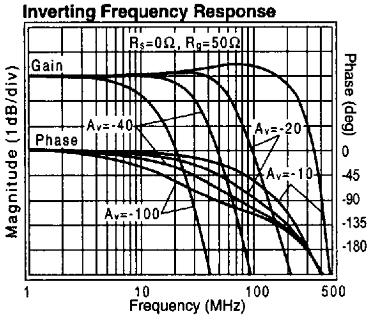
Equation 2: Noise Equation with $R_f \| R_g = R_{s_{eq}}$

CLC425 Typical Performance (T_A=25°C, V_{cc}=±5V, R_f=26.1Ω, R_f=499Ω, R_L=100Ω, unless noted)

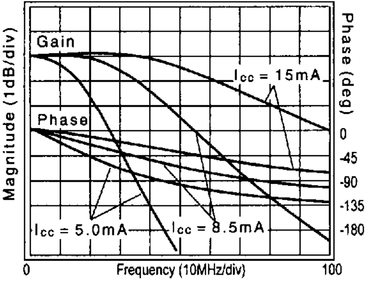
Non-Inverting Frequency Response



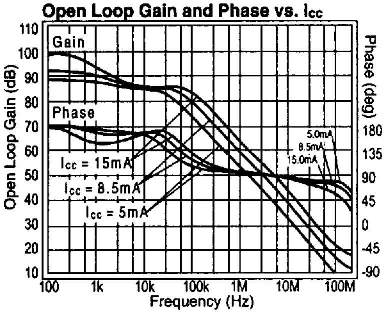
Inverting Frequency Response



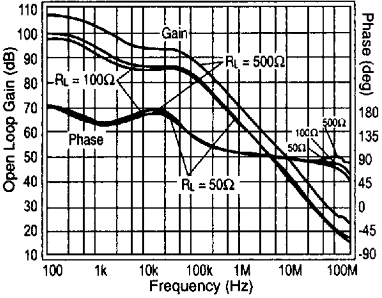
Frequency Response vs. I_{cc} (A_v=+20)



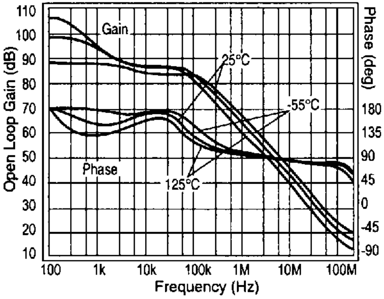
Open Loop Gain and Phase vs. I_{cc}



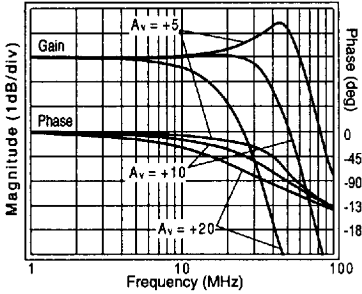
Open Loop Gain and Phase vs. R_L



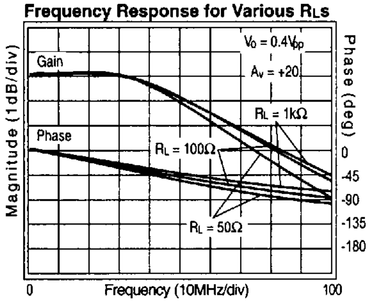
Open Loop Gain and Phase vs. Temp



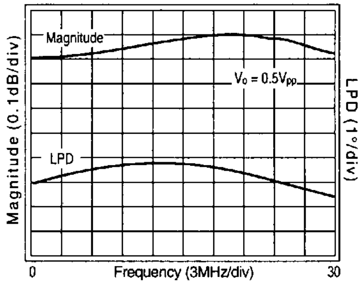
Non-Inverting Response (I_{cc}=5.0mA)



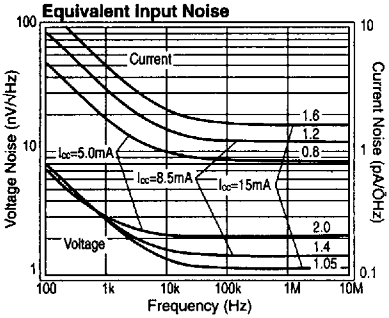
Frequency Response for Various R_Ls



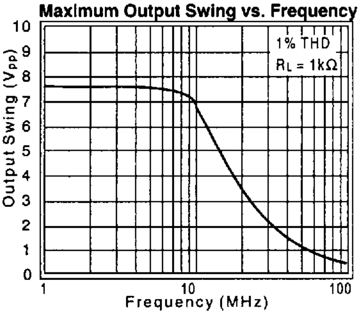
Gain Flatness & Linear Phase Deviation



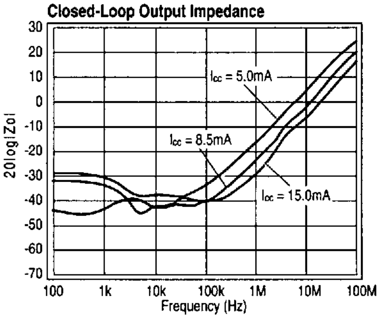
Equivalent Input Noise



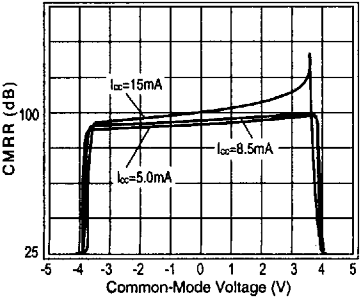
Maximum Output Swing vs. Frequency



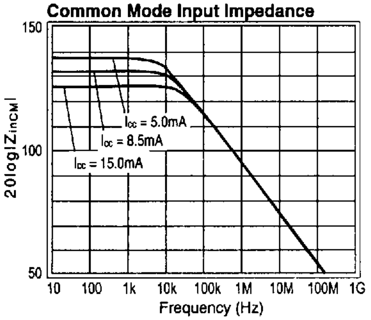
Closed-Loop Output Impedance



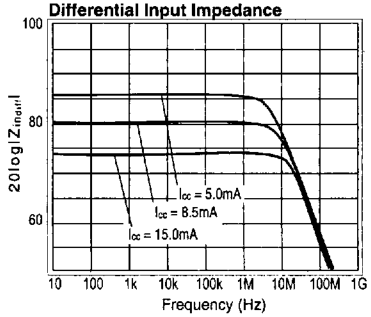
CMRR vs Common-Mode Input Voltage



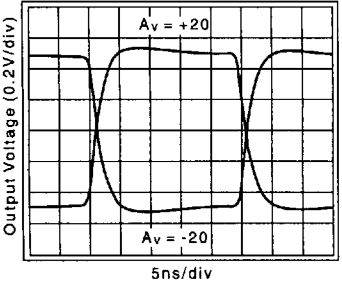
Common Mode Input Impedance

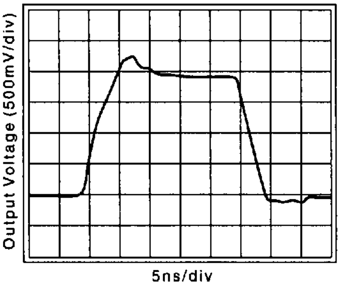


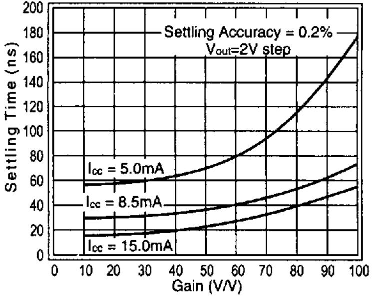
Differential Input Impedance

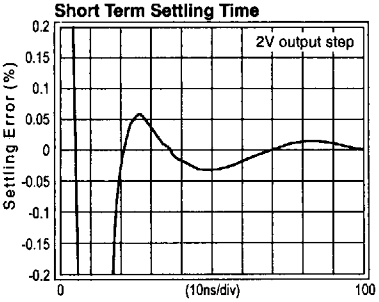


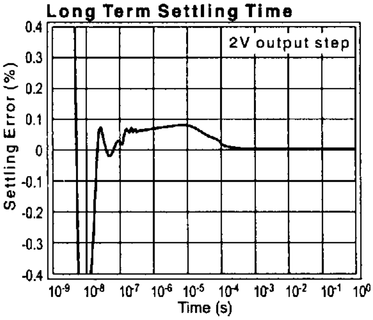
CLC425 Typical Performance (T_A=25°C, V_{cc}=±5V, R_f=26.1Ω, R_f=499Ω, R_L=100Ω, unless noted)

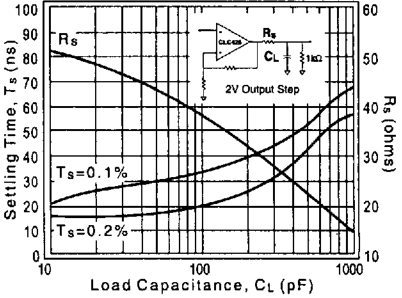

Pulse Response (V_o=1V_{pp})

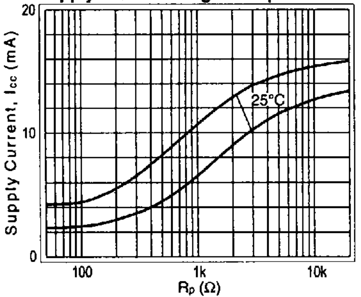

Large Signal Pulse Response (V_o=2V_{pp})

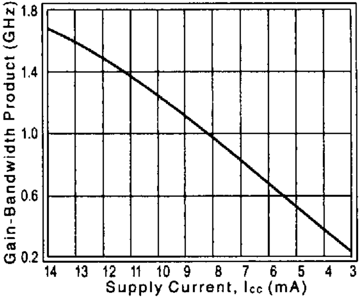

Settling Time vs. Gain

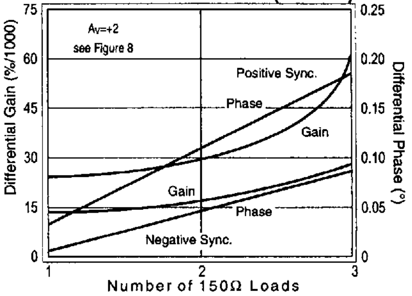

Short Term Settling Time

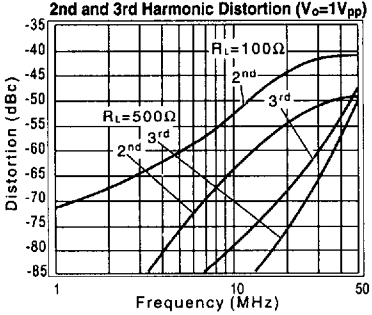

Long Term Settling Time

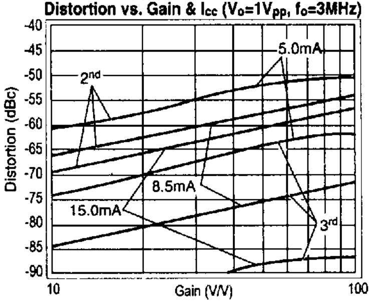

Settling Time vs. C_L and R_s

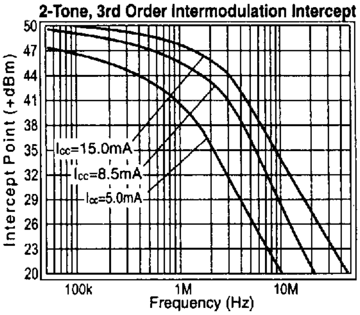

Supply Current Range vs. Rp

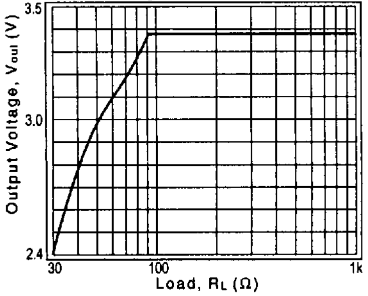

Gain-Bandwidth Product vs I_{cc}

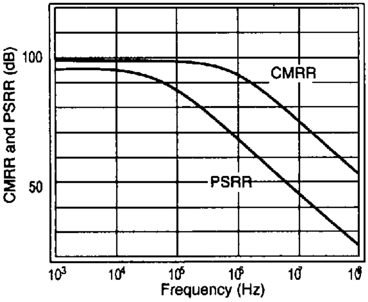

Differential Gain and Phase (4.43MHz)

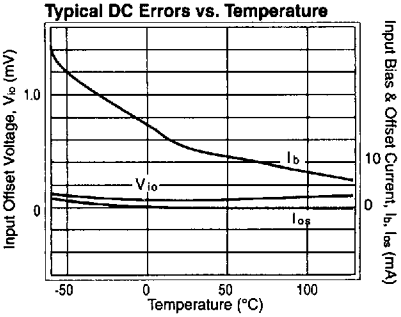

2nd and 3rd Harmonic Distortion (V_o=1V_{pp})


Distortion vs. Gain & I_{cc} (V_o=1V_{pp}, f_o=3MHz)


2-Tone, 3rd Order Intermodulation Intercept


Output Voltage vs Load


CMRR and PSRR


Typical DC Errors vs. Temperature

As seen in Figure 5, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 33.5Ω. Between 33.5Ω and 6.43kΩ, e_{ni} is dominated by the thermal noise ($e_t=\sqrt{4kTR_{seq}}$) of the external resistors. Above 6.43kΩ, e_{ni} is dominated by the amplifier's current noise ($\sqrt{2}i_nR_{seq}$). The point at which the CLC425's voltage noise and current noise contribute equally occurs for R_{seq}=464Ω (i.e. $e_n/\sqrt{2}i_n$). As an example, configured with a gain of +20V/V giving a -3dB of 90MHz and driven from an R_{seq}=25Ω, the CLC425 produces a total equivalent input noise voltage ($e_{ni}*\sqrt{1.57*90\text{MHz}}$) of 16.5μV$_{rms}$.

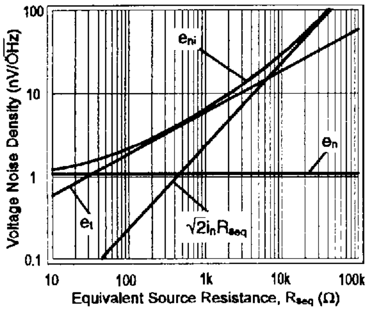


Figure 5: Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then $R_f||R_g$ does not need to equal R_{seq}. In this case, according to Equation 1, $R_f||R_g$ should be as low as possible in order to minimize noise. Results similar to Equation 1 are obtained for the inverting configuration of Figure 2 if R_{seq} is replaced by R_b and R_g is replaced by R_g+R_s. With these substitutions, Equation 1 will yield an e_{ni} refered to the non-inverting input. Refering e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains.

Noise Figure

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left(\frac{S_i/N_i}{S_o/N_o}\right) = 10LOG\left(\frac{e_{ni}^2}{e_t^2}\right)$$

The Noise Figure formula is shown in Equation 3. The addition of a terminating resistor R_T, reduces the external thermal noise but increases the resulting NF. The NF is increased because R_T reduces the input signal amplitude thus reducing the input SNR.

$$NF = 10LOG\left(\frac{e_n^2 + i_n^2\left(R_{seq} + \left(R_f||R_g\right)^2\right) + 4kTR_{seq} + 4kT\left(R_f||R_g\right)}{4kTR_{seq}}\right)$$

R_{seq} = R_s for Unterminated Systems
R_{seq} = R_s II R_T for Terminated Systems

Equation 3: Noise Figure Equation

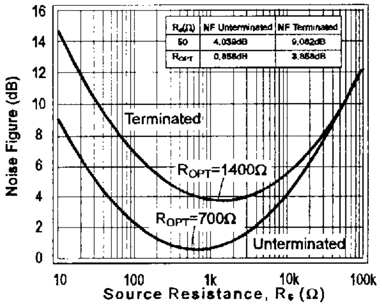
The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize noise figure, the following steps are recommended:

- Minimize $R_f||R_g$
- Choose the optimum R_s (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \cong (e_n/i_n)$$

Figure 6 is a plot of NF vs R_s with $R_f||R_g$ = 9.09 (A_v = +10). The NF curves for both Unterminated and Terminated systems are shown. The Terminated curve assumes R_s = R_T. The table indicates the NF for various source resistances including R_s = R_{OPT}.



R_s(Ω)	NF Unterminated	NF Terminated
50	4.039dB	9.062dB
R_{OPT}	0.858dB	3.858dB

Figure 6: Noise Figure vs Source Resistance

Supply Current Adjustment

The CLC425's supply current can be externally adjusted downward from its nominal value by adding an optional resistor (R_p) between pin 8 and the negative supply as shown in Figure 7. Several of the plots found within the plot pages demonstrate the CLC425's behavior at different supply currents. The plot labeled "I_{cc} vs. R_p" provides the means for selecting R_p and shows the result of standard IC process variation which is bounded by the 25°C curve.

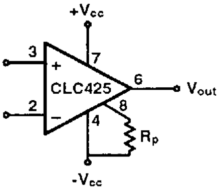


Figure 7: External Supply Current Adjustment

Non-Inverting Gains Less Than 10V/V

Using the CLC425 at lower non-inverting gains requires external compensation such as the shunt compensation as shown in Figure 8. The quiescent supply current must also be reduced to 5mA with R_p for stability. The compensation capacitors are chosen to reduce frequency response peaking to less than 1dB. The plot in the "Typical Performance" section labeled "Differential Gain and Phase" shows the video performance of the CLC425 with this compensation circuitry.

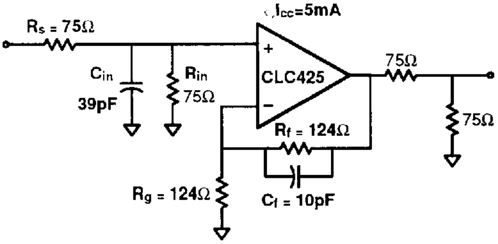


Figure 8: External Shunt Compensation

Inverting Gains Less Than 10V/V

The lag compensation of Figure 9 will achieve stability for lower gains. Placing the network between the two input terminals does not affect the closed-loop nor noise gain, but is best used for the invering configuration because of its affect on the non-inverting input impedance.

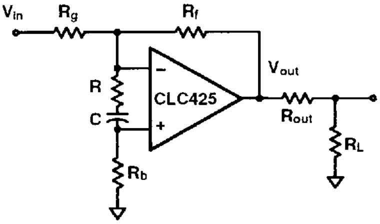


Figure 9: External Lag Compensation

Single-Supply Operation

The CLC425 can be operated with single power supply as shown iin Figure 10. Both the input and output are capacitively coupled to set the dc operating point.

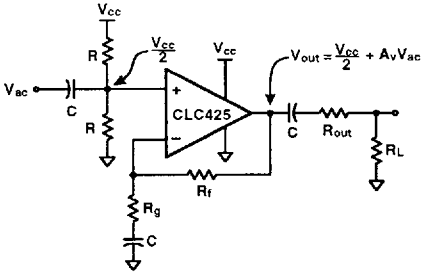


Figure 10: Single Supply Operation

Low Noise Transimpedance Amplifier

The circuit of Figure 11 implements a low-noise transimpedance amplifier commonly used with photo-diodes. The transimpedance gain is set by R_f. The simulated frequency response is shown in Figure 12 and shows the influence C_f has over gain flatness. Equation 4 provides the total input current noise density (i_{ni}) equation for the basic transimpedance configuration and is plotted against feedback resistance (R_f) showing all contributing noise sources in Figure 13. This plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_f). The total equivalent output voltage noise density (e_{no}) is $i_{ni}*R_f$.

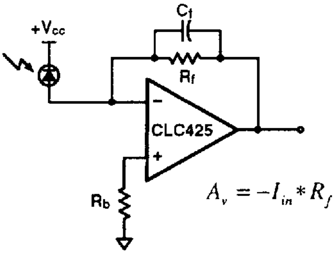


Figure 11: Transimpedance Amplifier Configuration

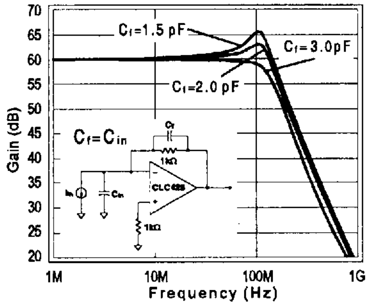


Figure 12: Transimpedance Amplifier Frequency Response

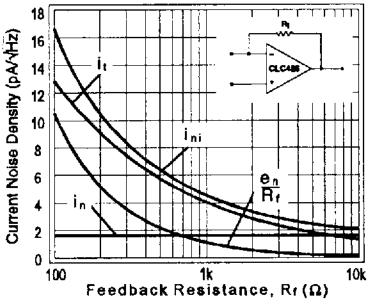


Figure 13: Current Noise Density vs. Feedback Resistance

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}}$$

Equation 4: Total Equivalent Input Refered Current Noise

Very Low Noise Figure Amplifier

The circuit of Figure 14 implements a very low Noise Figure amplifier using a step-up transformer combined with a CLC425 and a CLC404. The circuit is configured with a gain of 35.6dB. The circuit achieves measured Noise Figures of less than 2.5dB in the 10-40MHz region. 3rd order intercepts exceed +30dBm for frequencies less than 40MHz and gain flatness of 0.5dB is measured in the 1-50MHz pass bands. Application Note OA-14 provides greater detail on these low Noise Figure techniques.

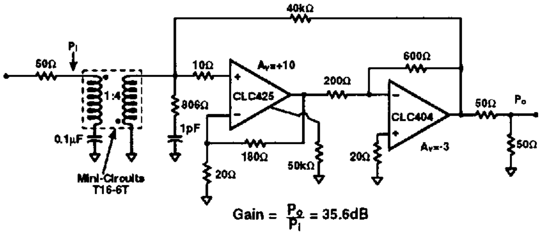
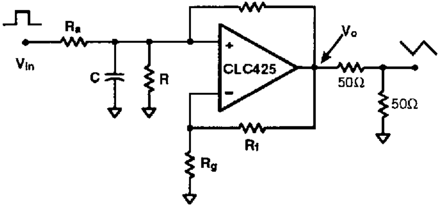


Figure 14: Very Low Noise Figure Amplifier

Low Noise Integrator

The CLC425 implements a deBoo integrator shown in Figure 15. Integration linearity is maintained through positive feedback. The CLC425's low input offset voltage and matched inputs allowing bias current cancellation provide for very precise integration. Stability is maintained through the constraint on the circuit elements.

$$V_o \cong V_{in}\frac{K_o}{sR_aC}; \qquad K_o = 1 + \frac{R_f}{R_g}$$



$$\frac{R_b}{R_a \| R} \geq \frac{R_f}{R_g}, \quad R \gg R_a$$

Figure 15: Low Noise Integrator

High-Gain Sallen-Key Active Filters

The CLC425 is well suited for high-gain Sallen-Key type of active filters. Figure 16 shows the 2nd order Sallen-Key low pass filter topology. Using component predistortion methods as discussed in OA-21 enables the proper selection of components for these high-frequency filters.

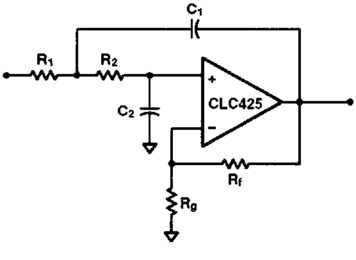
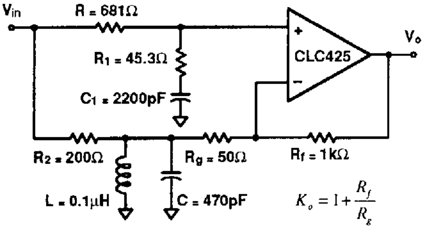


Figure 16: Sallen-Key Active Filter Topology

Low Noise Magnetic Media Equalizer

The CLC425 implements a high-performance low-noise equalizer for such applications as magnetic tape channels as shown in Figure 17. The circuit combines an integrator with a bandpass filter to produce the low-noise equalization. The circuit's simulated frequency response is illustrated in Figure 18.



$$\frac{V_o}{V_{in}} = K_o\left(\frac{sC_1R_1 + 1}{sC_1(R_1 + R) + 1} - \left(\frac{R_f}{R_f + R_g}\right)\frac{sLR_g}{s^2LCR_2R_g + sL(R_2 + R_g) + R_2R_g}\right)$$

Figure 17: Low Noise Magnetic Media Equalizer

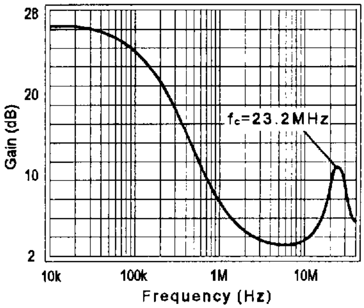


Figure 18: Equalizer Frequency Response

Low-Noise Phase-Locked Loop Filter

The CLC425 is extremely useful as a Phase-Locked Loop filter in such applications as frequency synthesizers and data synchronizers. The circuit of Figure 19 implements one possible PLL filter with the CLC425.

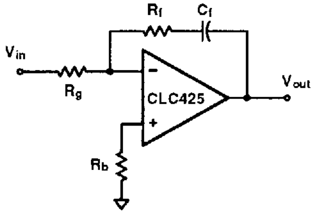


Figure 19: Phased-Locked Loop Filter

Decreasing the Input Noise Voltage

The input noise voltage of the CLC425 can be reduced from its already low $1.05\text{nV}/\sqrt{\text{Hz}}$ by slightly increasing the supply current. Using a 50kΩ resistor to ground on pin 8, as shown in the circuit of Figure 14, will increase the quiescent current to ≈17mA and reduce the input noise voltage to $< 0.95\text{nV}/\sqrt{\text{Hz}}$.

Printed Circuit Board Layout

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillation, see OA-15 for more information. Comlinear suggests the 730013 (through-hole) or the 730027 (SOIC) evaluation board as a guide for high-frequency layout and as an aid in device testing and characterization.