4 Megabit Static RAM Module
512K x 8-Bit

Features

- ☐ High-speed access times
  Com'l: 20, 25, and 35 ns
  Ind'l: 25, and 35 ns

- ☐ High density 4-megabit SRAM module
- ☐ JEDEC approved pinout
- ☐ Single +5V (±10%) power supply
- ☐ TTL compatible inputs and outputs
- ☐ Packages
  CerDIP (600 mil) - D

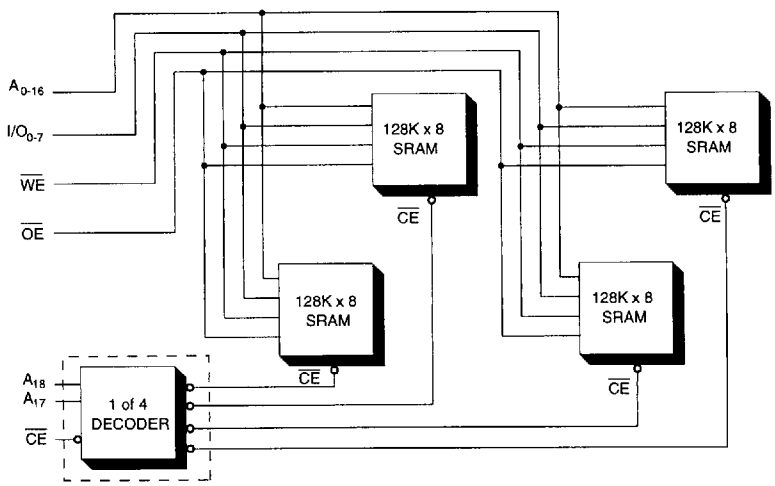
Description

The PDM4M096 is a high-performance CMOS static RAM module organized as 524,288 x 8 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing to this device is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ are both LOW.

The PDM4M096 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM4M096 comes in two versions, the standard power version PDM4M096S and a low power version the PDM4M096L. The two versions are functionally the same and only differ in their power consumption.

The PDM4M096 is available in a 32-pin 600 mil DIP.

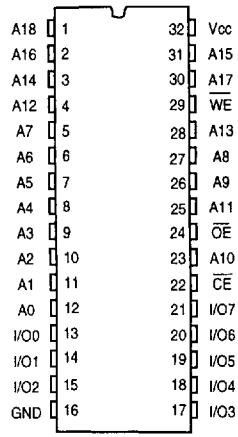
Functional Block Diagram



Note: Decoder is not required for higher speed versions.

Pin Configuration

DIP



Truth Table[1]

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D_{OUT}	Read
X	L	L	D_{IN}	Write
H	H	L	Hi-Z	Output Disable

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings[1]

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	–40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Conditions		PDM4M096 Min.	PDM4M096 Max.	PDM4M096 Min.	PDM4M096 Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = GND to V_{CC}	Com'l	–5	5	–2	2	µA
I_{LO}	Output Leakage Current	V_{CC} = MAX., V_{OUT} = GND to V_{CC} $\overline{CE}$ = V_{IH}, or CE2 = V_{IL}	Com'l	–5	5	–2	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CC} = Min. I_{OL} = 10 mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = –4 mA, V_{CC} = Min.		2.4	—	2.4	—	V
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage			–0.5(1)	0.8	–0.5(1)	0.8	V

NOTE: 1. V_{IL}(min) = –3.0V for pulse width less than 20 ns.

Power Supply Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Power	Function	-20 Com'l.	-20 Ind.	-25 Com'l.	-25 Ind.	-35 Com'l.	-35 Ind.	Unit
I_{CC}	Operating Current $\overline{CE}$ = V_{IL}, V_{CC} = Max., f = f_{MAX}(2)	S	Read Write	380 380	420 420	340 340	380 380	300 300	340 340	mA
		L	Read Write	380 380	420 420	340 340	380 380	300 300	340 340	mA
I_{SB}	Standby Current (TTL Level)	S		160	160	150	150	140	140	mA
	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max., f = f_{MAX} = 1/trc,	L		150	150	140	140	130	130	mA
I_{SB1}	Full Standby Current (CMOS Level)	S		40	40	40	40	40	40	mA
	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max., f = 0, V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V	L		20	20	20	20	20	20	mA

NOTE:All Values are maximum guaranteed values. V_{LC} ≤ 0.2V, V_{HC} ≥ 0.2V

Capacitance(1) (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	50	pF
C_{OUT}	Output Capacitance	50	pF

NOTE: 1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

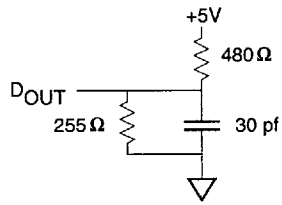


Figure 1. Output Load Equivalent

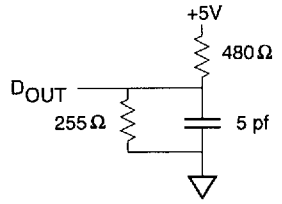
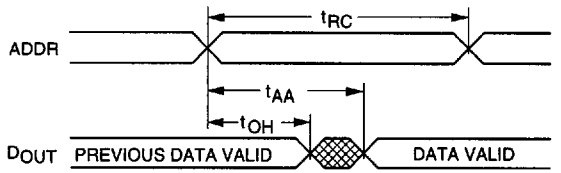
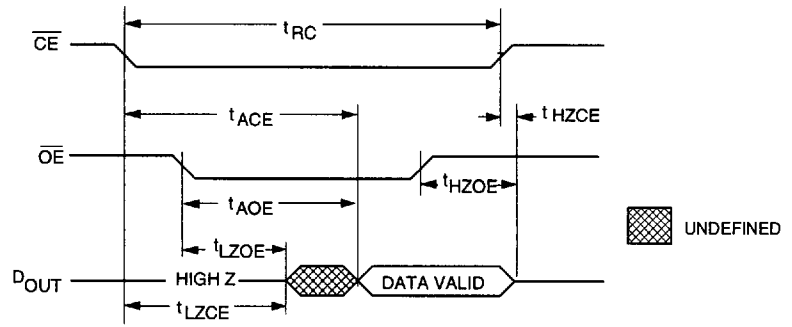


Figure 2. Output Load Equivalent
(for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE}, t_{LZOE}, t_{HZOE})

Read Cycle No. 1[5, 6]



Read Cycle No. 2[3, 5, 7]

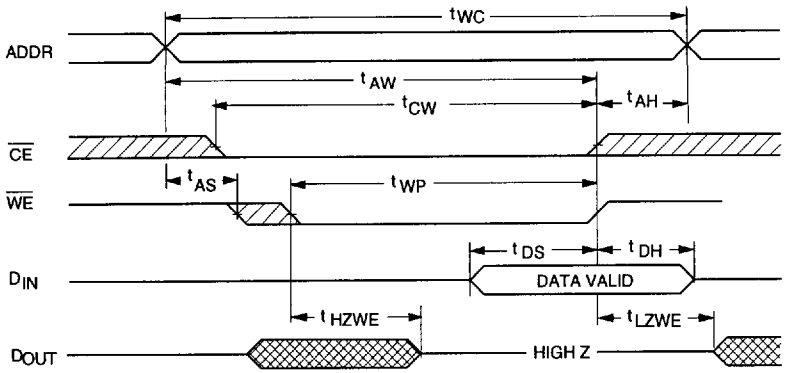


AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

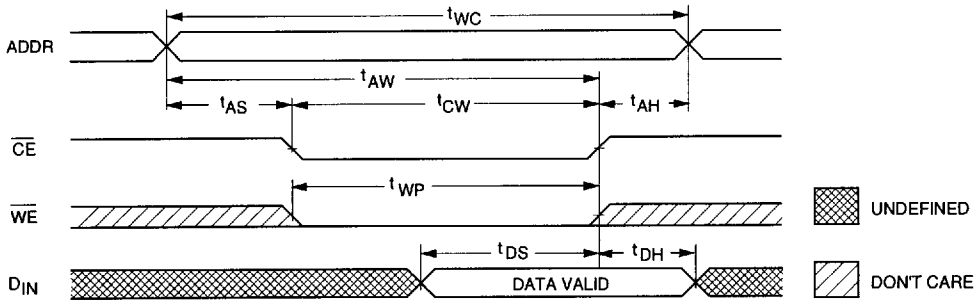
Symbol	Description READ Cycle	-20 Min.	-20 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Units
t_{RC}	READ Cycle time	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{ACE}	Chip enable Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{LZCE}	Chip Enable to Output in Low-Z[4]	0		0		0		ns
t_{HZCE}	Chip Disable to Output in High-Z[2, 3, 4]		10		15		20	ns
t_{PU}	Chip Enable to Power Up Time[4]	0		0		0		ns
t_{PD}	Chip Disable to Power Down Time[4]		20		25		30	ns
t_{AOE}	Output Enable Access Time		10		12		15	ns
t_{LZOE}	Output Enable to Output in Low-Z[4]	0		0		0		ns
t_{HZOE}	Output Disable to Output in High-Z[2, 3, 4]		8		10		20	ns

Note: Reference page 6 for all notes on this page.

Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Chip Enable Controlled)

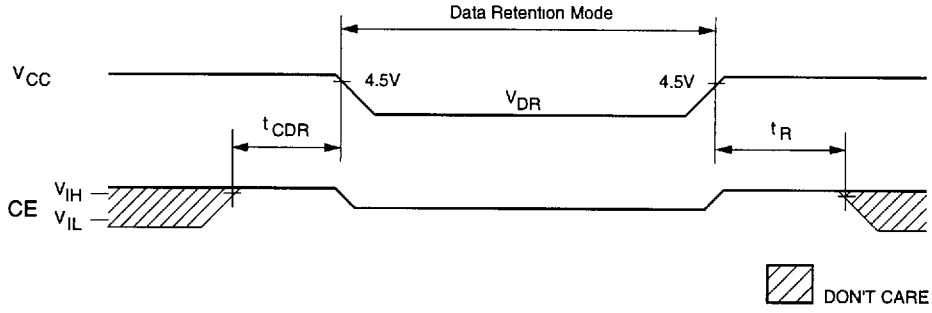


AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Description		-20		-25		-35		
WRITE Cycle	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
WRITE Cycle time	t_{WC}	20		25		35		ns
Chip enable to end of write	t_{CW}	17		20		30		ns
Address Valid to end of write	t_{AW}	17		20		30		ns
Address setup time	t_{AS}	0		0		10		ns
Address hold from end of write [8]	t_{AH}	0		0		0		ns
Write pulse width	t_{WP}	17		17		20		ns
Data setup time	t_{DS}	12		12		15		ns
Data hold time[8]	t_{DH}	0		0		0		ns
Write disable to output in Low-Z[4]	t_{LZWE}	0		0		0		ns
Write enable to output in High-Z[2, 3, 4]	t_{HZWE}		8		10		15	ns

Note: Reference page 6 for all notes on this page.

Low V_{CC} Data Retention Waveform



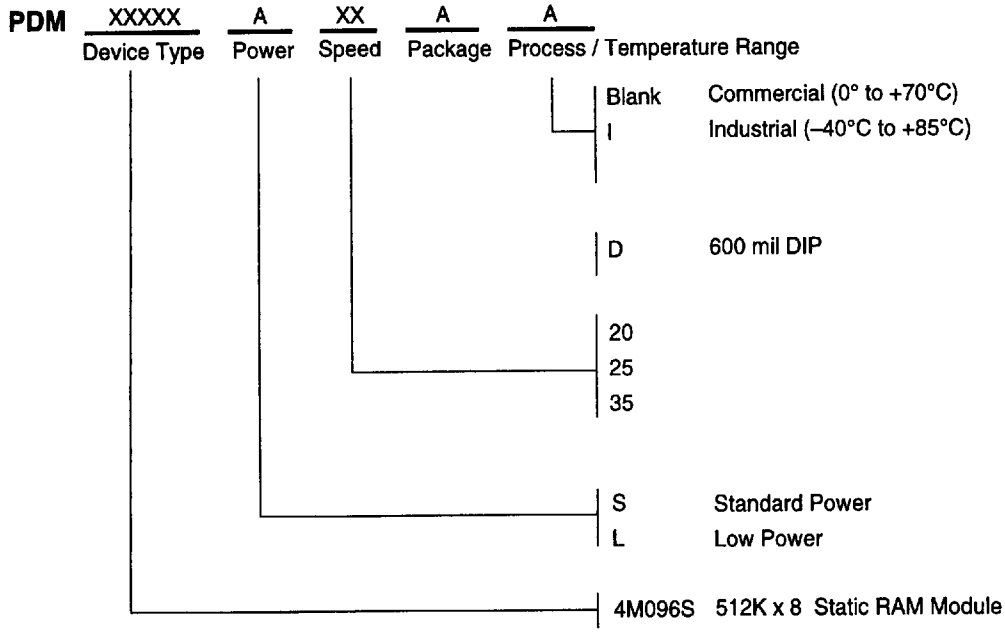
Data Retention Electrical Characteristics (L Version Only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 2V$	—	.380	2	mA
			$V_{CC} = 3V$	—	1.4	3	mA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(4)	Operation Recovery Time			t_{RC}(5)	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)

1. −55°C to +125°C temperature range only.
2. t_{HZCE} and t_{HZWE} aretested with CL = 5 pF as shown in Fig. #2. Transition is measured ±200 mV from steady state voltage.
3. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
4. This parameter is sampled.
5. $\overline{WE}$ is high for a READ cycle.
6. The device is continuously selected. All the Chip Enables are held in their active state.
7. The address is valid prior to or coincident with the latest occuring Chip Enable.
8. During chip enable controlled write cycle t_{DH} and t_{AH} equal 5 ns (min).

Ordering Information



Chip	Package Type
PDM4M096	32-pin CerDIP 600 Mil

Advanced Packaging

Advances in packaging techniques permit a wide variety of solutions to board space problems.

Modules are comprised of individual semiconductor devises with other support devises, such as decoders and capacitors as required, mounted on a multilayer substrate. The substrate is custom designed to provide appropriate circuitry for the components in a package configuration that meets thermal and mechanical design objectives in a minimal amount of board real estate. The final module may have a through-hole pin configuration or may be surface mountable device.

Commercial modules are generally developed using components encapsulated in plastic, surface mounted on FR4 epoxy laminate substrates. The surface mountable component packages may be SOJ, SOIC, VSOP, TSOP, or QFP styles.

Ceramic packaging may be used for devices that need to be hermetic or require extended temperature range performance, such as military applications. Ceramic modules may use LCC or CSOJ component packaging on ceramic substrates with sidebrazed lead attach, or may use multiple die bonded in an MCM-C package.

Module Package Styles

Many module package styles are available from Paradigm. Features and relative board space are described here.

SIP

Vertically mounted, the SIP (Single In-line Package) contains a single row of pins along on edge for through-hole assembly. Pins are on a 100-mil pitch. Components may be mounted on both sides of the substrate. The device is most commonly constructed using plastic encapsulated components on an FR4 substrate, but it may be constructed of ceramic, as well. The vertical orientation and the ability to mount components on both sides of the substrate adds up to exceptional density.

ZIP

ZIP (Zig-zag In-line Package) is similar in space savings to the SIP, since both feature vertical substrate configurations. They also feature the additional advantages of larger pin counts with the structural stability of two rows of pins. Pins are placed on a 100-mil pitch, with 100-mil spacing between the rows.

SIMM

The SIMM (Single In-line Memory Module) package is similar to the SIP. The major difference is, rather than a single row of pins, the bottom edge has a row of connector contacts that are designed to plug into a socket mounted on the motherboard. Spacing between contacts is either 50- or 100-mil pitch. Since socket mounted SIMMs may be changed easily, they offer greater system flexibility by allowing multiple densities and speed grades.

CELP/DIMM

Like the SIMM, the DIMM (Dual readout In-line Memory Module) is socket mounted, but its dual readout contains larger pinouts for extremely high density in a compact component.

DIP

DIP (Dual In-line Package) modules offer a low profile with excellent mechanical ruggedness. Historically, DIP modules have provided the same form, fit, and function as future generation memory devices. Ceramic DIP modules have also been the preferred package for military applications.

PGA

The PGA (Pin Grid Array) has an array of pins arranged in a matrix on a 100-mil grid. This ceramic package style provides a large pin count in a smaller area than possible in package styles with pins only on the package edge or perimeter. With its large number of through-hole contract points, it offers exceptional structural integrity. This package style is also commonly used for multichip arrays bonded within a single cavity.