



54F/74F550 • 54F/74F551 Octal Registered Transceiver with Status Flags

General Description

The 'F550 and 'F551 octal transceivers each contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its TRI-STATE® buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer. The 'F550 is non-inverting; the 'F551 inverts data in both directions.

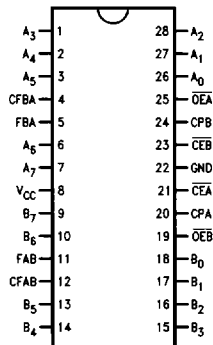
Features

- 8-bit bidirectional I/O port with handshake
- Back-to-back registers for storage
- Register status flag flip-flops
- Separate edge-detecting clears for flags
- Inverting and non-inverting versions
- B outputs sink 64 mA (48 mA Mil)

Ordering Code: See Section 5

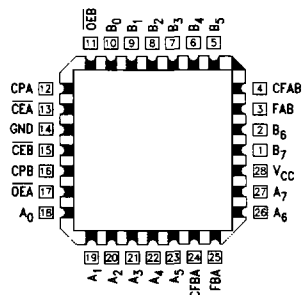
Connection Diagrams

**Pin Assignment for
DIP, SOIC and Flatpak
'F550**



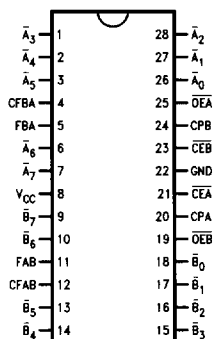
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**Pin Assignment
for LCC and PCC
'F550**



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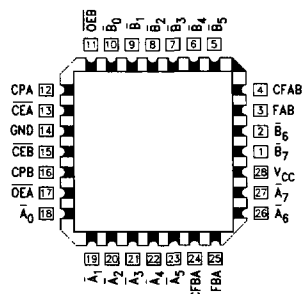
'F551



IEEE/IEC

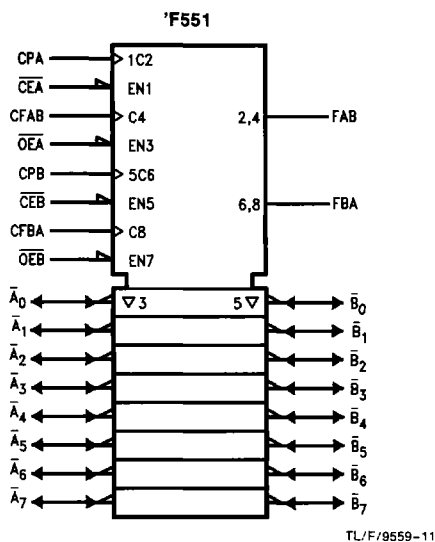
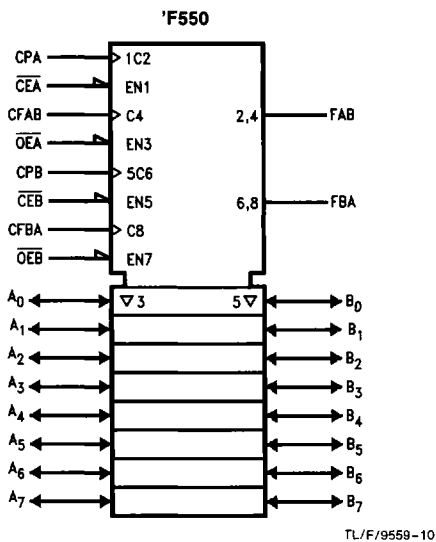
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'F551

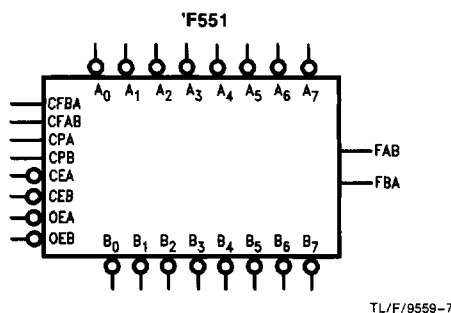
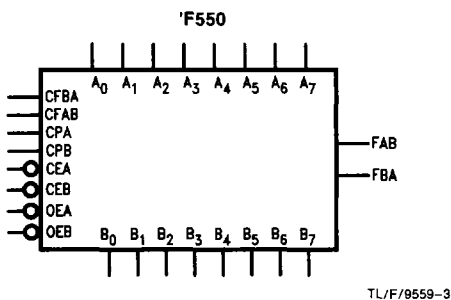


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Connection Diagrams (Continued)



Logic Symbols



Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CPA	A-to-B Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
CPB	B-to-A Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
\overline{CEA}	A-to-B Clock Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{CEB}	B-to-A Clock Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{OEA}	A Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{OEB}	B Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
CFAB	A-to-B Flag Clear Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
CFEA	B-to-A Flag Clear Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
A_0 - A_7	A-to-B Data Inputs or TRI-STATE B-to-A Outputs	3.5/1.083	70 μ A/ -0.65 mA
B_0 - B_7	B-to-A Data Inputs or TRI-STATE A-to-B Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
FAB	A-to-B Status Flag Output (Active HIGH)	3.5/1.083	70 μ A/ -0.65 mA
FBA	B-to-A Status Flag Output (Active HIGH)	600/106.6 (80)	-12 mA/64 mA (48 mA)
		50/33.3	-1 mA/20 mA
		50/33.3	-1 mA/20 mA

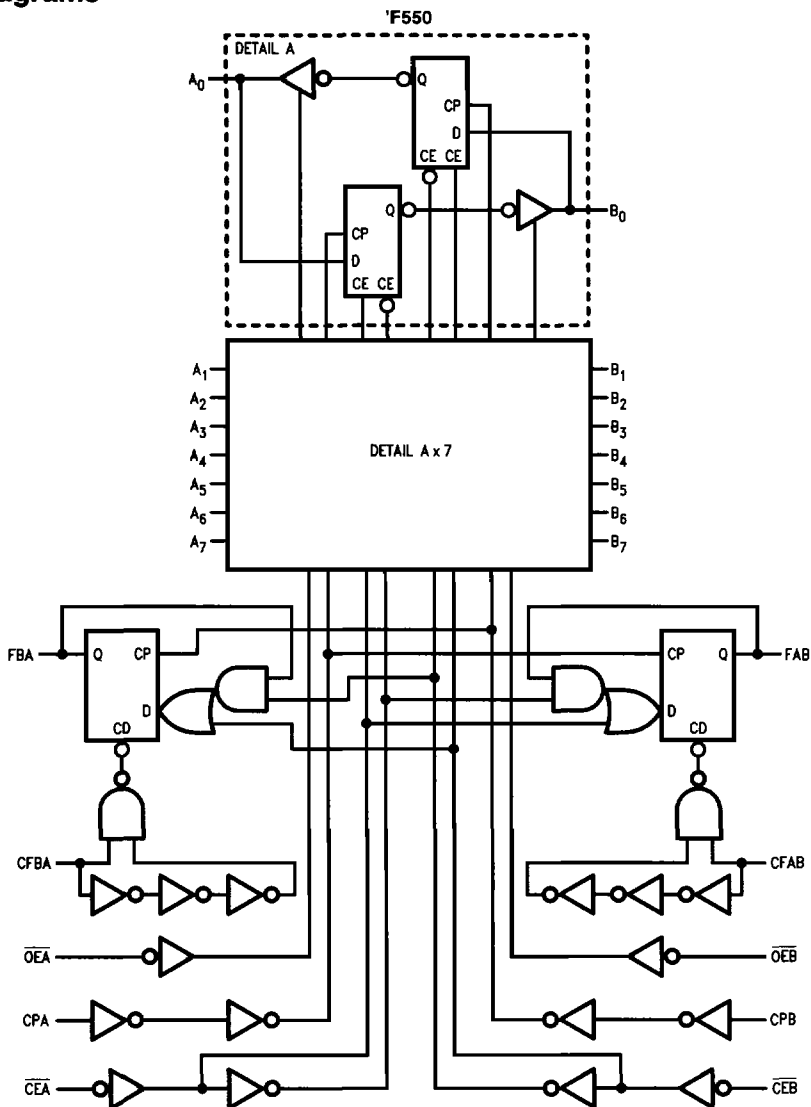
Functional Description

Data applied to the A inputs is entered and stored on the rising edge of the A Clock Pulse (CPA), provided that the A Clock Enable ($\overline{\text{CEA}}$) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH. Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{\text{OEB}}$) signal is made LOW. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a LOW-to-HIGH tran-

sition to the CFAB input. Optionally, the $\overline{\text{OEB}}$ and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{\text{CEB}}$ and CPB enter the B input data and set the B-to-A flag (FBA) output HIGH. A LOW signal on $\overline{\text{OEA}}$ enables the A output buffers and a LOW-to-HIGH transition on CFBA clears the FBA flag.

Logic Diagrams

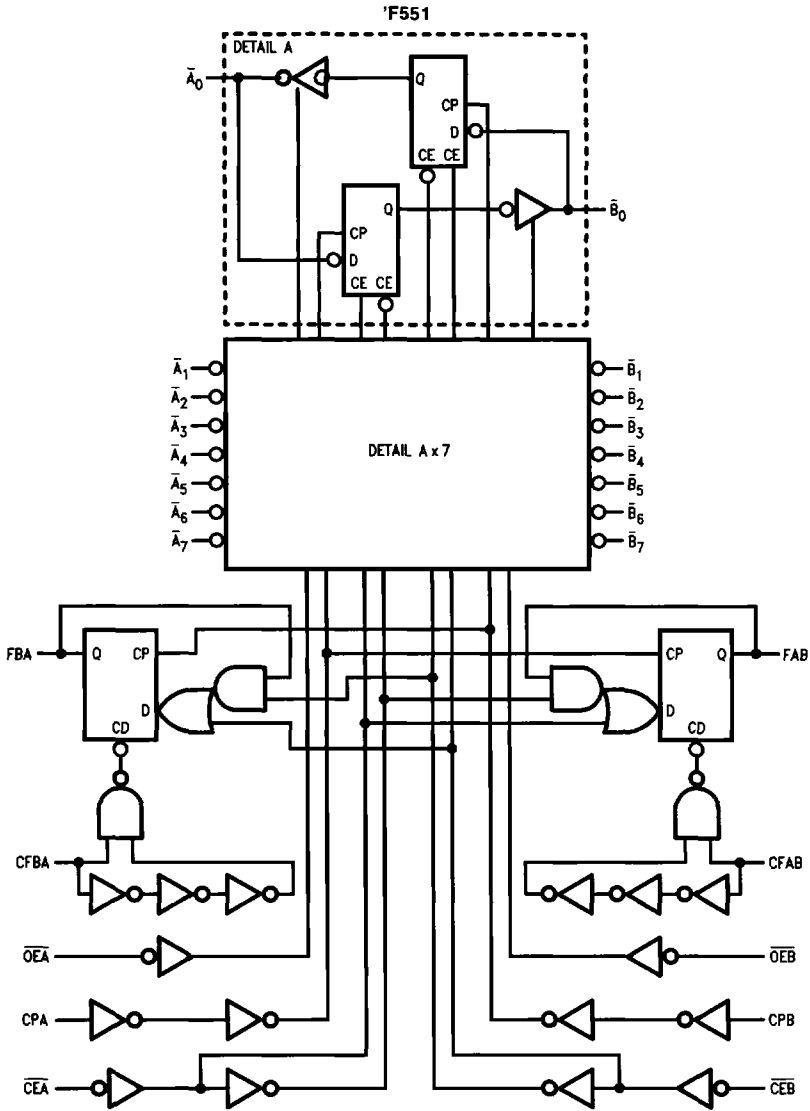


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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA (A ₀ -A ₇)
		54F 10% V _{CC}	2.4				I _{OH} = -3 mA (A ₀ -A ₇)
		54F 10% V _{CC}	2.0				I _{OH} = -12 mA (B ₀ -B ₇)
		74F 10% V _{CC}	2.5				I _{OH} = -1 mA (A ₀ -A ₇)
		74F 10% V _{CC}	2.4				I _{OH} = -3 mA (A ₀ -A ₇)
		74F 10% V _{CC}	2.0				I _{OH} = -12 mA (B ₀ -B ₇)
		74F 5% V _{CC}	2.7				I _{OH} = -1 mA (A ₀ -A ₇)
		74F 5% V _{CC}	2.7				I _{OH} = -3 mA (A ₀ -A ₇)
74F 10% V _{CC}	2.0		I _{OH} = -15 mA (B ₀ -B ₇)				
V _{OL}	Output Low Voltage	54F 10% V _{CC}			V	Min	I _{OL} = 20 mA (A ₀ -A ₇)
		54F 10% V _{CC}					I _{OL} = 48 mA (B ₀ -B ₇)
		74F 10% V _{CC}	0.5				I _{OL} = 24 mA (A ₀ -A ₇)
		74F 10% V _{CC}	0.55				I _{OL} = 64 mA (B ₀ -B ₇)
I _{IH}	Input HIGH Current				μA	Max	V _{IN} = 2.7V (Non I/O Inputs)
I _{BVI}	Input HIGH Current Breakdown Test				μA	Max	V _{IN} = 7.0V (Non I/O Inputs)
I _{IL}	Input LOW Current				mA	Max	V _{IN} = 0.5V (Non I/O Inputs)
I _{IH} + I _{OZH}	Output Leakage Current				μA	Max	V _{OUT} = 2.7V (A ₀ -A ₇ , B ₀ -B ₇)
I _{IL} + I _{OZL}	Output Leakage Current				μA	Max	V _{OUT} = 0.5V (A ₀ -A ₇ , B ₀ -B ₇)
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V (A ₀ -A ₇)
		-100		-225	mA	Max	V _{OUT} = 0V (B ₀ -B ₇)
I _{CEX}	Output HIGH Leakage Current				μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test				μA	0.0V	V _{OUT} = V _{CC}
I _{COH}	Power Supply Current	84		140	mA	Max	V _O = HIGH
I _{COL}	Power Supply Current	105		140	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current	102		140	mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig No
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPA or CPB to B_n or A_n	3.0 4.0	5.5 7.0	7.5 9.0			2.5 3.5	8.5 10.0	ns	2-3
t_{PLH}	Propagation Delay CPA or CPB to FBA or FAB	3.5	6.0	8.0			3.0	9.0	ns	2-3
t_{PHL}	Propagation Delay CFAB or CFBA to FAB or FBA	5.0	9.0	11.5			4.5	13.0	ns	2-3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}A$ or $\overline{OE}B$ to A_n or B_n	2.5 3.5	5.5 7.0	7.5 9.5			2.0 3.0	8.5 10.5	ns	2-5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}A$ or $\overline{OE}B$ to A_n or B_n	3.0 2.5	6.5 5.5	9.0 7.5			2.5 2.0	10.0 8.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig No
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n, B_n to CPA, CPB	4.0 4.0				4.5 4.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n, B_n to CPA, CPB	2.0 2.0				2.5 2.5			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CE}A, \overline{CE}B$ to CPA, CPB	1.0 4.0				1.5 4.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CE}A, \overline{CE}B$ to CPA, CPB	2.0 2.0				2.5 2.5			
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0				3.5 3.5		ns	2-4
$t_w(H)$	Pulse Width, HIGH CFAB or CFBA	3.0				3.5		ns	2-4
t_{rec}	Recovery Time CFAB, CFBA to CPA, CPB	9.0				10.0		ns	2-6