128Kx8 MONOLITHIC SRAM, SMD 5962-96691 (pending)

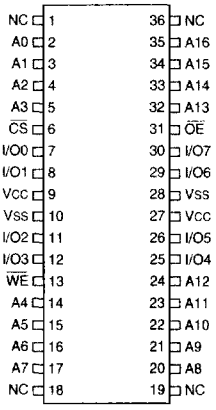
FEATURES

- Access Times 17, 20, 25, 35, 45, 55ns
- Radiation Tolerant Devices Available
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
  - 32 lead Ceramic SOJ (Package 101)
  - 36 lead Ceramic SOJ (Package 100)
  - 36 lead Ceramic Flat Pack (Package 200)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
  - 32 pin Ceramic DIP (Package 300)
  - 32 lead Ceramic SOJ (Package 101)
  - 32 lead Ceramic Flat Pack (Package 206)
- MIL-STD-883 Compliant Devices Available
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- 2V Data Retention Devices Available (Low Power Version)
- TTL Compatible Inputs and Outputs

REVOLUTIONARY PINOUT

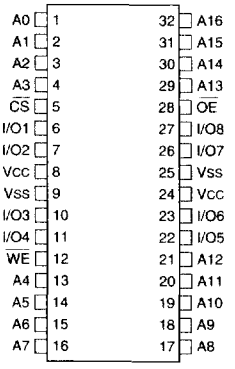
36 FLAT PACK
36 CSOJ

TOP VIEW



32 CSOJ (DR)

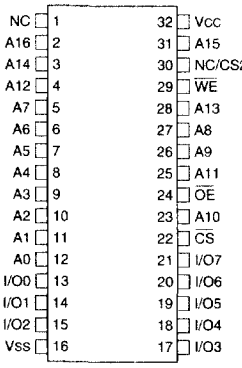
TOP VIEW



EVOLUTIONARY PINOUT

32 DIP
32 CSOJ (DE)
32 FLAT PACK (FE)

TOP VIEW



* NC for single chip select devices
CS_2 for dual chip select devices

PIN DESCRIPTION

A_{0-16}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Package	Speed (ns)	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	32 Pin CSOJ, DIP, Flat Pack Evolutionary	17 to 55	20	pF
			36 Pin CSOJ, Flat Pack and	17 to 25	12	pF
			32 Pin CSOJ Revolutionary	35 to 55	20	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	32 Pin CSOJ, DIP, Flat Pack Evolutionary	17 to 55	20	pF
			36 Pin CSOJ, Flat Pack and	17 to 25	12	pF
			32 Pin CSOJ Revolutionary	35 to 55	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	-17		-20		-25		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		120		120		120	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		20		20		15	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		2.4		2.4		V

Parameter	Sym	Conditions	-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		120		120		120	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		15		15		15	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, V_{CC} = 4.5	2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		35		45		55		ns
Address Access Time	t_{AA}		17		20		25		35		45		55	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		17		20		25		35		45		55	ns
Output Enable to Output Valid	t_{OE}		10		12		15		20		25		30	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		3		3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		10		10		12		20		20		20	ns
Output Disable to Output in High Z	t_{OHZ}[1]		10		10		12		20		20		20	ns

1. This parameter is guaranteed by design but not tested.

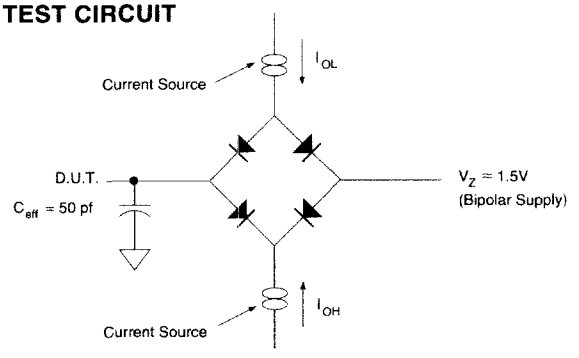
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
Write Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		35		45		55		ns
Chip Select to End of Write	t_{CW}	14		15		20		25		30		45		ns
Address Valid to End of Write	t_{AW}	15		15		20		25		30		45		ns
Data Valid to End of Write	t_{DW}	10		12		15		20		25		25		ns
Write Pulse Width	t_{WP}	14		15		20		25		30		45		ns
Address Setup Time	t_{AS}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	3		3		3		4		4		4		ns
Write Enable to Output in High Z	t_{WHZ}[1]		10		12		15		20		25		25	ns
Data Hold Time	t_{DH}	0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit ATE tester includes jig capacitance.

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

LOW POWER VERSION ONLY

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -0.2V	2.0		5.5	V
Data Retention Current	I_{CCDR2}	V_{CC} = 2V		500	750	µA
	I_{CCDR3}	V_{CC} = 3V		1	2.6	mA

ORDERING INFORMATION

W M S 128K8 X - XXX X X X X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

SPECIAL PROCESSING:
E = Epitaxial Layer

DEVICE GRADE:
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE:
C = 32 Pin Ceramic .600" DIP (Package 300)
DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary
DJ = 36 Lead Ceramic SOJ (Package 100)
DR = 32 Lead Ceramic SOJ (Package 101) Revolutionary
F = 36 Lead Ceramic Flat Pack (Package 200)
FE = 32 Lead Ceramic Flat Pack (Package 206)

ACCESS TIME (ns)

IMPROVEMENT MARK
C = Dual Chip Select Device
L = Low Power for 2V Data Retention

ORGANIZATION, 128K x 8

SRAM

MONOLITHIC

WHITE MICROELECTRONICS

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 8 SRAM Monolithic	55ns	32 lead SOJ Revol (DR)	5962-96691 05HUX*
128K x 8 SRAM Monolithic	45ns	32 lead SOJ Revol (DR)	5962-96691 06HUX*
128K x 8 SRAM Monolithic	35ns	32 lead SOJ Revol (DR)	5962-96691 07HUX*
128K x 8 SRAM Monolithic	25ns	32 lead SOJ Revol (DR)	5962-96691 08HUX*
128K x 8 SRAM Monolithic	20ns	32 lead SOJ Revol (DR)	5962-96691 09HUX*
128K x 8 SRAM Monolithic	17ns	32 lead SOJ Revol (DR)	5962-96691 10HUX*
128K x 8 SRAM Monolithic	55ns	32 lead SOJ Evol (DE)	5962-96691 05HTX*
128K x 8 SRAM Monolithic	45ns	32 lead SOJ Evol (DE)	5962-96691 06HTX*
128K x 8 SRAM Monolithic	35ns	32 lead SOJ Evol (DE)	5962-96691 07HTX*
128K x 8 SRAM Monolithic	25ns	32 lead SOJ Evol (DE)	5962-96691 08HTX*
128K x 8 SRAM Monolithic	20ns	32 lead SOJ Evol (DE)	5962-96691 09HTX*
128K x 8 SRAM Monolithic	17ns	32 lead SOJ Evol (DE)	5962-96691 10HTX*
128K x 8 SRAM Monolithic	55ns	32 pin DIP (C)	5962-96691 05HYX*
128K x 8 SRAM Monolithic	45ns	32 pin DIP (C)	5962-96691 06HYX*
128K x 8 SRAM Monolithic	35ns	32 pin DIP (C)	5962-96691 07HYX*
128K x 8 SRAM Monolithic	25ns	32 pin DIP (C)	5962-96691 08HYX*
128K x 8 SRAM Monolithic	20ns	32 pin DIP (C)	5962-96691 09HYX*
128K x 8 SRAM Monolithic	17ns	32 pin DIP (C)	5962-96691 10HYX*
128K x 8 SRAM Monolithic	55ns	36 lead SOJ (DJ)	5962-96691 05HZX*
128K x 8 SRAM Monolithic	45ns	36 lead SOJ (DJ)	5962-96691 06HZX*
128K x 8 SRAM Monolithic	35ns	36 lead SOJ (DJ)	5962-96691 07HZX*
128K x 8 SRAM Monolithic	25ns	36 lead SOJ (DJ)	5962-96691 08HZX*
128K x 8 SRAM Monolithic	20ns	36 lead SOJ (DJ)	5962-96691 09HZX*
128K x 8 SRAM Monolithic	17ns	36 lead SOJ (DJ)	5962-96691 10HZX*
128K x 8 SRAM Monolithic	55ns	36 lead Flatpack (F)	5962-96691 05HXX*
128K x 8 SRAM Monolithic	45ns	36 lead Flatpack (F)	5962-96691 06HXX*
128K x 8 SRAM Monolithic	35ns	36 lead Flatpack (F)	5962-96691 07HXX*
128K x 8 SRAM Monolithic	25ns	36 lead Flatpack (F)	5962-96691 08HXX*
128K x 8 SRAM Monolithic	20ns	36 lead Flatpack (F)	5962-96691 09HXX*
128K x 8 SRAM Monolithic	17ns	36 lead Flatpack (F)	5962-96691 10HXX*

* Pending