PYRAMID SEMICONDUCTOR CORPORATION

P4C1024

HIGH SPEED 128K X 8 DUAL CHIP ENABLE CMOS STATIC RAM

FEATURES

- **Access Times**
  – 17/20/25/35/45/55/70 ns
- **Single 5V±10% Power Supply**
- **Easy Memory Expansion using $\overline{CE}_1$, CE_2, and $\overline{OE}$ Inputs**
- **Battery Backup: 2V Data Retention [P4C1024L only]**
- **Common Data I/O**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Automatic Power Down**
- **Packages**
  – 32-Pin 400 or 600 mil Ceramic DIP
  – 32-Pin 300 mil Ceramic SOJ
  – 32-Pin Ceramic LCC (400x820 mil) [2-sided]
  – 32-Pin Ceramic LCC (450x550 mil)
  – 32-Pin Solder Seal Ceramic Flatpack
  – 32-Pin 600 mil Plastic DIP
  – 32-Pin 400 mil Plastic SOJ

DESCRIPTION

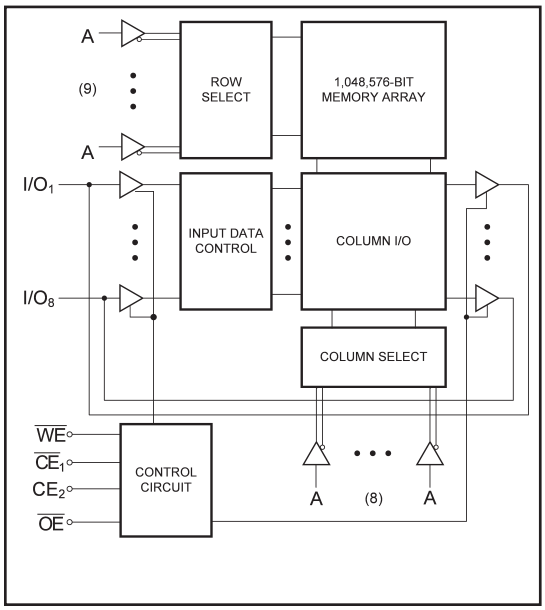
The P4C1024/L is a 1,048,576-bit high speed CMOS static RAM organized as 128K x 8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

Access times of 17 ns to 70 ns are available. CMOS is utlilized to reduce power consumption to a low level.

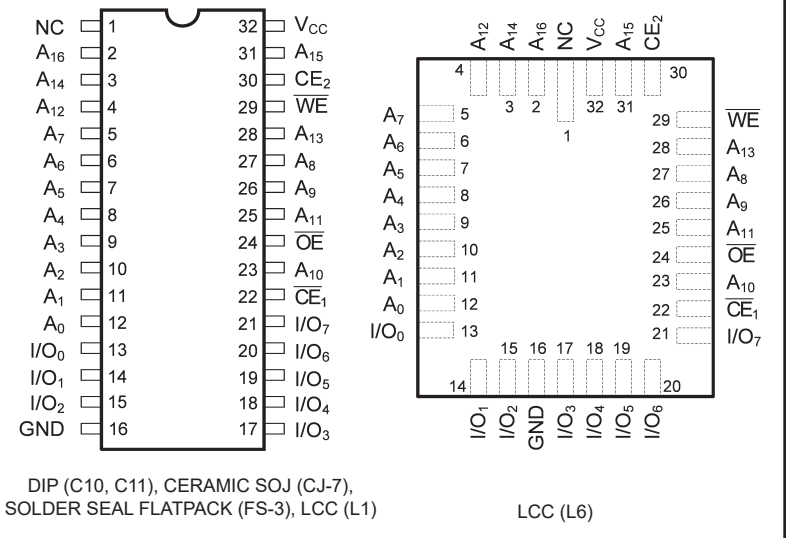
The P4C1024/L device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{16}. Reading is accomplished by device selection ($\overline{CE}_1$ low and CE_2 high) and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}_1$ or $\overline{OE}$ is HIGH or $\overline{WE}$ or CE_2 is LOW. The low power version offers 2V data retention mode.

The P4C1024/L is packaged in a 32-pin 400 or 600 mil ceramic DIP and in a 32-pin ceramic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (C10, C11), CERAMIC SOJ (CJ-7), SOLDER SEAL FLATPACK (FS-3), LCC (L1)

LCC (L6)

MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +6	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{CC}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	Output High Voltage (I/O_0-I/O_7)	I_{OH} = -4mA, V_{CC}=4.5V	2.4		V
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 6mA, Com/Ind		0.40	V
		I_{OL} = 6mA, Military		0.55	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$=V_{IH}	-10	10	µA
I_{SB}	V_{CC} Current TTL Standby Current (TTL Input Levels)	$\overline{CE_1}$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{CC}=Max, f=0, Outputs Open		33	mA
I_{SB1}	V_{CC} Current CMOS Standby Current (CMOS Input Levels)	$\overline{CE_1}$ ≥ V_{HC} or CE_2 ≤ V_{LC}, V_{CC}=Max,f=0, Outputs Open, V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}		17	mA

N/A = Not applicable

POWER DISSIPATION CHARACTERISTICS VS. SPEED

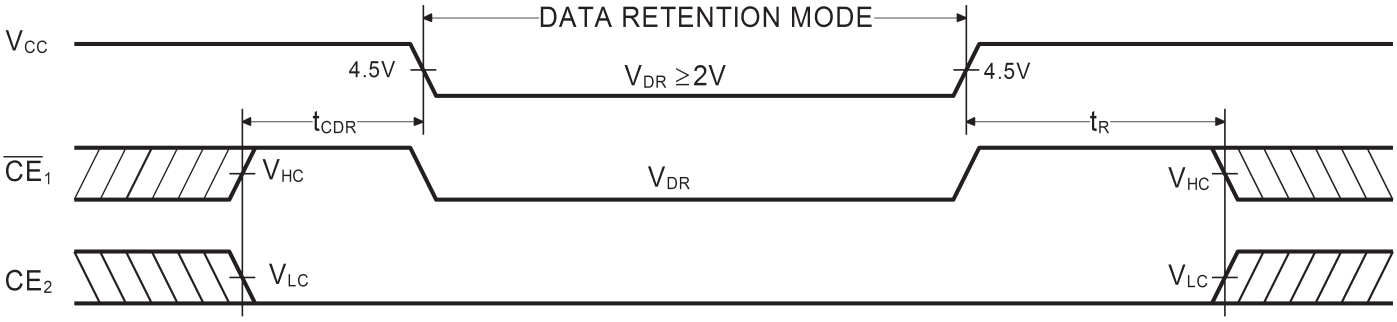
Symbol	Parameter	Temperature	-17	-20	-25	-35	-45	-55	-70	Unit
I_{CC}	Dynamic Operating Current	Commercial	100	90	85	80	N/A	N/A	N/A	mA
		Industrial	110	100	95	90	85	N/A	N/A	mA
		Military	125	110	105	100	95	90	85	mA

DATA RETENTION CHARACTERISTICS (P4C1024L ONLY)

Symbol	Parameter	Test Conditions	Min	Typ* V_{cc} =		Max V_{cc} =		Unit
				2.0V	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	$\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		325	530	6,000	9,000	µA
t_{CDR}	Chip Deselect to Data Retention Time		0					ns
t_R†	Operation Recovery Time		t_{RC}§					ns

§ t_{RC} = Read Cycle Time
† This Parameter is guaranteed but not tested
* T_A = +25°C

DATA RETENTION WAVEFORM

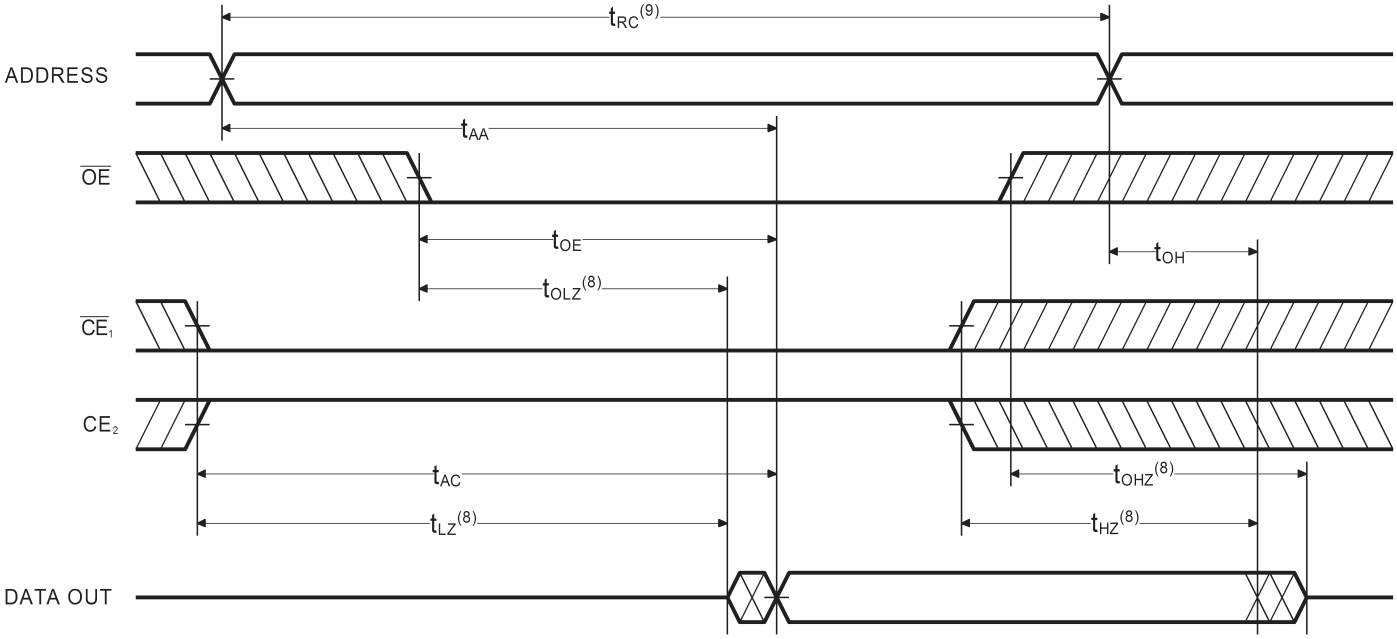


AC ELECTRICAL CHARACTERISTICS—READ CYCLE

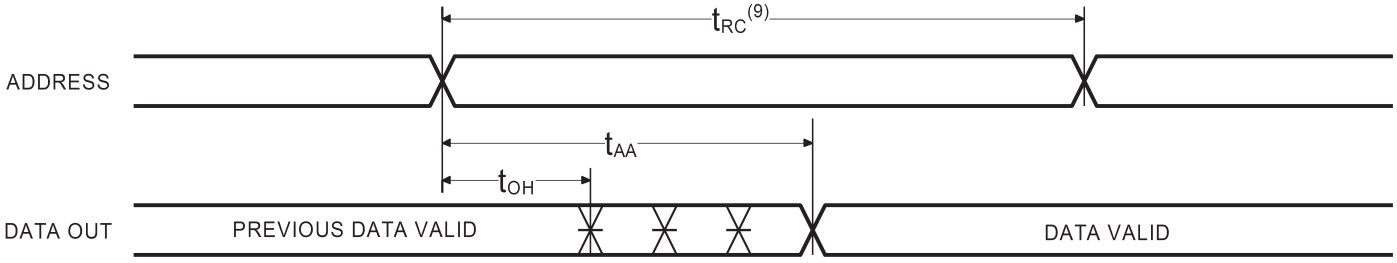
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-17		-20		-25		-35		-45		-55		-70		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	17		20		25		35		45		55		70		ns
t_{AA}	Address Access Time		17		20		25		35		45		55		70	ns
t_{AC}	Chip Enable Access Time		17		20		25		35		45		55		70	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	3		3		3		3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		10		12		13		15		20		25		30	ns
t_{OE}	Output Enable Low to Data Valid		10		12		13		15		20		25		30	ns
t_{OLZ}	Output Enable Low to Low Z	0		0		0		0		0		0		0		ns
t_{OHZ}	Output Enable High to High Z		9		10		12		15		20		25		30	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		17		20		25		35		45		55		70	ns

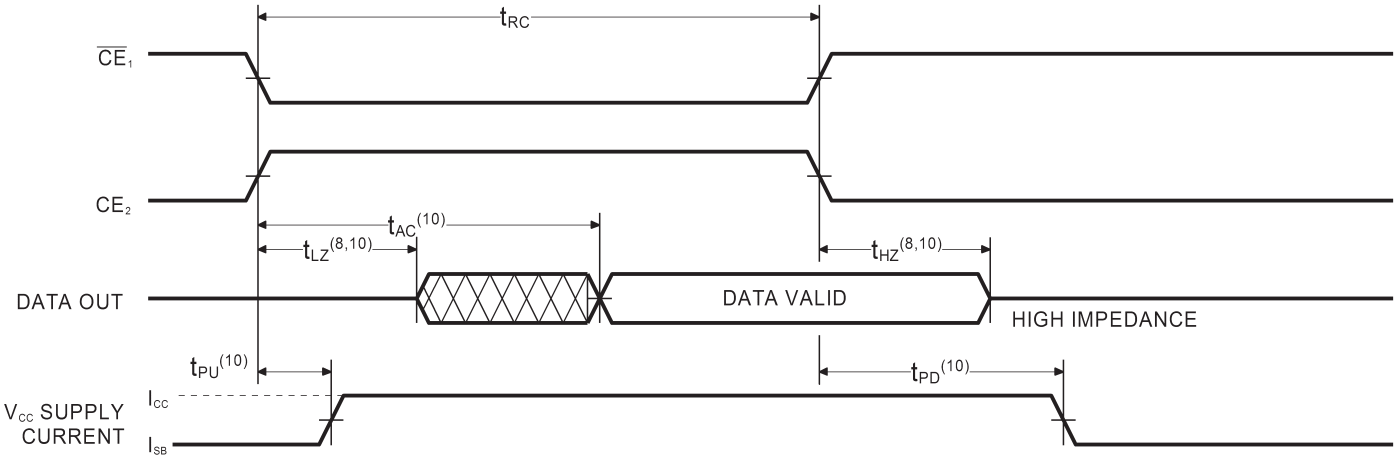
TIMING WAVEFORM OF READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[5]



TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)[5,7,8]



TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{CE}_1$, CE_2 CONTROLLED)[5, 7, 10]



Notes:

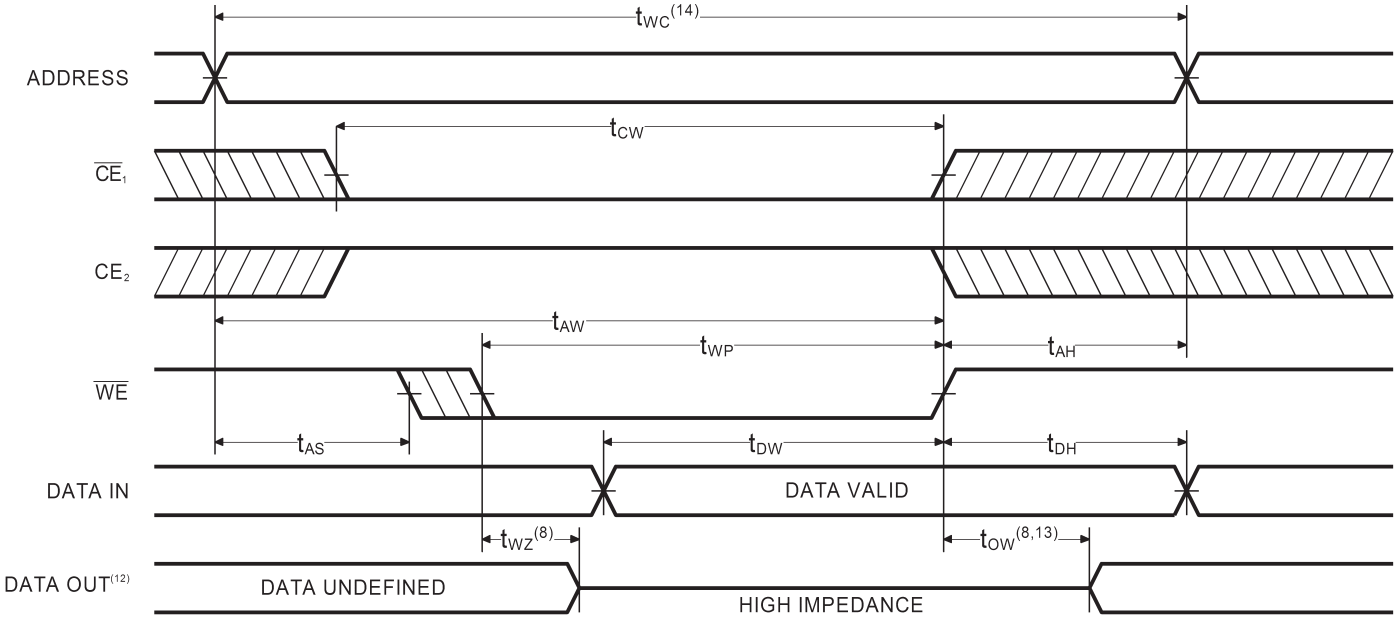
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.
10. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE}_1$ or CE_2 causes them.

AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

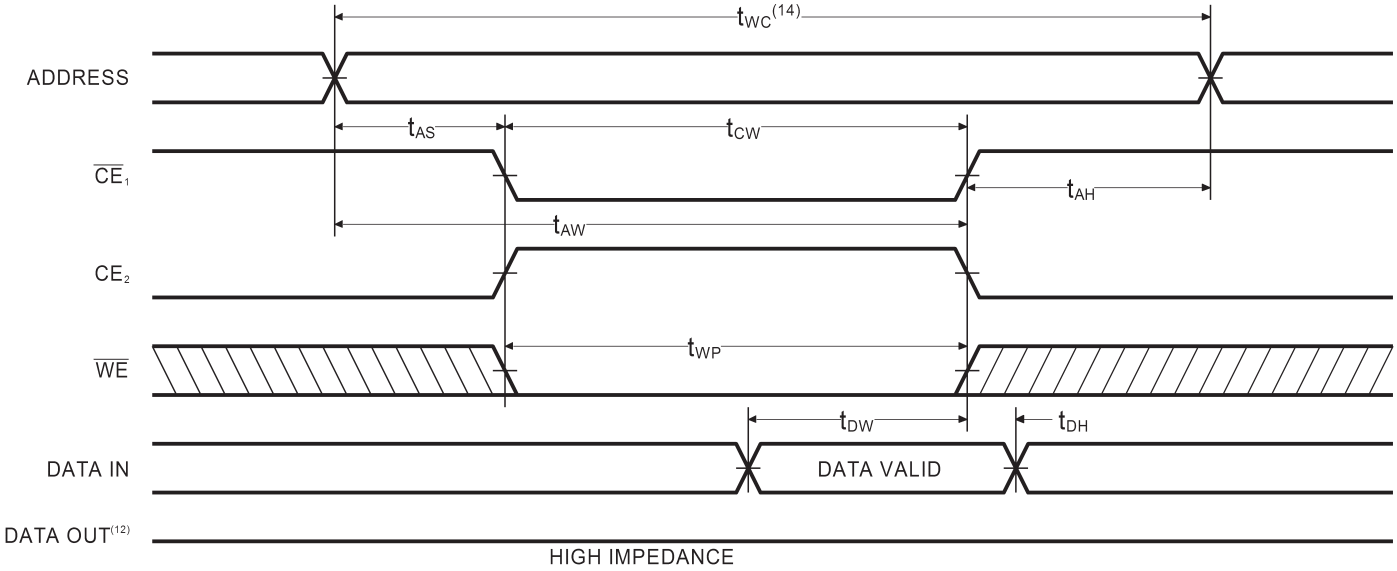
Sym	Parameter	-17		-20		-25		-35		-45		-55		-70		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	17		20		25		35		45		55		70		ns
t_{CW}	Chip Enable Time to End of Write	14		15		20		25		35		40		45		ns
t_{AW}	Address Valid to End of Write	14		15		20		25		35		40		45		ns
t_{AS}	Address Setup Time	0		0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	14		15		20		25		35		40		45		ns
t_{AH}	Address Hold Time	0		0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	9		10		15		20		30		35		40		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z	8		9		10		15		20		25		30		ns
t_{OW}	Output Active from End of Write	3		3		3		3		3		3		3		ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[11]



Notes:
11. $\overline{CE_1}$ and $\overline{WE}$ must be LOW, and CE_2 HIGH for WRITE cycle.
12. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
13. If $\overline{CE_1}$ goes HIGH, or CE_2 goes LOW, simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state
14. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[11]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	D_{IN}	Active

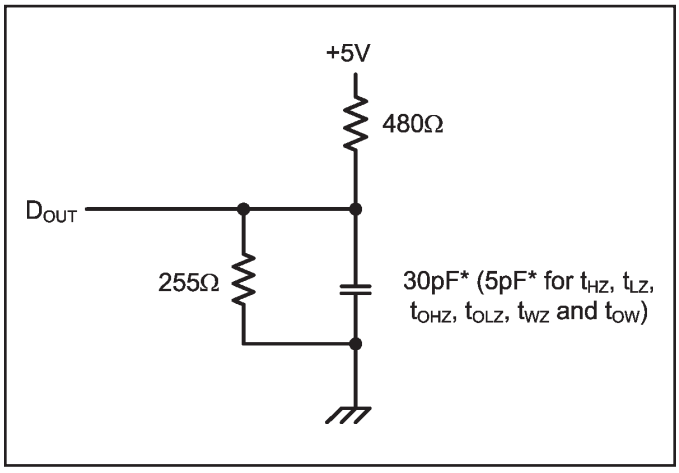


Figure 1. Output Load

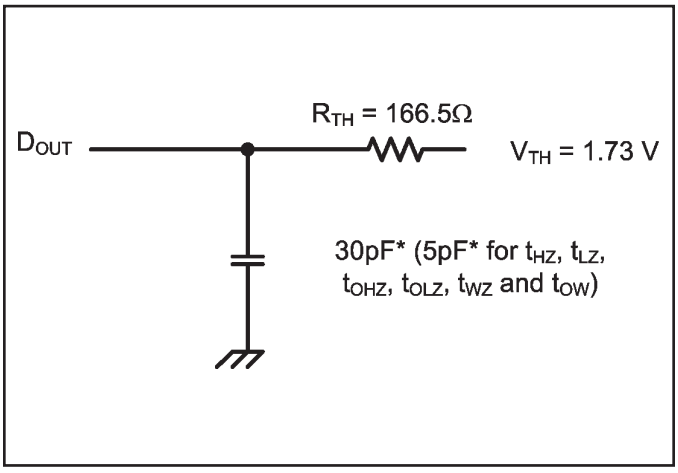


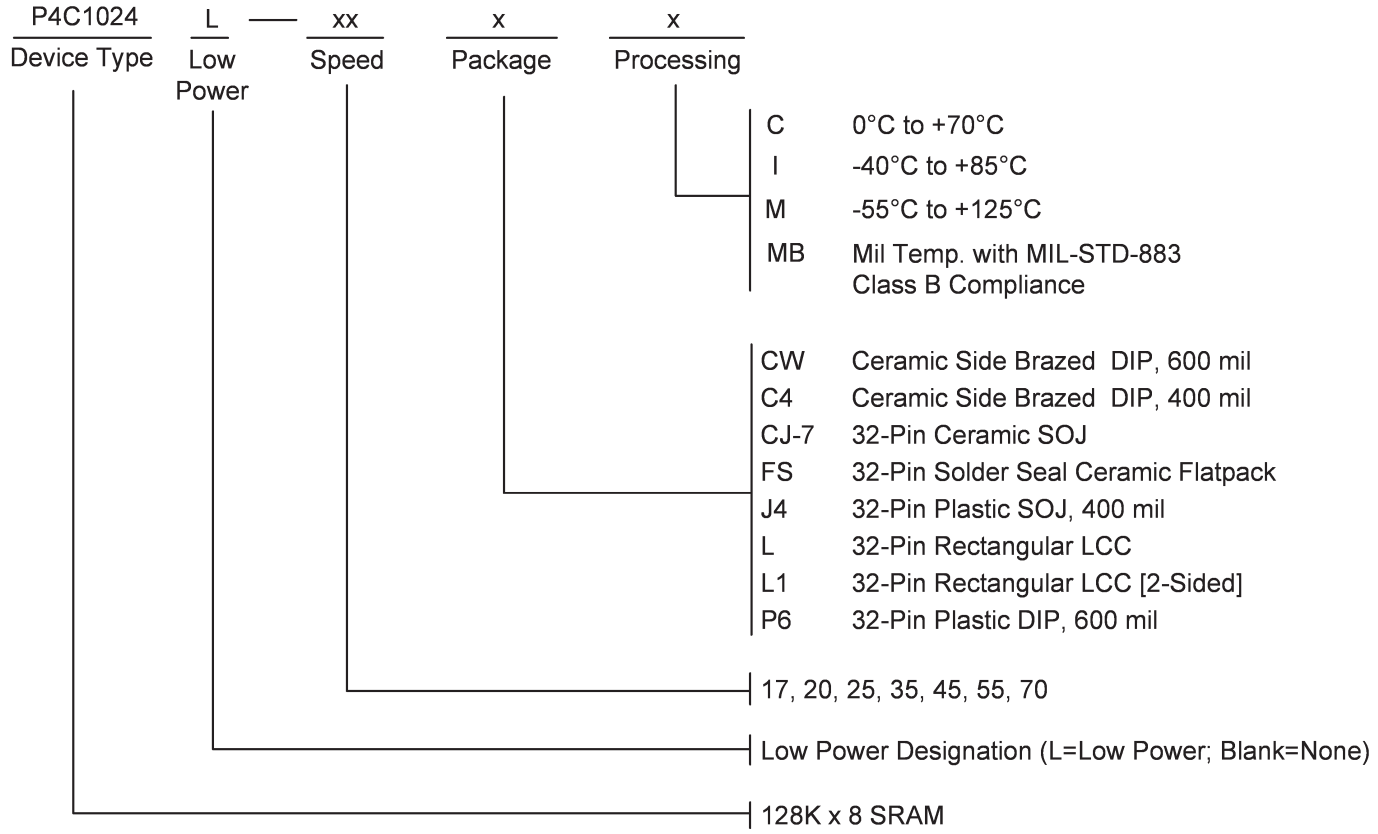
Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Because of the high speed of the P4C1024, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground.

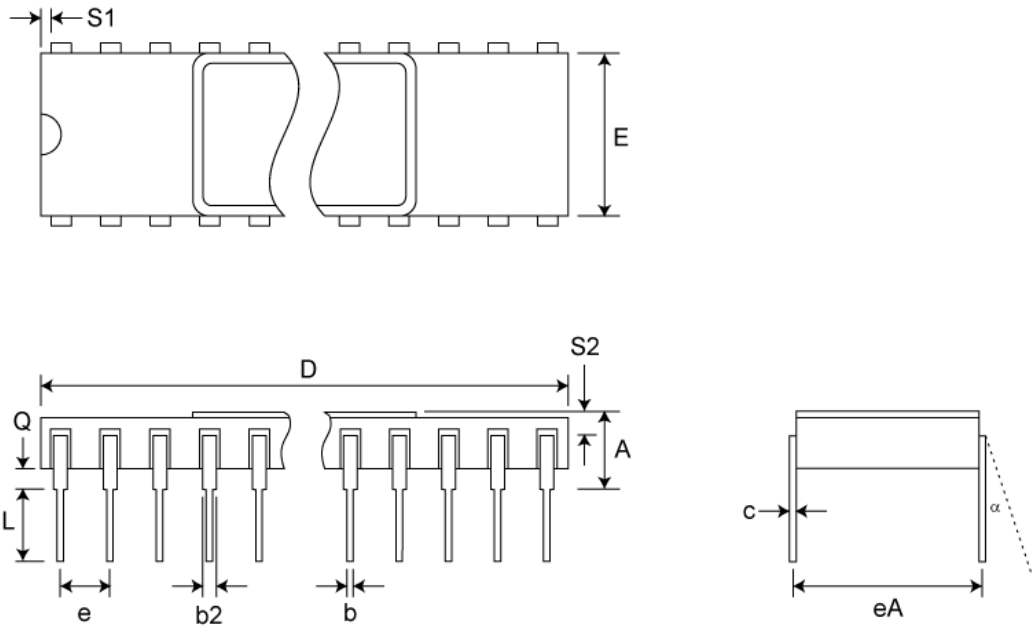
To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION



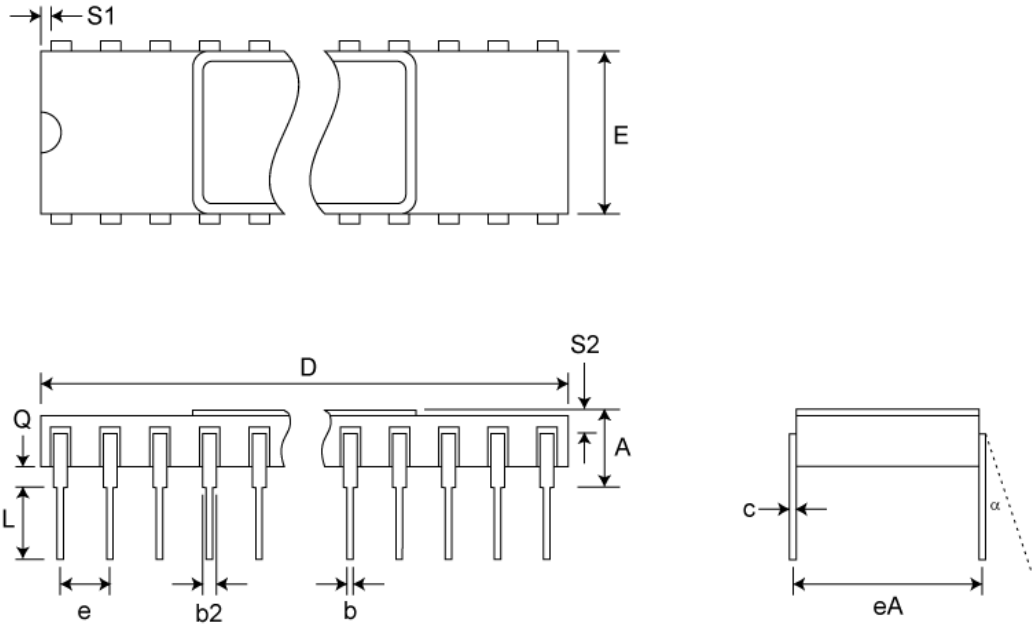
Pkg #	C10	
# Pins	32 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.680
E	0.510	0.620
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



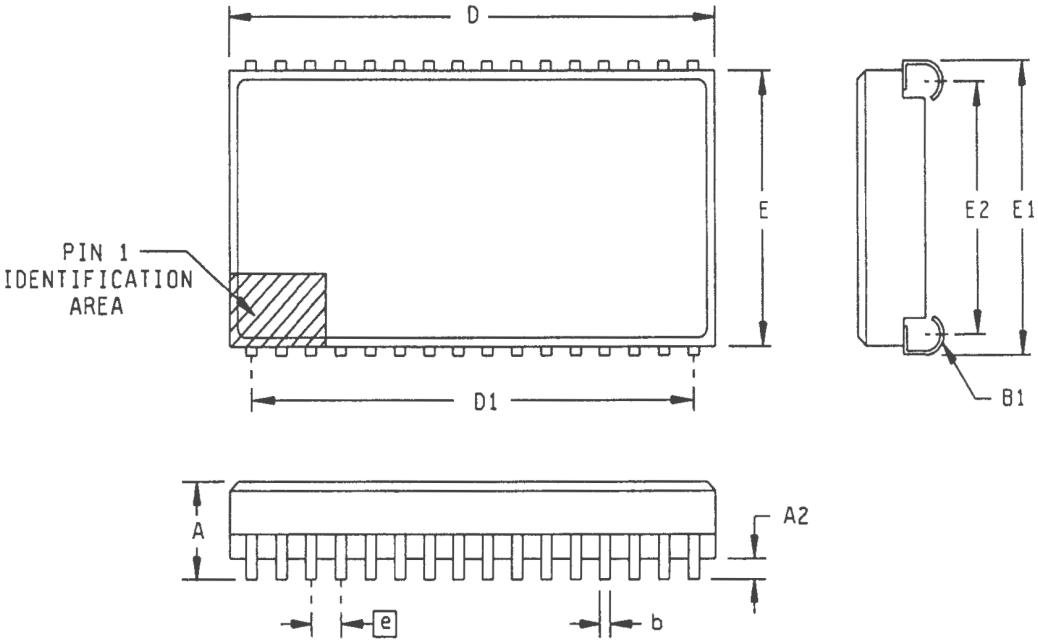
Pkg #	C11	
# Pins	32 (400 mil)	
Symbol	**Min**	**Max**
A	-	0.232
b	0.014	0.023
b2	0.038	0.065
C	0.008	0.018
D	-	1.700
E	0.350	0.410
eA	0.400 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



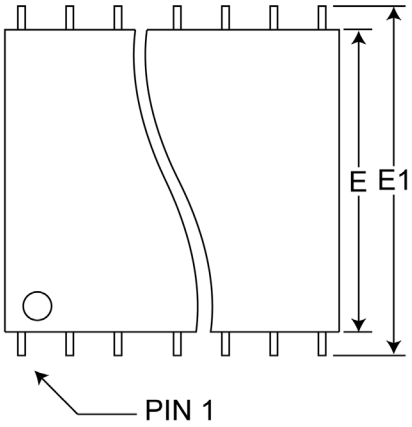
Pkg #	CJ-7	
# Pins	32	
Symbol	**Min**	**Max**
A	0.132	0.144
A2	0.026	0.036
b	0.015	0.019
B1	0.030	0.040
D	0.812	0.828
D1	0.740	0.760
E	0.405	0.415
E1	0.435	0.445
E2	0.360	0.380
e	0.050 BSC	

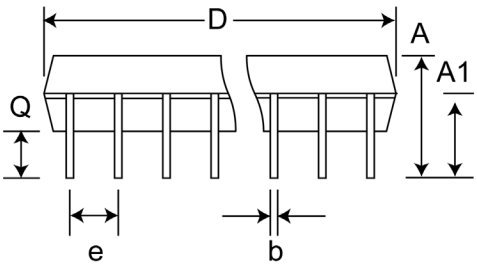
CERAMIC SOJ SMALL OUTLINE IC PACKAGE

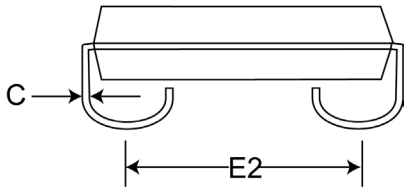


Pkg #	J400	
# Pins	32 (400 mil)	
Symbol	**Min**	**Max**
A	0.128	0.148
A1	0.082	-
b	0.015	0.020
C	0.007	0.013
D	0.820	0.830
e	0.050 BSC	
E	0.395	0.405
E1	0.435	0.445
E2	0.370 BSC	
Q	0.025	-

SOJ SMALL OUTLINE IC PACKAGE (400 mil)

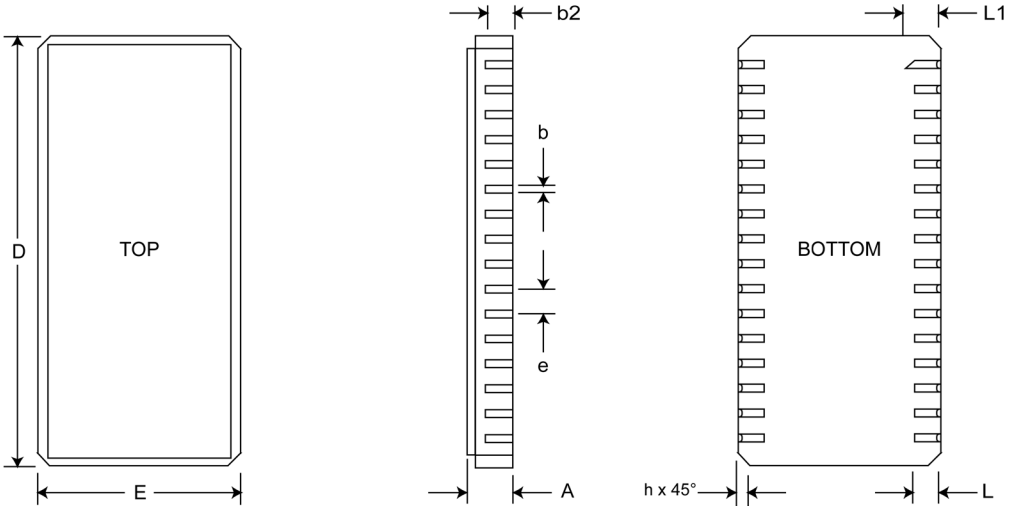






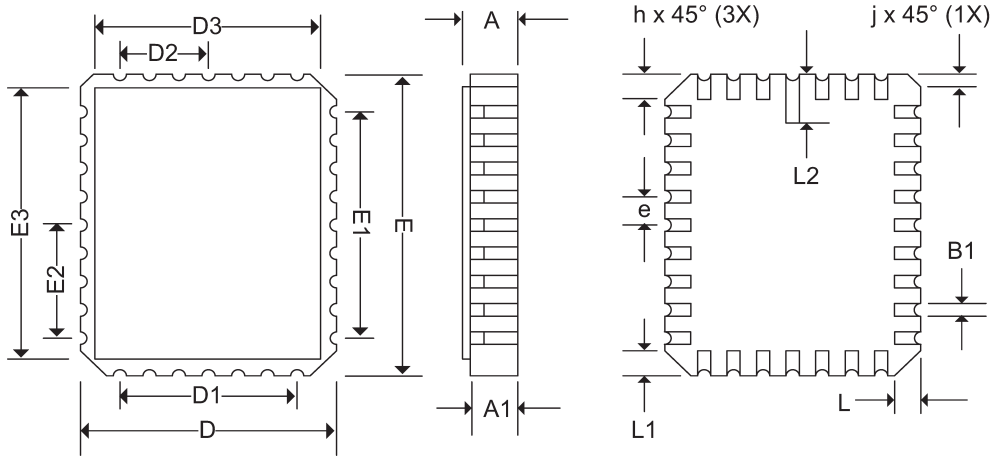
2-SIDED LEADLESS CHIP CARRIER

Pkg #	L1	
# Pins	32	
Symbol	**Min**	**Max**
A	0.080	0.100
b	0.022	0.028
b1	0.006	0.022
b2	0.040	-
D	0.820	0.840
E	0.392	0.400
e	0.050 BSC	
h	0.012 REF	
L	0.070	0.080
L1	0.090	0.110
L2	0.003	0.015
N	32	



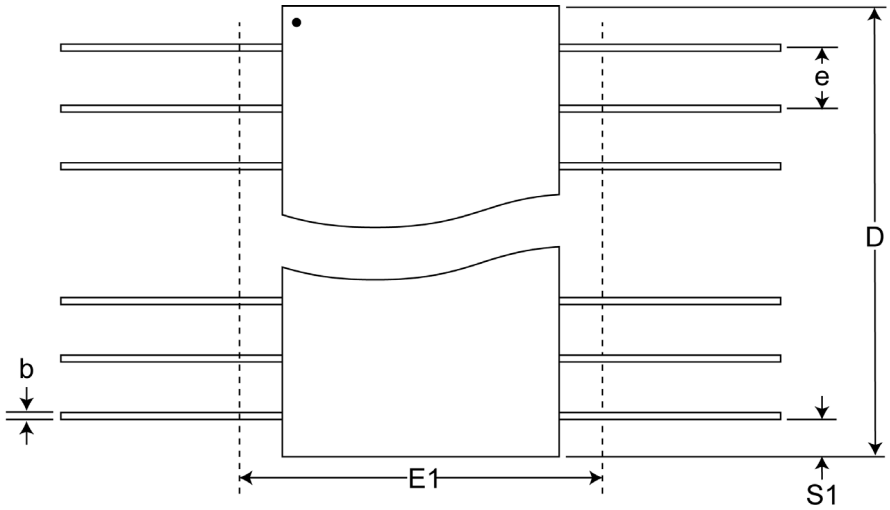
RECTANGULAR LEADLESS CHIP CARRIER

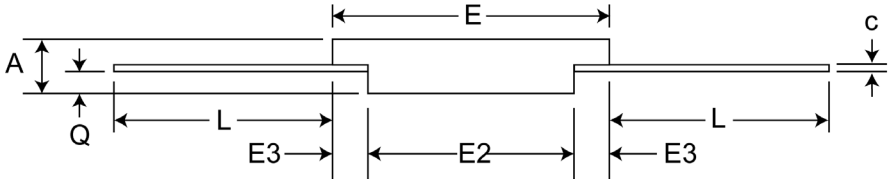
Pkg #	L6	
# Pins	32	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	-	0.458
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	9	



Pkg #	FS-3	
# Pins	32	
Symbol	**Min**	**Max**
A	0.097	0.125
b	0.015	0.019
c	0.003	0.009
D	-	0.830
E	0.400	0.420
E1	-	0.450
E2	0.180	-
E3	0.030	-
e	0.050 BSC	
L	0.250	0.370
Q	0.020	0.045
S	-	0.045
S1	0.000	-
M	-	0.002
N	32	

SOLDER SEAL FLAT PACKAGE





Pkg #	P600	
# Pins	32 (600 mil)	
Symbol	**Min**	**Max**
A	0.160	0.200
A1	0.015	-
b	0.014	0.023
b2	0.045	0.070
C	0.006	0.014
D	1.600	1.700
E1	0.526	0.548
E	0.590	0.610
e	0.100 BSC	
eB	0.600 BSC	
L	0.120	0.150
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE