

**DESCRIPTION**

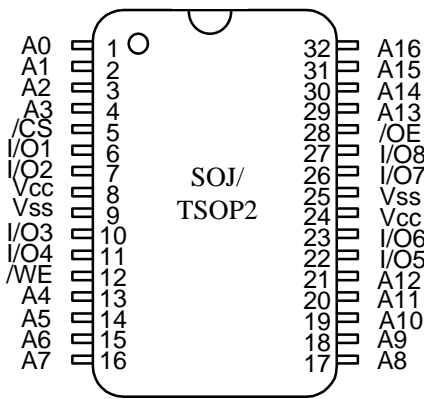
The HY63V8100A is a 1,048,576-bit high-speed, SRAM organized as 131,072 words by 8-bits. The HY63V8100A uses eight common input and output lines and has an output enable pin which operates faster than. address access time at read cycle. The device is fabricated using Hyundai's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications

**FEATURES**

- Single 3.3V ± 0.3V Power Supply
- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Low data Retention Voltage:  
 - 2.0V(min) – L-ver. Only
- Center Power/Ground Pin Configuration
- Standard pin configuration  
 - 32pin 400mil SOJ/TSOP-II

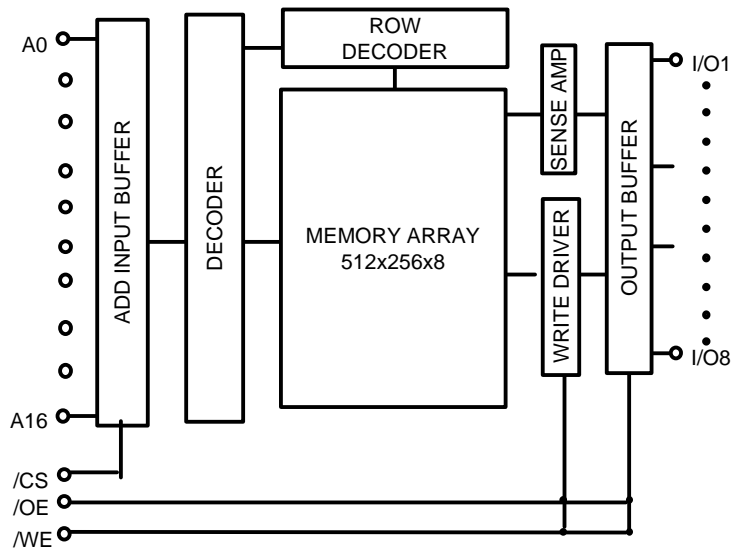
Product No.	Supply Voltage(V)	Speed (ns)	Operation Current(mA)	Standby Current(mA)	
					L
HY63V8100A	3.3	8	200	5	0.5
HY63V8100A	3.3	10	190	5	0.5
HY63V8100A	3.3	12	180	5	0.5

**PIN CONNECTION**



SOJ/TSOP2

**BLOCK DIAGRAM**



**PIN DESCRIPTION**

Pin Name	Pin Function	Pin Name	Pin Function
/CS	Chip Select	A0~A16	Address Input
/WE	Write Enable	Vcc	Power(+3.3V)
/OE	Output Enable	Vss	Ground
I/O1~I/O8	Data Inputs/Outputs	N.C	No Connection

### ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Rating	Unit
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on Any Pin Relative to V <sub>SS</sub>	-0.5 to 4.6	V
V <sub>CC</sub>	Voltage on V <sub>CC</sub> Supply Relative to V <sub>SS</sub>	-0.5 to 5.5	V
T <sub>A</sub>	Operating Temperature	Commercial	0 to 70
		Industrial	-40 to 85
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C
P <sub>D</sub>	Power Dissipation	1.0	W

Note

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS (T<sub>A</sub>=0°C to 70°C)

Symbol	Parameter	Min.	Type	Max.	Unit
V <sub>CC</sub>	Supply Voltage	3.0	3.3	3.6	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>CC</sub> +0.3(2)	V
V <sub>IL</sub>	Input Low Voltage	-0.3(1)	-	0.8	V

Note

1. V<sub>IL</sub>(min) = -2.0V a.c(pulse width less than 8ns) for I ≤ 20mA
2. V<sub>IH</sub>(max) = V<sub>CC</sub> + 2.0V a.c(pulse width less than 8ns) for I ≤ 20mA

### DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 3.3V±0.3V, T<sub>A</sub> = 0°C to 70°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
I <sub>LI</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-2	-	2	uA	
I <sub>LO</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , /CS = V <sub>IH</sub> or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub>	-2	-	2	uA	
I <sub>CC</sub>	Operating Current	/CS = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> , I <sub>I/O</sub> = 0mA Min. Duty Cycle = 100%	8ns	-	-	200	mA
			10ns	-	-	190	mA
			12ns	-	-	180	mA
I <sub>SB</sub>	TTL Standby Current (TTL Inputs)	/CS = V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> Min. Cycle	-	-	60	mA	
I <sub>SB1</sub>	CMOS Standby Current (CMOS Inputs)	/CS ≥ V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V		-	-	5	mA
			L	-	-	0.5	mA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8.0mA	-	-	0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4.0mA	2.4	-	-	V	

Note : Typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C

**AC CHARACTERISTICS**

 (V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>A</sub> = 0°C to 70°C, unless otherwise specified.)

#	Symbol	Parameter	8ns		10ns		12ns		Unit
			Min	Max	Min	Max	Min	Max	
<b>READ CYCLE</b>									
1	t <sub>RC</sub>	Read Cycle Time	8	-	10	-	12	-	ns
2	t <sub>AA</sub>	Address Access Time	-	8	-	10	-	12	ns
3	t <sub>ACS</sub>	Chip Select Access Time	-	8	-	10	-	12	ns
4	t <sub>OE</sub>	Output Enable to Output Valid	-	4	-	5	-	6	ns
5	t <sub>CLZ</sub>	Chip Select to Output in Low Z	3	-	3	-	3	-	ns
6	t <sub>OLZ</sub>	Output Enable to Output in Low Z	0	-	0	-	0	-	ns
7	t <sub>CHZ</sub>	Chip Deselecting to Output in High Z	0	5	0	5	0	6	ns
8	t <sub>OHZ</sub>	Out Disable to Output in High Z	0	5	0	5	0	6	ns
9	t <sub>OH</sub>	Output Hold from Address Change	3	-	3	-	3	-	ns
<b>WRITE CYCLE</b>									
10	t <sub>WC</sub>	Write Cycle Time	8	-	10	-	12	-	ns
11	t <sub>CW</sub>	Chip Select to End of Write	6	-	7	-	8	-	ns
12	t <sub>AW</sub>	Address Valid to End of Write	6	-	7	-	8	-	ns
13	t <sub>AS</sub>	Address Set-up Time	0	-	0	-	0	-	ns
14	t <sub>WP</sub>	Write Pulse Width(/OE High)	6	-	7	-	8	-	ns
15	t <sub>WP1</sub>	Write Pulse Width(/OE Low)	8	-	10	-	12	-	ns
16	t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	ns
17	t <sub>WHZ</sub>	Write to Output in High Z	0	4	0	5	0	6	ns
18	t <sub>DW</sub>	Data to Write Time Overlap	4	-	5	-	6	-	ns
19	t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	0	-	ns
20	t <sub>OW</sub>	Output Active from End of Write	3	-	3	-	3	-	ns

NOTE : Above parameters are also guaranteed at industrial temperature range.

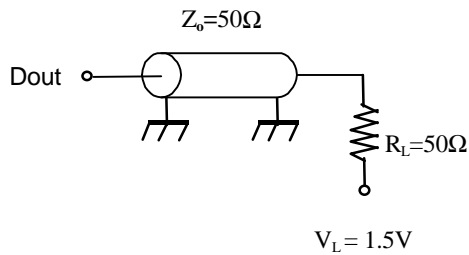
### AC TEST CONDITIONS

(V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>A</sub> = 0°C to 70°C, unless otherwise specified.)

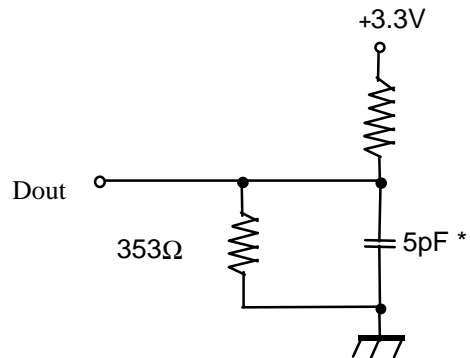
Parameter	Value
Input Pulse Level	0V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Level	1.5V
Output Load	See below

### AC TEST CONDITIONS

Output Load (A)



Output Load (B)  
(for t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OHZ</sub>, t<sub>OLZ</sub>, t<sub>WHZ</sub> & t<sub>OW</sub>)



Note : \*Including jig and scope capacitance

### CAPACITANCE

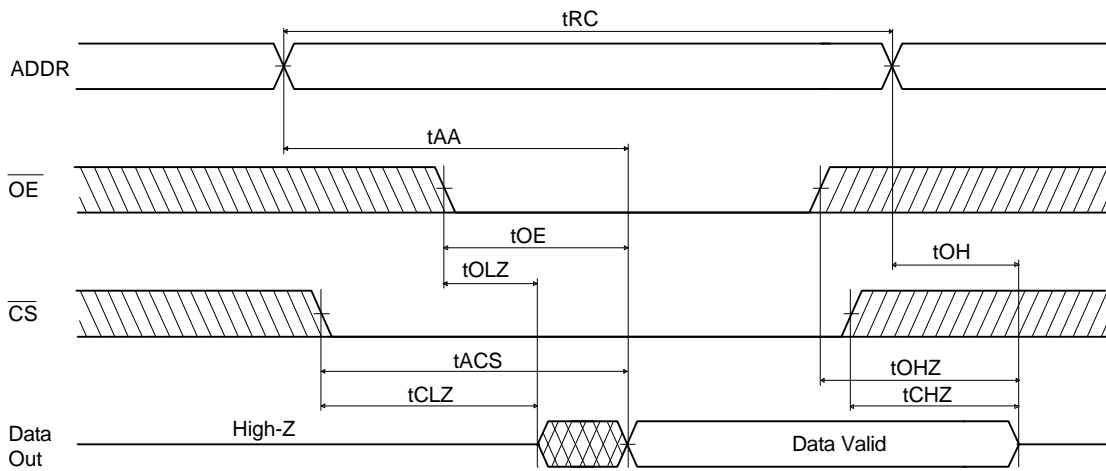
Temp = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	7	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>I/O</sub> = 0V	8	pF

Note : This parameter is sampled and not 100% tested

**TIMING DIAGRAM**

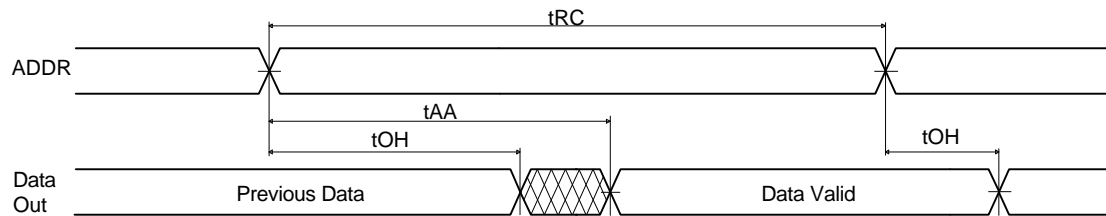
**READ CYCLE 1**



**Note (Read Cycle)**

1.  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{CHZ}$  max. is less than  $t_{CLZ}$  min. both for a given device and from device to device.
3.  $\overline{WE}$  is high for read cycle.

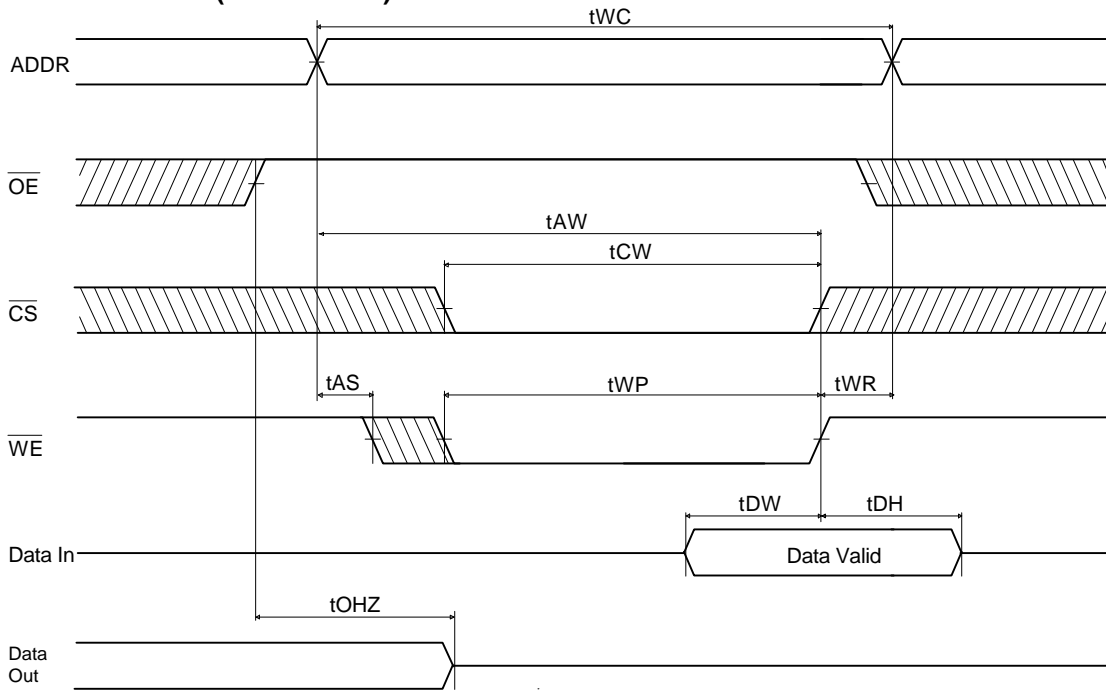
**READ CYCLE 2**



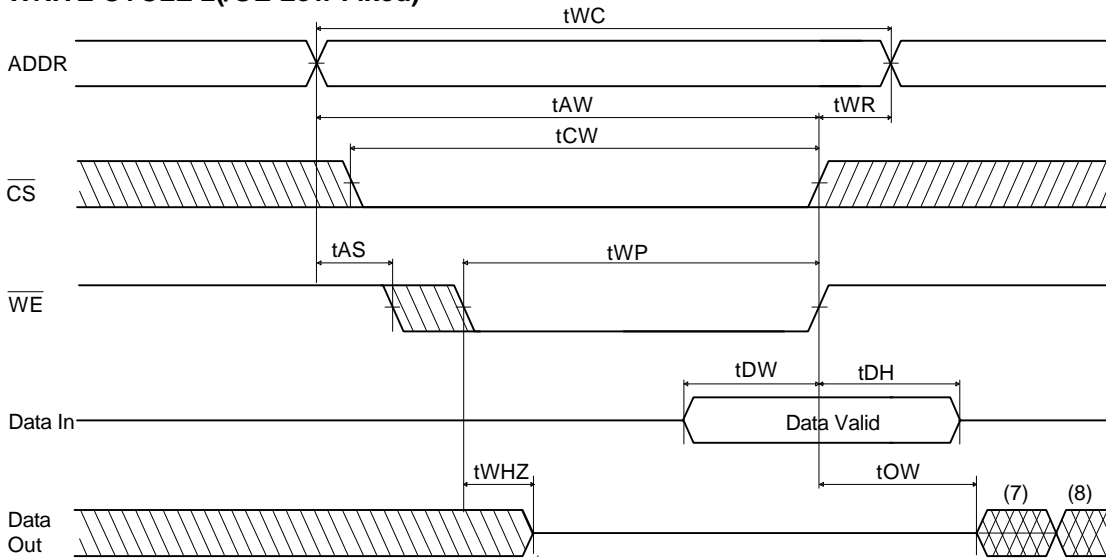
**Note (Read Cycle)**

1.  $\overline{WE}$  is high for read cycle.
2. Device is continuously selected  $\overline{CS}=V_{IL}$ .
3.  $\overline{OE}=V_{IL}$ .

**WRITE CYCLE 1(/OE Clocked)**



**WRITE CYCLE 2(/OE Low Fixed)**



**Notes(Write Cycle)**

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low, and /WE going low : A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS or /WE going high.
5. If /OE and /WE are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of latest written data in the write cycle.
8. DOUT is the read data of the new address.

### FUNCTIONAL DESCRIPTION

/CS	/WE	/OE	/LB	/UB	MODE	I/O Pin		Supply Current
						I/O1 - I/O8	I/O9 - I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	I <sub>sb</sub> , I <sub>sb1</sub>
L	H	H	X	X	Output Disable	High-Z	High-Z	I <sub>cc</sub>
L	X	X	H	H				
L	H	L	L	H	Read	Dout	High-Z	I <sub>cc</sub>
			H	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	X	L	H	Write	Din	High-Z	I <sub>cc</sub>
			H	L		High-Z	Din	
			L	L		Din	Din	

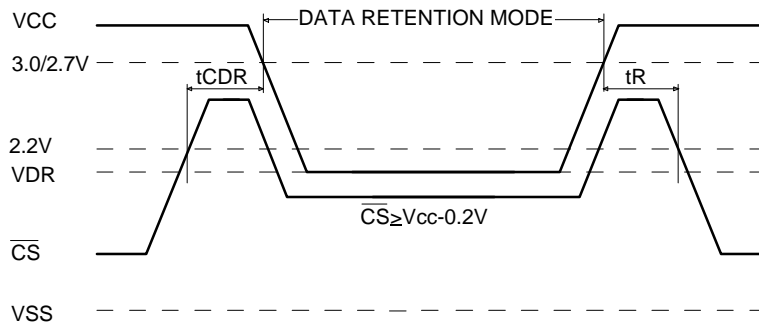
\* NOTE : X means Don,t Care

### DATA RETENTION ELECTRIC CHARATERISTIC

(TA = 0°C to 70°C)

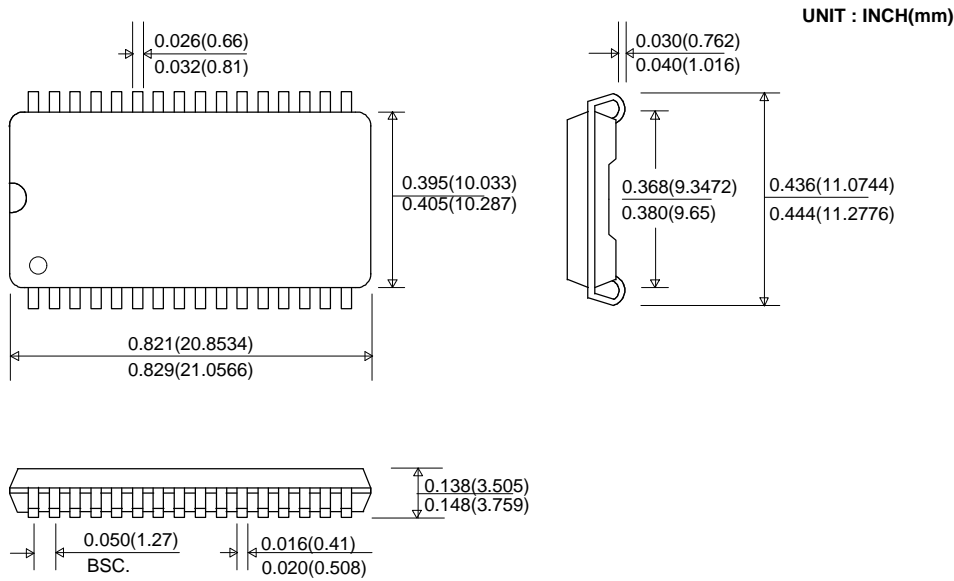
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDR	V <sub>cc</sub> for Data Retention	/CS ≥ V <sub>cc</sub> - 0.2V	2.0	-	3.6	V
IDR	Data Retention Current	V <sub>cc</sub> = 3.0V, /CS ≥ V <sub>cc</sub> - 0.2V V <sub>in</sub> ≥ V <sub>cc</sub> - 0.2V or ≤ 2.0V	-	-	0.9	mA
		V <sub>cc</sub> = 2.0V, /CS ≥ V <sub>cc</sub> - 0.2V V <sub>in</sub> ≥ V <sub>cc</sub> - 0.2V or ≤ 2.0V	-	-	0.7	
tCDR	Data Retention Set-Up Time		0	-	-	ns
tR	Recovery Time		5	-	-	ms

### DATA RETENTION TIMING DIAGRAM



**PACKAGE INFORMATION**

**32pin 400mil Small Outline J-Form Package (J)**



**32pin 400mil Thin Small Outline Package (T2)**

