DESCRIPTION

The HY62V256 is a high-speed, low power and 32,768 x 8-bits CMOS Static Random Access Memory fabricated using Hyundai's high performance twin tub CMOS process technology. The HY62V256 has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt. Using the CMOS technology, supply voltages from 2.0 to 5.5 volt has little effect on supply current in the data retention mode.The HY62V256 is suitable for use in low voltage (3.3V) operation and battery back-up applications.

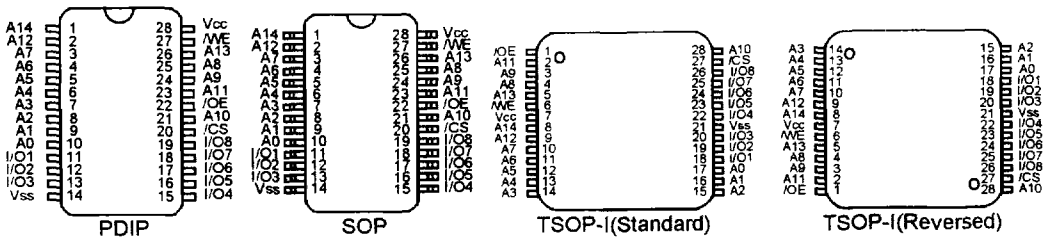
FEATURES

- Fully static operation and Tri-state output
- *TTL compatible inputs and outputs*
- Low power consumption
- Battery backup
  - 2.0V(min.) data retention
- Tri-state output
- Standard pin configuration
  - 28 pin 600 mil PDIP
  - 28 pin 330 mil SOP
  - 28 pin 8x13.4 mm TSOP-I (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)	Temperature (℃)
HY62V256A	3.3	100/120/150	25	15	0~70(Normal)
HY62V256A-I	3.3	100/120/150	25	25	-40~85(E.T.)

Note 1. E.T. : Extended Temperature, Normal : Normal Temperature
2. Current value is max.

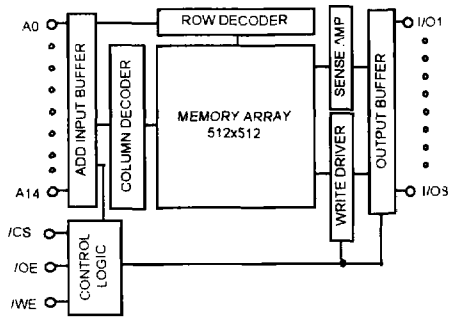
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(+3.3V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Package	Package
HY62V256LP	100/120/150		PDIP
HY62V256LJ	100/120/150		SOP
HY62V256LT1	100/120/150		TSOP-I Standard
HY62V256LR1	100/120/150		TSOP-I Reversed
HY62V256LP-I	100/120/150	E.T.	PDIP
HY62V256LJ-I	100/120/150	E.T.	SOP
HY62V256LT1-I	100/120/150	E.T.	TSOP-I Standard
HY62V256LR1-I	100/120/150	E.T.	TSOP-I Reversed

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	-0.5 to 4.6	V
T_A	Operating Temperature	0 to 70	℃
T_{STG}	Storage Temperature	-65 to 150	℃
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260 • 10	℃•sec

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

T_A=0°C to 70°C(Normal)/ -40°C to 85°C(E.T.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	-	0.4	V

Note
1. V_{IL} = -3.0V for pulse width less than 30ns

TRUTH TABLE

/CS	/WE	/OE	MODE	I/O OPERATION
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note
1. H=V_{IH}, L=V_{IL}, X=Don't Care

DC CHARACTERISTICS

V_{CC} = 3.3V±10%, T_A = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified.

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		-1	-	1	uA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		-1	-	1	uA
I_{CC}	Operating Power Supply Current	/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		-	9	25	mA
I_{CC1}	Average Operating Current	/CS = V_{IL}, Min. Duty Cycle = 100%, $I_{I/O}$ = 0mA		-	10	35	mA
I_{SB}	TTL Standby Current (TTL Inputs)	/CS= V_{IH}		-	-	0.5	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	CS ≥ Vcc-0.2V	HY62V256	-	1.5	15	uA
			HY62V256-I	-	1.5	25	uA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA		2.2	-	-	V

Note : Typical values are at T_A = 25℃

AC CHARACTERISTICS

V_{CC} = 3.3V±10%, T_A = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified.

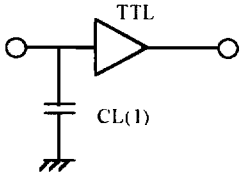
#	Symbol	Parameter	-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	100	-	120	-	150	-	ns
2	tAA	Address Access Time	-	100	-	120	-	150	ns
3	tACS	Chip Select Access Time	-	100	-	120	-	150	ns
4	tOE	Output Enable to Output Valid	-	50	-	55	-	75	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	10	-	10	-	10	-	ns
7	tCHZ	Chip Disable to Output in High Z	0	35	0	40	0	50	ns
8	tOHZ	Out Disable to Output in High Z	0	35	0	40	0	50	ns
9	tOH	Output Hold from Address Change	10	-	20	-	20	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	100	-	120	-	150	-	ns
11	tCW	Chip Selection to End of Write	100	-	110	-	120	-	ns
12	tAW	Address Valid to End of Write	100	-	110	-	120	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	60	-	70	-	100	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	35	0	40	0	50	ns
17	tDW	Data to Write Time Overlap	45	-	50	-	50	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	20	-	20	-	20	-	ns

AC TEST CONDITIONS

T_A = 0℃ to 70℃(Normal) / -40℃ to 85℃(E.T.) unless otherwise specified.

PARAMETER	VALUE
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 100pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

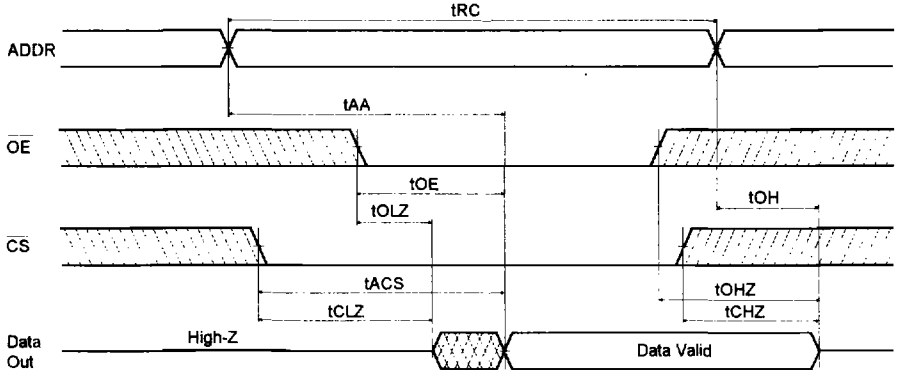
T_A = 25℃, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : These parameters are sampled and not 100% tested

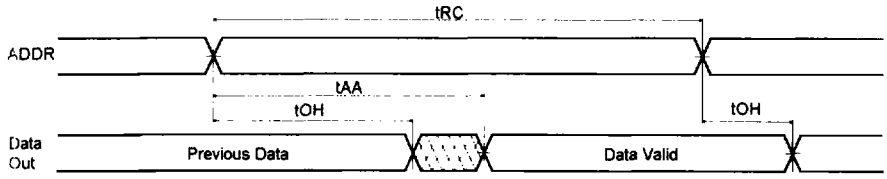
TIMING DIAGRAM

READ CYCLE 1



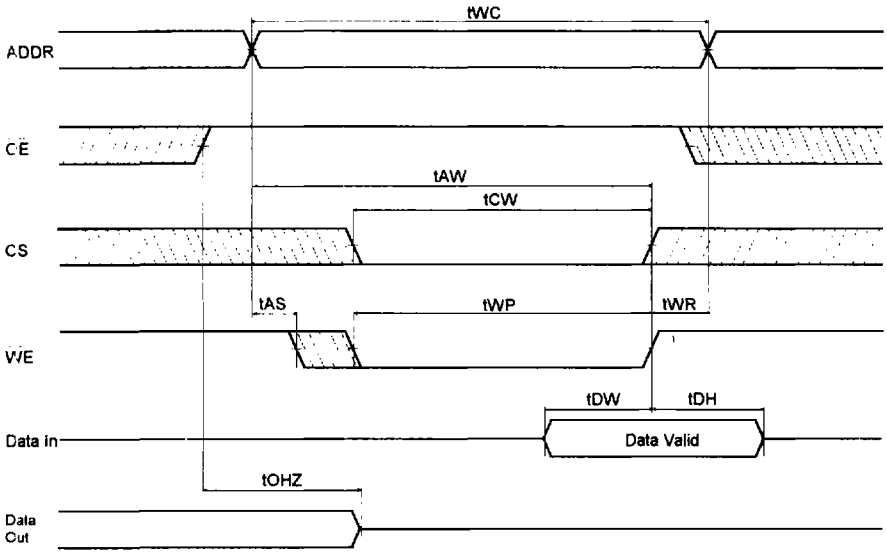
Note(READ CYCLE):
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. /WE is high for the read cycle.

READ CYCLE 2

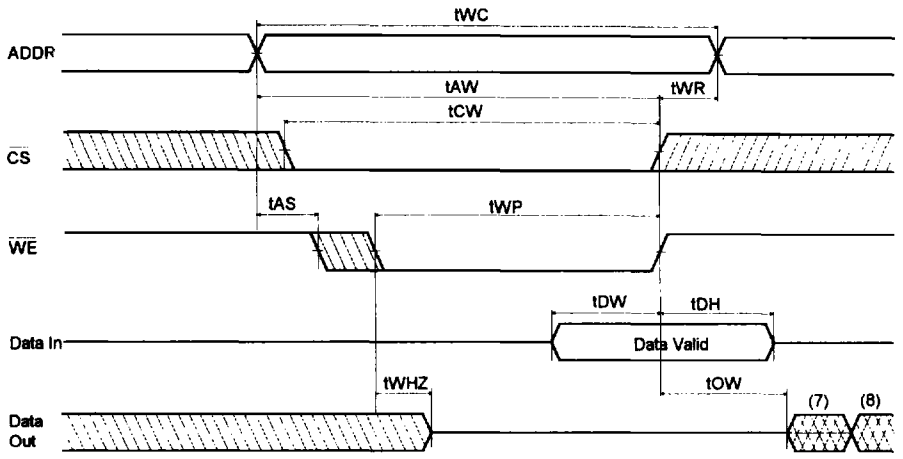


Note(READ CYCLE):
1. /WE is high for the read cycle.
2. Device is continuously selected /CS= V_{IL}.
3. /OE =V_{IL}.

WRITE CYCLE 1(/OE Clocked)



WRITE CYCLE 2 (/OE Low Fixed)



Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tRW is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of the latest written data in this write cycle.
8. DOUT is the read data of the new address.

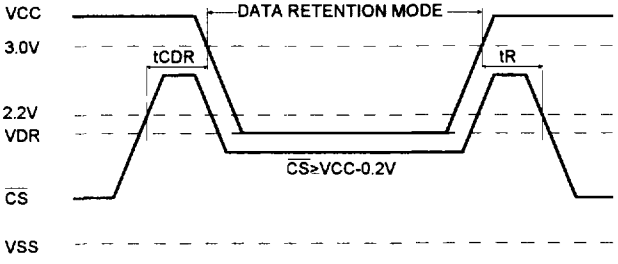
DATA RETENTION CHARACTERISTICS

TA=0°C to 70°C (normal)/ -40°C to 85°C(E.T.)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DR}	Vcc for Data Retention	/CS ≥ Vcc-0.2V, Vss ≤ V_{IN} ≤ Vcc	2	-	-	V
I_{CCDR}	Data Retention Current	Vcc = 3.0V, /CS ≥ Vcc-0.2V, Vss ≤ V_{IN} ≤ Vcc	-	1	15(2)	uA
tCDR	Chip Disable to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
tR	Operating Recovery Time		tRC(3)	-	-	ns

Notes
1. Typical values are under the condition of T_A = 25℃.
2. 3uA max. at T_A=0℃ to 40 ℃.
3. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM

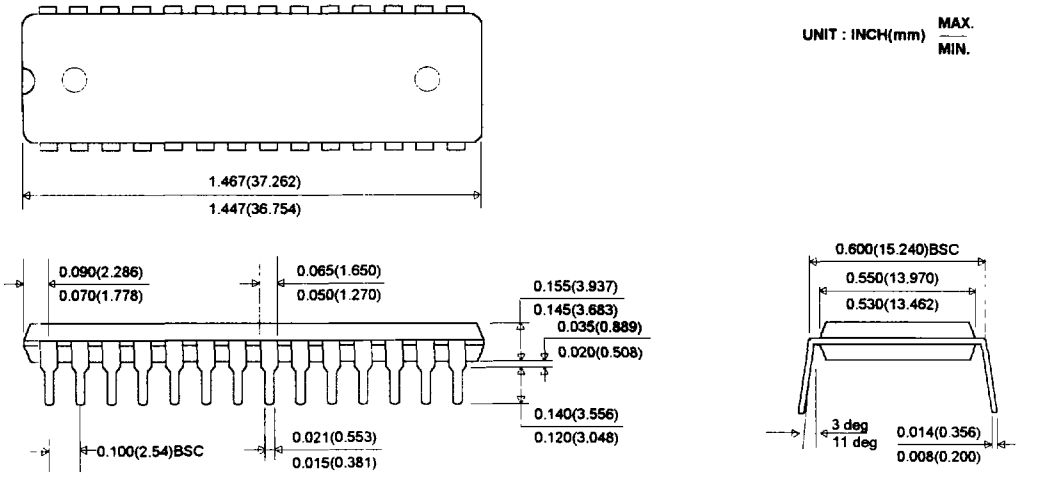


RELIABILITY SPEC.

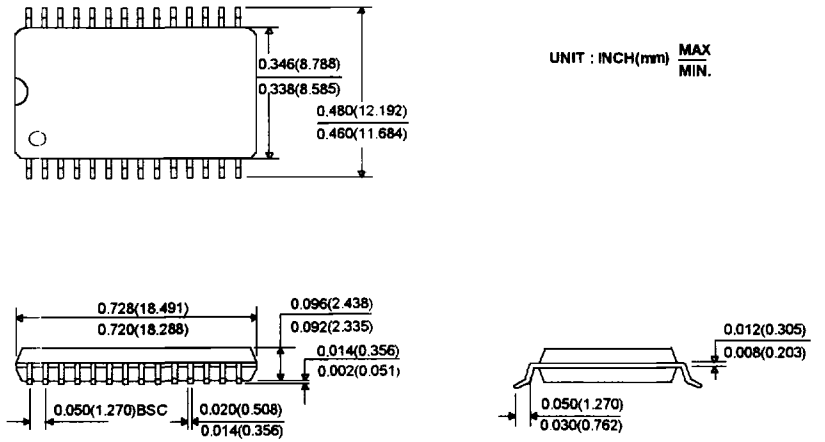
TEST MODE		TEST SPEC.
ESD	HBM	≥ 2000V
	MM	≥ 250V
LATCH - UP		≤ -100mA
		≥ 100mA

PACKAGE INFORMATION

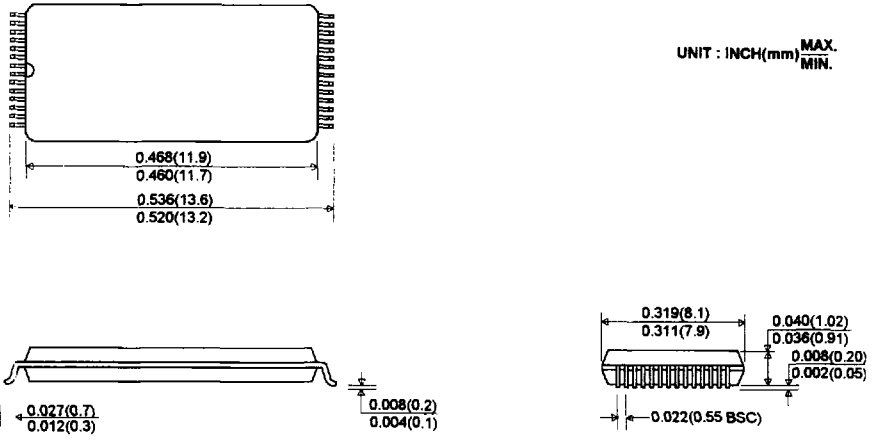
28pin 600mil Dual In-Line Package(P)



28pin 330mil Small Outline Package(J)



28pin 8x13.4mm Thin Small Outline Package Standard(T1)



28pin 8x13.4mm Thin Small Outline Package Reversed(R1)