SGS-THOMSON MICROELECTRONICS

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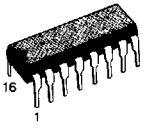
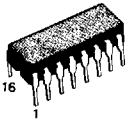
M54HC259
M74HC259

8 BIT ADDRESSABLE LATCH

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS259



B1N
Plastic Package



F1
Ceramic Frit Seal Package

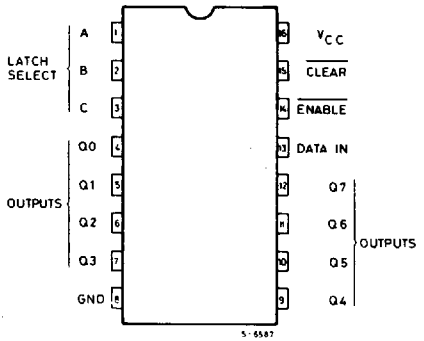
M1
Micro Package

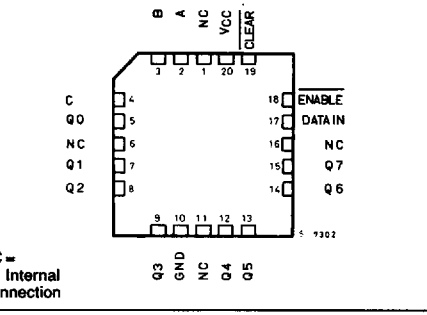
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC259 F1
M74HC259 B1N
M74HC259 F1
M74HC259 C1
M74HC259 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

The M54/74HC259 is a high speed CMOS 8 BIT ADDRESSABLE LATCH fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M54HC259/M74HC259 has single data input (D) 8 latch outupts (Q0-Q7), 3 address inputs (A, B, and C), common enable input (E), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken low the data flows through to the addresses output. The data is stored on the positive-going edge of the ENABLE pulse. All unaddressed latches will remain unaffected. With ENABLE in the high state the device is deselected and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the ENABLE should be held high (inactive) while the address lines are changing. If ENABLE is held high and CLEAR is taken low all eight latches are cleared to the low state. If ENABLE is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to 8 line decoder.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

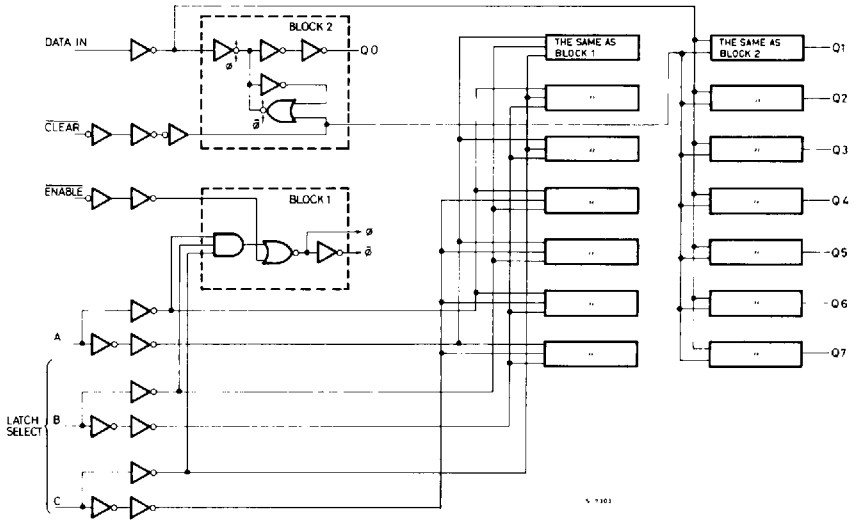
TRUTH TABLE

INPUTS		OUTPUTS OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{G}$			
H	L	D	Qi0	ADDRESSABLE LATCH
H	H	Qi0	Qi0	MEMORY
L	L	D	L	8-LINE DEMULTIPLEXER
L	H	L	L	CLEAR ALL BITS TO 'L'

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D: THE LEVEL AT THE DATA INPUT
Qi0: THE LEVEL BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED, (i = 0,1,.....,7).

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

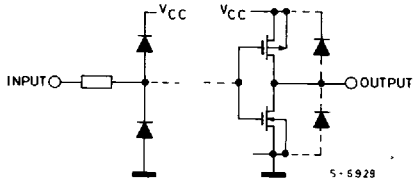
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

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Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - QN)		13	21	ns
t_{PLH} t_{PHL}	Propagation Delay Time (ADD - QN)		21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time (EN - QN)		18	29	ns
t_{PHL}	Propagation Delay Time (CL - QN)		14	23	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$) S G S-THOMSON

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	22	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - QN)	2.0		—	73	130	—	165		195	ns
		4.5		—	16	26	—	33		39	
		6.0		—	14	22	—	28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (ADD - QN)	2.0		—	115	190	—	240		285	ns
		4.5		—	24	38	—	48		57	
		6.0		—	21	32	—	41		48	
t_{PLH} t_{PHL}	Propagation Delay Time (EN - QN)	2.0		—	100	165	—	205		250	ns
		4.5		—	21	33	—	41		50	
		6.0		—	18	28	—	35		43	
t_{PHL}	Propagation Delay Time (CL - QN)	2.0		—	80	135	—	170		205	ns
		4.5		—	17	27	—	34		41	
		6.0		—	15	23	—	29		35	
$t_{W(L)}$	Minimum Pulse Width (CL)	2.0		—	33	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width (EN)	2.0		—	35	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time (DATA)	2.0		—	15	50	—	65		75	ns
		4.5		—	3	10	—	13		15	
		6.0		—	3	9	—	11		13	
t_s	Minimum Set-up Time (ADD)	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
t_h	Minimum Hold Time (DATA)	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
t_h	Minimum Hold Time (ADD)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	73	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

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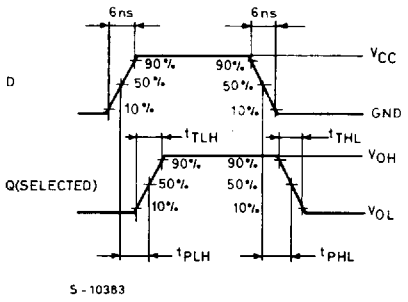
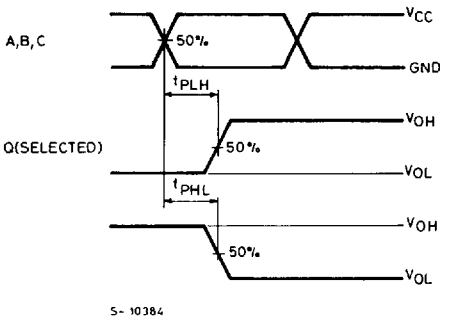
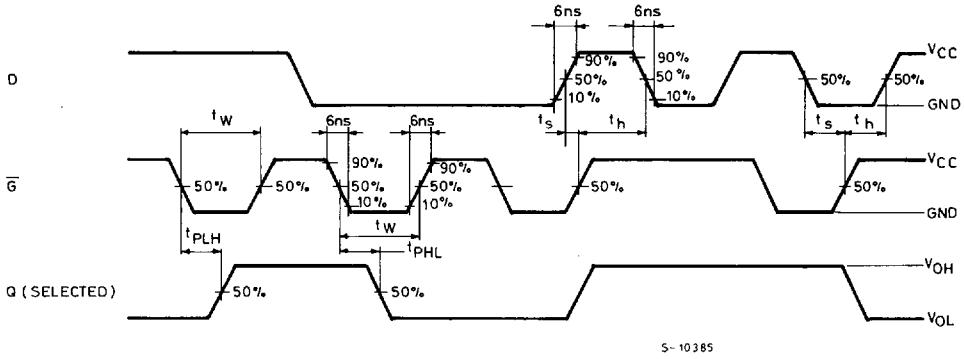
WAVEFORM 1. ($\overline{G}$ = L, $\overline{CLR}$ = H, A ~ C = STABLE)



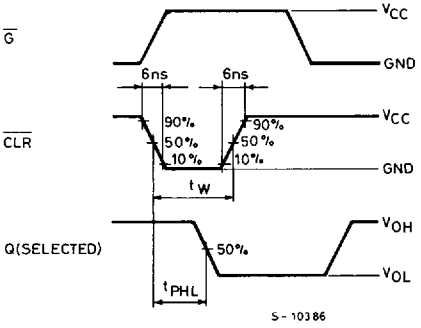
WAVEFORM 2. ($\overline{G}$ = L)



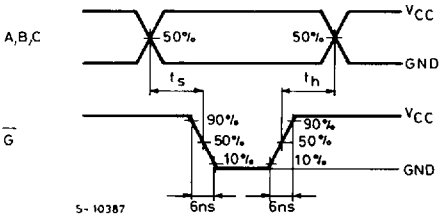
WAVEFORM 3. ($\overline{CLR}$ = H, A ~ C = STABLE)



WAVEFORM 4. (D = H, A ~ C-STABLE)



WAVEFORM 5. ($\overline{CLR}$ = H)



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TEST CIRCUIT I_{CC} (Opr.)