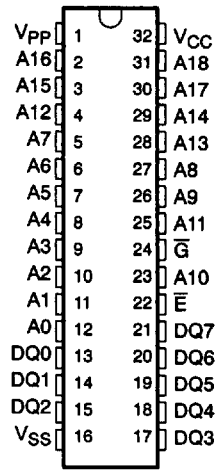
TMS28F040
4 194 304-BIT FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY

SMJS040–DECEMBER 1992

- **Organization . . . 512K × 8**
- **Separately Erasable 32K Byte Blocks**
- **Two Power Supplies (5 V and 12 V)**
- **100% TTL-Level Control Inputs**
- **Fully Automated On-Chip Erase and Byte Program Operations**
- **RAM-Like Write Setup/Read Timings for Standard Processor Interface**
- **10 000, 1000, and 100 Program/Erase Cycle Versions**
- **Automotive Temperature Range: – 40°C to 125°C**
- **Low Power Dissipation (V_{CC} = 5.50 V)**
  - **Active Write . . . 55 mW**
  - **Active Read . . . 165 mW**
  - **Electrical Erase . . . 82.5 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Pin Compatible With Existing 4-Megabit EPROMS**
- **All Inputs/Outputs TTL Compatible**
- **Chip Erase Before Reprogramming**

N PACKAGE†
(TOP VIEW)



† The package is shown for pinout reference only.

PIN NOMENCLATURE	
A0–A18	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0–DQ7	Data In/Data Out
NC	No Internal Connection
V_{PP}	12-V Power Supply
V_{CC}	5-V Power Supply
V_{SS}	Ground

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description

The TMS28F040 is a 4 194 304 bit, programmable read-only memory that can be electrically erased (bulk-erased and block-erased) and re-programmed. This device is offered in 32-pin plastic DIP and 40-pin TSOP packages. The TMS28F040 is organized as 16 independent 32K byte blocks. Blocks may be dynamically marked read-only by configuring soft protection registers with command sequences. Embedded byte write and chip/block erase functions are fully automated by an on-chip write state machine (WSM), thus releasing the system processor for other tasks. A suspend/resume feature allows access to unaltered memory blocks during erase operations.

The TMS28F040 Flash EEPROM is offered in a dual in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2 mm (600-mil) centers, a 40-lead thin small outline package (DD suffix), and reverse pinout TSOP package (DU suffix). The TMS28F040 is offered with two choices of temperature ranges of 0°C to 70°C (NL, DDL, and DUL suffixes) and – 40°C to 125°C (NQ, DDQ, and DUQ suffixes).

operation

Device operations are selected by writing JEDEC standard commands with conventional microprocessor timings into a command register through the I/O pins (DQ0–DQ7) while $V_{PP} = V_{PPH}$. The device is always in the read-only mode when $V_{PP} = V_{PPL}$. The content of the command register acts as input to an on-chip state machine. The command register latches commands as issued by system software and is not altered by write state machine (WSM) actions. It defaults to read array mode upon initial power-up. With an appropriate command written to the command register, standard processor accesses output stored data, device/mfg codes, or output status of program/erase operations for validation. The functions associated with altering memory contents are program, erase, protection, and status. These functions are accessed via the command register and validated through the status register. The signature register may be accessed while $V_{PP} \leq V_{PPH}$ by applying $A9 = V_{ID}$. High voltage (V_{PPH}) on V_{PP} enables device erasure and programming.

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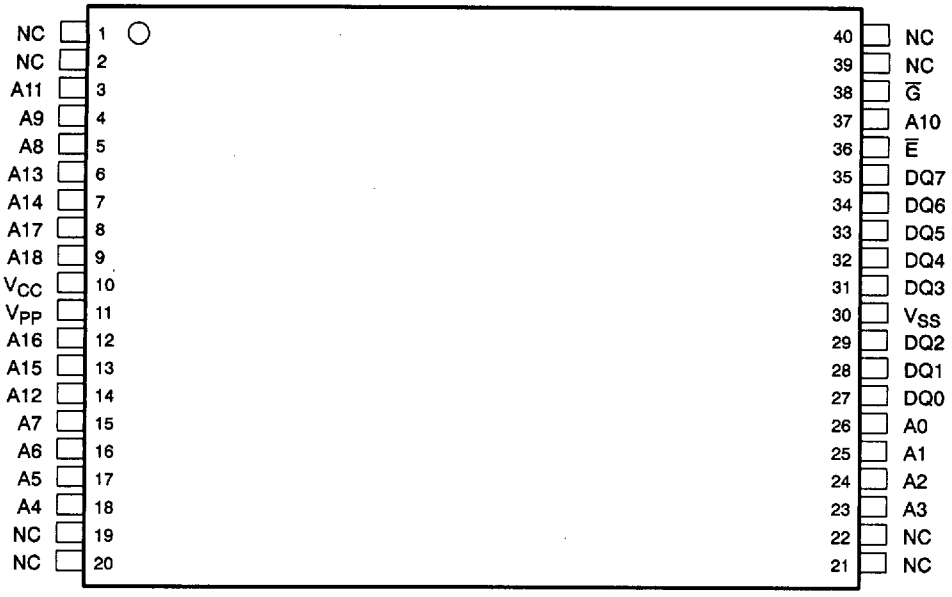
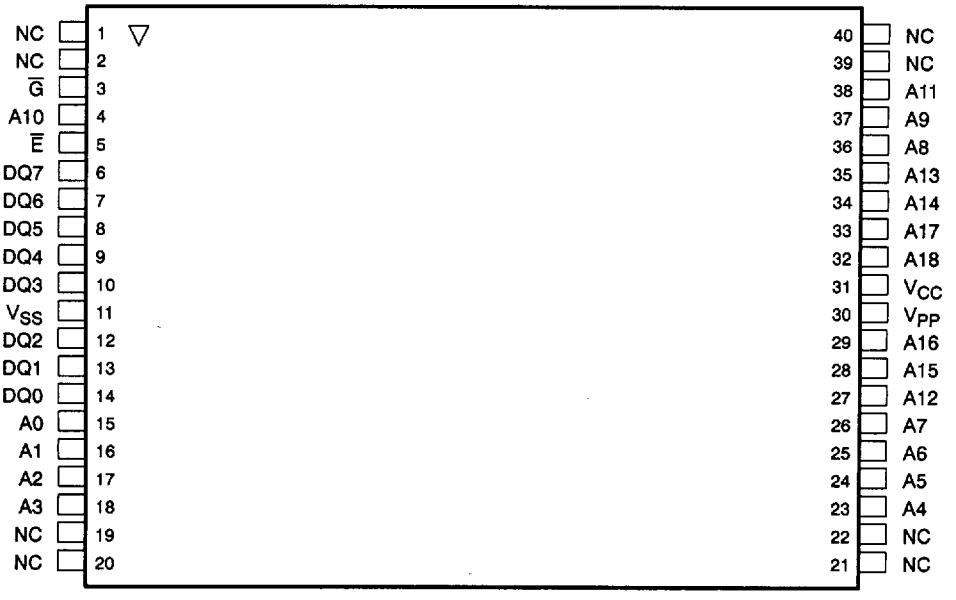
DD PACKAGE†
(TOP VIEW)



DU PACKAGE†
REVERSE PINOUT
(TOP VIEW)



† The package shown is for pinout reference only.

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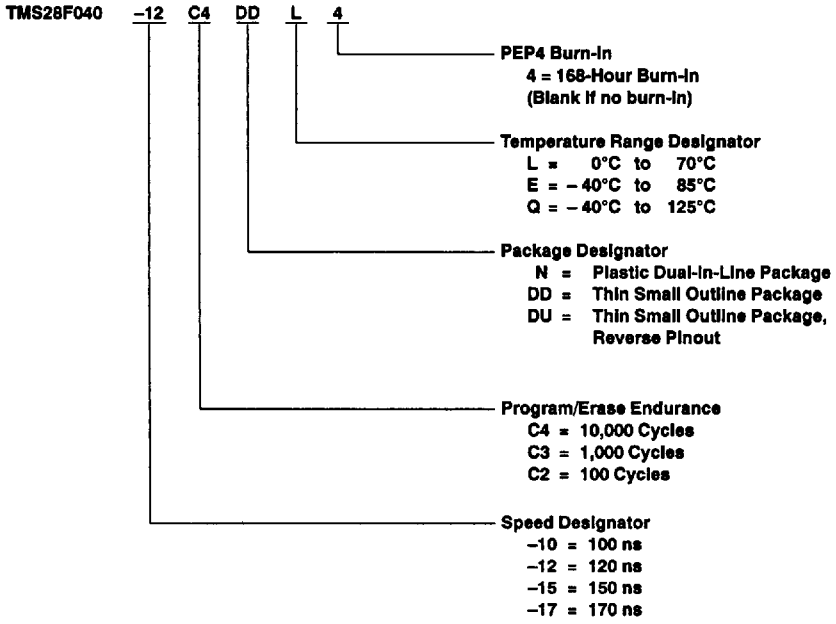
device symbol nomenclature



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functional block diagram

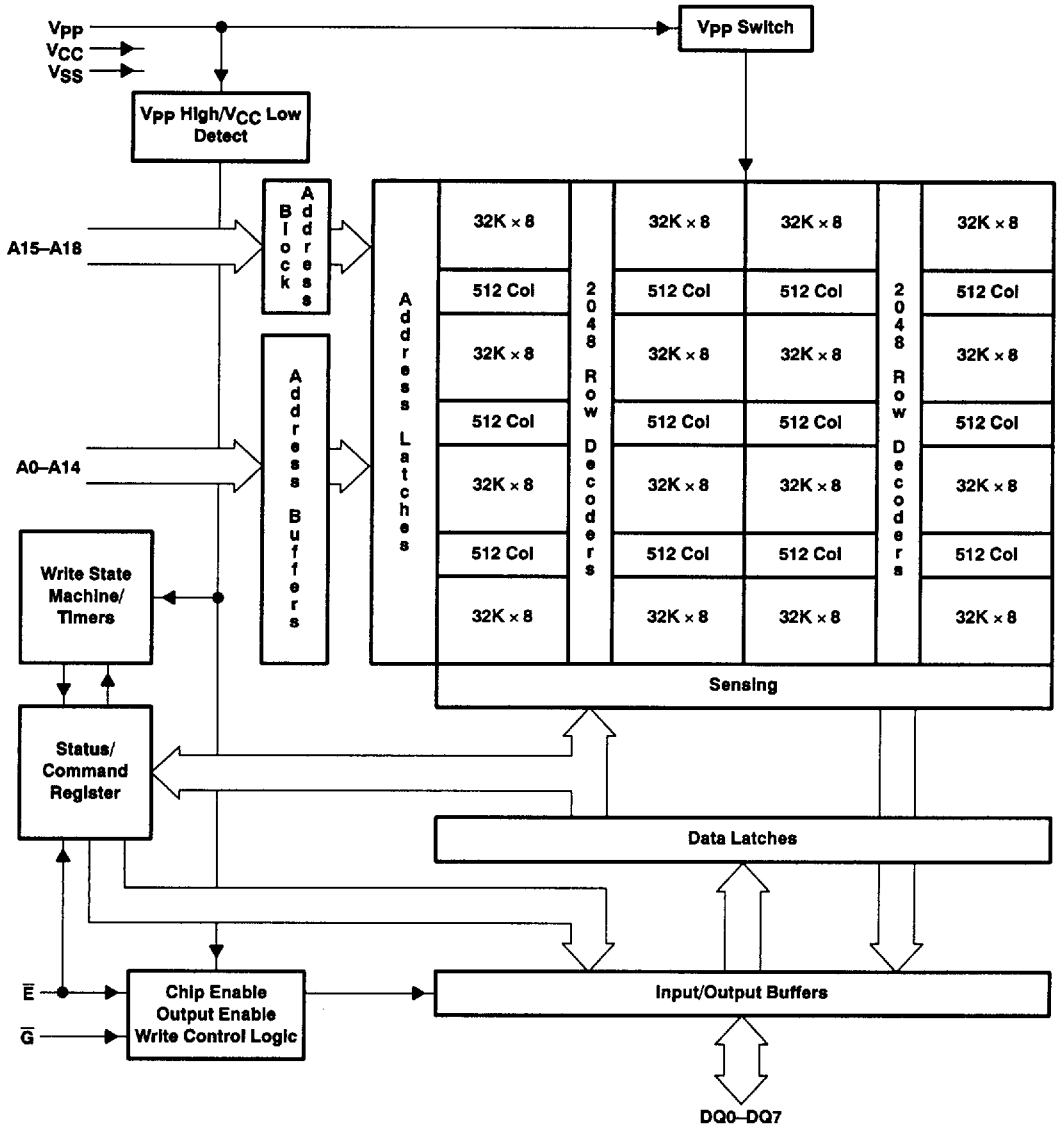

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Table 1. Operation Modes

MODE	$\overline{E}$	$\overline{G}$	V_{PP}	A9	A0	DQ0–DQ7
Read-Only	V_{IL}	V_{IL}	V_{PPL}	X	X	DOUT
Read	V_{IL}	V_{IL}	X	X	X	DOUT
Output Disable	V_{IL}	V_{IH}	V_{PPL}	X	X	High-Z
Standby	V_{IH}	X	X	X	X	High-Z
Signature (Mfr)	V_{IL}	V_{IL}	X	V_{ID}	V_{IL}	97h
Signature (Device)	V_{IL}	V_{IL}	X	V_{ID}	V_{IH}	79h
Write	V_{IL}	V_{IH}	V_{PPH}	X	X	DIN

NOTES: 1. X can be V_{IL} or V_{IH} for control pins or addresses, and V_{PPL} or V_{PPH} for V_{PP}.
2. Write/Erase operations will continue during standby until completed.
3. Block erase, chip erase, and byte programming commands are assured only when $V_{PP} = V_{PPH}$.

access modes

The TMS28F040 is configured as read-only while $V_{PP} = V_{PPL}$. Commands to initiate status reads and program/erase operation are possible with $V_{PP} = V_{PPH}$. The memory address space consists of sixteen 32K × 8-bit blocks indexed by address inputs A15–A18.

read access

While $V_{PP} = V_{PPL}$, the TMS28F040 is configured for read-only access; program and erase operations are not available. When $V_{PP} = V_{PPH}$, a read cycle must assert $\overline{G}$ low with $\overline{E} = V_{IL}$. Hardware signature read is always available.

write access

Write access is available when $V_{PP} = V_{PPH}$. Commands, data, and addresses are latched by the TMS28F040 using the $\overline{E}$ input. A write cycle is defined as $\overline{E}$ switching low with $\overline{G}$ high and $V_{PP} = V_{PPH}$. Command or program data are latched on the rising edge of $\overline{E}$. Addresses are latched on the falling edge of $\overline{E}$. Software signature, status, polling, suspend/resume, and program/erase commands are functional during write access.

read modes

The TMS28F040 always operates in one of three read modes. The read mode is latched by writing an initiation command and remains latched regardless of subsequent program and erase operations. Only the read memory mode is available when $V_{PP}=V_{PPL}$.

read memory data/poll bits

Upon initial power up, the device defaults to the read memory mode. This mode can also be set at any time by writing either of the commands FFh or 00h. The mode remains latched until one of the other two read modes is initiated. The read array commands are functional when $V_{PP}=V_{PPL}$ or V_{PPH}.

The data available while in the read memory mode, when $V_{PP}=V_{PPH}$, is dependent on the state of the write state machine. If the WSM is not performing a program or erase operation, the standard processor read cycles simply retrieve the array data. If the WSM is busy, the system processor may read the data poll bit (DQ7) and the toggle bit (DQ6) to test for operation progress and completion. The behavior of these bits is described in a later section.

read status register

The device contains a status register than can be read to determine the status of the automated program/erase operations. This register is read by writing the command 70h. Following the write command 70h, all subsequent read cycles output data from the status register until one of the other two read modes is initiated. The status register is updated automatically by the write state machine. The purpose and behavior of the bits of the status register are described in a separate section. The read status register command is functional when $V_{PP}=V_{PPH}$.

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read signature mode

The signature operation outputs the manufacturer code (97h) and device code (79h). This mode can be entered through either a hardware or software operation.

The read signature mode may be latched through software by writing the command 90h. Upon latching 90h, asserting A0 = V_{IL} outputs the manufacturer code, while setting A0 = V_{IH} produces the device code. This mode remains effective until one of the other two read modes is initiated. The read signature command is functional when V_{PP}=V_{PPH} and is accessible from any operating mode.

Alternatively, the hardware implementation is achieved by setting $\overline{E}$=$\overline{G}$=V_{IL}, A9=V_{ID} and A0 = V_{IL} or V_{IH}. When A0 = V_{IL}, the output represents the manufacturer code. The device code is output when A0 = V_{IH}. The hardware signature access is not latched. Once A9 returns to V_{IL} or V_{IH}, the device returns to the previously latched read mode.

standby mode

When $\overline{E}$ = V_{IH}, the device is in standby mode where much of the circuitry is disabled resulting in lower power consumption. In this mode, the output pins (DQ0–DQ7) are placed in high-impedance state irrespective of $\overline{G}$. An erase/program operation will continue during standby until completed.

output disable

When $\overline{G}$ = V_{IH} or $\overline{E}$ = V_{IH}, the device outputs are disabled and the output pins (DQ0–DQ7) are placed in high-impedance state.

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write/erase modes

The TMS28F040 offers fully automated block erase, chip erase, and byte program operating modes. All pulse generation, preconditioning, and verification is handled by the on-chip write state machine. Upon initial power-up, the device defaults to reading memory data. Program and erase operations require two command cycles to initiate. Program and erase operations are accepted when V_{PP} = V_{PPH}. Attempting to initiate a program or erase operation while V_{PP} = V_{PPL} will leave the array contents unaltered. Additionally, if V_{PP} drops sufficiently below V_{PPH} during a program or erase operation, the operation will be aborted. If V_{CC} drops below V_{LKO}, any operation in progress will be aborted, new operations will be locked out, and the device will return to the read array mode. If any operation is in progress or suspended, write/erase mode commands will be ignored until the operation in progress completes.

block erase

Block erase will initialize the contents of a single unprotected block to all 1s. Block erase is initiated by the command sequence: block erase setup(20h) followed by block erase confirm(D0h). This command sequence is to ensure that memory contents are not accidentally erased. These commands are associated with a block address to be erased (A15–A18). Addresses are latched during the confirm command on the falling edge of $\overline{E}$. Command data is latched on the rising edge of $\overline{E}$. Block preconditioning, erase, and verify are handled by the write state machine, invisible to the system. Block erasure takes place when V_{PP} = V_{PPH} and V_{CC} > V_{LKO}. If the addressed block has been protected, the operation will abort with the erase status register flag SR.5 = V_{IH}.

chip erase

Chip erase is initiated by the command sequence: chip erase setup(30h) followed by chip erase confirm(30h). This command sequence is to ensure that memory contents are not accidentally erased. Command data is latched on the rising edge of $\overline{E}$. Chip erase is handled by the write state machine, invisible to the system. The chip erasure takes place only when V_{PP}=V_{PPH} and V_{CC} > V_{LKO}. Chip erase will set the memory contents of all unprotected blocks to 1s in a single erase operation. Individual blocks may be excluded from erasure by configuring the soft protection registers.

erase suspend/resume

The erase suspend command (B0h) allows interruption of a block erase operation in order to read data from an unaltered block of memory. Once the erase sequence is started, the erase suspend command (B0h) requests the write state machine to suspend the erase operation at predetermined breakpoints in the erase algorithm. The device operation status must be monitored to determine when the suspend has been executed (see related monitoring operation status section). After suspend has been granted, the read command should be written with appropriate address to read data from another block. V_{PP} is required to remain at V_{PPH} during the suspend so that the operation may be continued with a resume command. Block erase, chip erase, byte/word program, and soft protect commands are not accepted when any operation has been suspended. The erase sequence can be resumed with the erase resume command (D0h). An erase resume command must follow a suspend command before any other write/erase operation is allowed. If V_{PP} drops sufficiently below V_{PPH} during a suspended operation, the suspended operation will be aborted and a resume command must be given before another write/erase operation is accepted.

byte/word program

Byte programming is initiated by the command sequence: program setup (10h) followed by a write confirm command specifying address and data to be programmed. Addresses are latched during the confirm command on the falling edge of $\overline{E}$. Program data is latched on the rising edge of $\overline{E}$. Polling the device will determine when the program operation is complete. Ones (1s) cannot be programmed into any bit position and are ignored (e.g., programming FFh over an address location does not alter its data and does not return a fail condition).

soft protection

Data in the TMS28F040 is organized into sixteen separate 32K × 8-bit blocks indexed by address A15–A18. The device features the ability to protect the data stored in individual blocks from erasure and reprogramming. The protection mechanism is a bank of sixteen flags which can be set or reset through register commands. If a flag is set, it secures the data in the corresponding block by preventing all program/erase operations pertaining to that block. Upon power up, all flags are automatically cleared to allow unrestricted modification of the data array.

Alteration of the protection flags is a two bus-cycle process. On the first bus cycle, the software protect command, 0Fh, must be written to the device using the standard write cycle timings. On the next write strobe, a block address is latched into the address register on its falling edge and a keyword is latched into the data register on its rising edge. To have effect, the keyword must be one of the four patterns specifying the change as described in the command table. If data other than one of the four valid patterns is written on the second bus cycle, no change is made to the flag registers. Protection flags are not altered by V_{PP} transitions.

The benefit of this feature is that the end user can dynamically configure portions of the array as read-only. An attempt to alter data located in a protected block has no effect on its data. During an entire chip erase operation, protected blocks are unchanged and unprotected blocks are erased.

monitoring operation status

The status of the on-chip program and erase operations may be monitored when $V_{PP} = V_{PPH}$. The most complete monitoring method uses the status register. Alternatively, either the data poll bit (DQ7) or the toggle bit (DQ6) can be analyzed.

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Table 2. Status Register Bit Definitions

DESCRIPTION			FUNCTION
REGISTER BIT	HIGH (1)	LOW (0)	
SR.7 (DQ7)	Ready	Busy	Write state machine ready
SR.6 (DQ6)	Suspended	In progress/completed	Erase suspended
SR.5 (DQ5)	Failure in chip/block erasure	Successful chip/block erasure	Erase status
SR.4 (DQ4)	Failure in byte program	Successful byte program	Program status
SR.3 (DQ3)	V_{PP} low detect/operation aborted	V_{PP} status ok	V_{PP} low
SR0–SR.2			Reserved

NOTES: 4. Register bits SR.7–SR.0 correspond with DQ7–DQ0 respectively.
5. The SR.7 bit must first be checked to determine program or erase completion before status bits are checked for program/erase success. The erase status bit (SR.5) and program status bit (SR.4) are set by the write state machine and can only be reset by the clear status register command (50h). Program/erase operations are not guaranteed when V_{PP} drops below V_{PPH}. If a command sequence error is detected (invalid confirm command), both the program (SR.4) and erase (SR.5) status bits will be set. Status bits SR.3–SR.0 are reserved and should be masked out when polling the status register.

status register

The status register bit definitions table summarizes this functional description. The status register can be monitored by issuing the read status register command, 70h, either before or after initiating a program/erase operation. After the read status register command is given, the status register remains available until the device is reset to the read array mode by the FFh or 00h commands or read signature mode 90h. Any number of memory modifications can be performed before returning to the read array mode.

The contents of the status register are updated automatically by the write state machine. After a program/erase command is issued and confirmed, the ready bit (DQ7) of the status register indicates that the operation is in progress. No other program/erase commands are effective when the ready bit is low. Polling the ready bit for V_{OH} determines when the operation is complete. Afterwards, the program status (DQ5), erase status (DQ4) and V_{PP} low (DQ3) bits of the status register can be analyzed to validate successful completion. If any of these are set, they can be cleared by issuing a clear status register command, 50h. To maximize system flexibility, no requirement is made to verify or clear the status bits before another operation is attempted. The status register is cleared only by the clear status register command so that any number of memory modifications may be made between status register checks. Any failure conditions that occur will accumulate in the status register between clear commands. The clear status register command is available when $V_{PP} = V_{PPH}$ and while no write erase operation is in progress or suspended.

The status register can be used to monitor the state of the device entering and exiting the suspend mode. After the suspend command (B0h) is given, the suspend bit (DQ6) will be set to V_{OH}. When a breakpoint is reached, the write state machine sets the ready bit DQ7 to V_{OH}. Ready bit DQ7 should be used to monitor when a suspend request has been granted, and the suspend bit DQ6 should be used to determine if a resume operation is necessary. If the write state machine is not busy, the suspend command is ignored and suspend bit DQ6 will not be set. To begin reading the array, one of the read array commands, 00h or FFh, must be issued if the device was in the read status register mode. After reading the array, the device can be returned to reading the status register by again writing 70h. The resume command, D0h, continues the erase operation and resets both the suspend and ready bits to V_{OL}.

V_{PP} low status bit DQ3 indicates a catastrophic V_{PP} supply failure during a program, erase, or suspend operation. This bit will be set if V_{PP} drops significantly below V_{PPH} while the write state machine is busy or suspended. Any operation that was in progress at that time will be aborted. The V_{PP} low status bit provides a valid indication of gross failure of the V_{PP} supply. V_{PP} loss for short duration or slightly below minimum operating levels might still corrupt data without the status register indicating a failure. It is left to the user to provide power supply integrity.

data polling and toggle bits

If the device is set in the read array mode before or during a program/erase operation, the poll bit and toggle bit will be available. One method to check for operation completion is to use the toggle bit (DQ6). This bit is available along with the data poll bit (DQ7) when the device is in the read array mode. While the write state machine is busy, the toggle bit switches logic states with each falling edge of $\overline{E}$ or $\overline{G}$. When the program or erasure is complete, the output pins automatically return to providing the data stored in the byte specified by the address pins. Therefore, when DQ6 stops toggling between two consecutive reads to the same address, the operation is complete. To confirm successful array modification, the status register may be read by issuing the read status register command, 70h.

By addressing an unaltered block, the toggle bit may also be used to determine when a suspend request has been granted. After the B0h command is given, the toggle bit will continue to switch logic states with each falling edge of $\overline{E}$ or $\overline{G}$ until the current operation is suspended. DQ6 stops toggling between two consecutive reads to the same address once the suspend request has been granted.

While the write state machine is busy, the data poll bit (DQ7) reflects the complement of the data stored in the seventh bit of the target data register. After the operation is complete, the device output pins automatically return to reading the byte specified by the address pins. Data bit DQ7 changing from complement to true indicates the end of an operation. When using this monitor method, the addresses should remain stable throughout the operation. During a block or chip erasure, the data poll bit (DQ7) is always low and returns high at successful completion. Should the device fail to erase or program, the data poll bit (DQ7) might not return to its uncomplemented state. Data polling is available after the second bus-cycle write sequence initiating a program/erase operation. The success of the modification can be verified when the byte data becomes available. The status register is always readable by issuing the read status register command, 70h.

Table 3. Command Definitions

COMMAND	BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS†	DATA†
Read Array	1	Write	X	00h			
Read Array	1	Write	X	FFh			
Signature	3	Write	X	90h	Read	IA	
Read Status Register	2	Write	X	70h	Read	X	SRD
Clear Status Register	1	Write	X	50h			
Automated Block Erase	2	Write	X	20h	Write	BA	D0h
Erase Suspend	1	Write	X	B0h			
Erase Resume	1	Write	X	D0h			
Automated Byte Program	2	Write	X	10h	Write	PA	PD
Automated Chip Erase	2	Write	X	30h	Write	X	30h
Soft Protect	2	Write	X	0Fh	Write	BA	PC

NOTES: 6. The command data is written through DQ0–DQ7.
7. Following the signature command, two read operations access the manufacturer code (97h) and device code (79h).

† Description of terms:
IA = signature address: 00000h for mfr code; 00001h for device code.
BA = any address within the block to be selected; latched on falling edge of $\overline{E}$.
PA = address of memory location to be programmed; latched on falling edge of $\overline{E}$.
SRD = data read from status register.
PD = data to be written at location PA. Data is latched on rising edge of $\overline{E}$.
PC = Protect Command.
: 00h = Clear all protection (enable chip W/E)
: FFh = Set all protection (disable chip W/E)
: F0h = Clear addressed block protection (enable block W/E)
: 0Fh = Set addressed block protection (disable block W/E)

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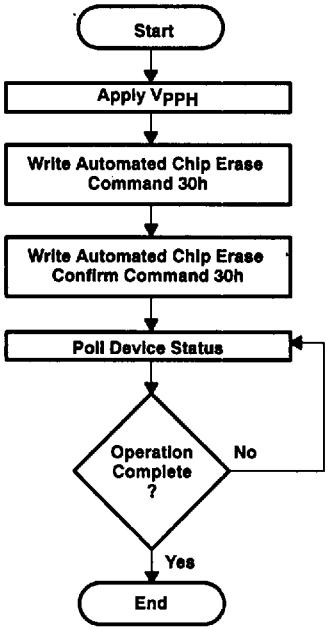

Figure 1. Automated Chip Erase Algorithm

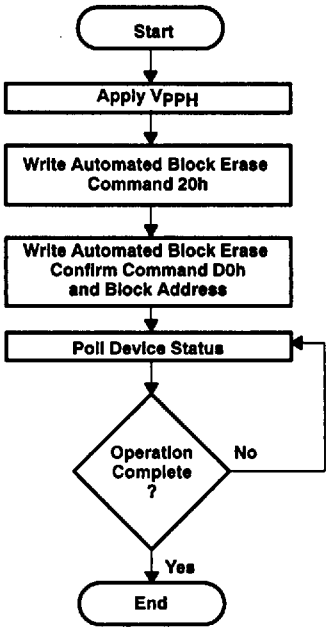

Figure 2. Automated Block Erase Algorithm

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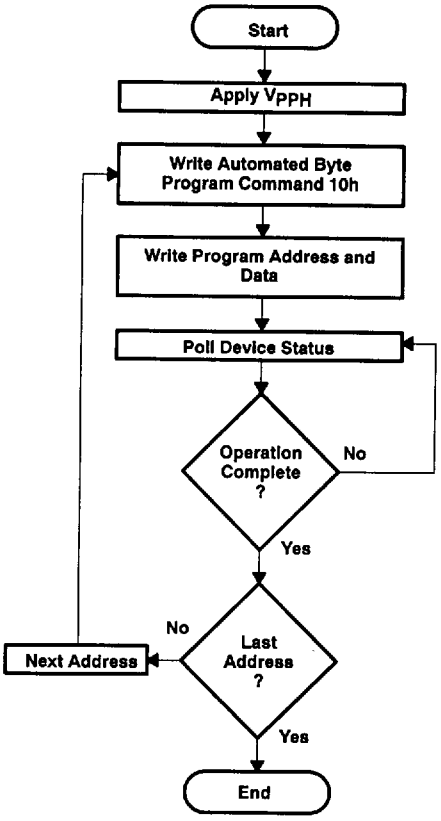

Figure 3. Automated Byte Program Algorithm

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absolute maximum ratings over operating free-air termperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 8) ..... –0.6 V to 7 V
Supply voltage, V_{PP} ..... –0.2 V to 15 V
Input voltage range: All except A9 (see Note 9) ..... –0.6 to 7 V
A9 (see Note 9) ..... –0.6 to 15 V
Output voltage ..... –0.6 to 7 V
Operating free-air temperature range during read/erase/program (NL, DDL, DUL) ..... 0°C to 70°C
Operating free-air temperature range during read/erase/program (NQ, DDQ, DUQ) ..... –40°C to 125°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 8. All voltage values are with respect to the most negative supply voltage V_{SS}.
9. The voltage on any input pin may undershoot to –2.0 V for periods less than 20 ns.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		Operating Range	4.5	5	5.5	V
		V_{LKO}	Erase/Write Lock-Out	2.5			V
V_{PP}	Supply voltage	V_{PPL}	Read Mode	–2.0‡	0	V_{CC}+2	V
		V_{PPH}	Program/Erase Mode	11.4	12	12.6	V
V_{IH}	High-level input voltage	TTL		2		V_{CC}+0.5	V
		CMOS		V_{CC} – 0.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage	TTL		–0.5		0.8	V
		CMOS		–0.5		0.2	V
V_{ID}	A9 signature voltage			11.4		13	V
T_A	Operating free-air temperature	NL, DDL, DUL, suffix		0		70	°C
		NQ, DDQ, DUQ suffix		–40		125	

‡ Duration of V_{PP} undershoot must be < 20 ns.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	CMOS-output level	$I_{OH} = -20\ \mu A$	$V_{CC} - 0.2$		V
		TTL-output level	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Low-level output voltage	TTL-output level	$I_{OL} = 2.1$ mA		0.45	V
		CMOS-output level	$I_{OL} = 20\ \mu A$		0.1	V
I_I	Input current (leakage)		$V_I = 0$ to V_{CC}		±1	µA
I_O	Output current (leakage)		$\overline{E} = V_{IH}$, $V_O = 0$ to V_{CC}		±10	µA
I_{ID}	A9 signature mode current		A9 = V_{ID} MAX		200	µA
I_{CC1}	V_{CC} supply current (Standby)	TTL-input level	$\overline{E} = V_{IH}$, $V_{CC} = 5.5$ V		1	mA
		CMOS-input level	$\overline{E} = V_{CC} + 0.2$ V, $V_{CC} = 5.5$ V		100	µA
I_{CC2}	V_{CC} supply current (Read mode)		$\overline{E} = V_{IL}$, $V_{CC} = 5.5$ V, f = 6 MHz, $I_{OUT} = 0$ mA		40	mA
I_{CC3}	V_{CC} supply current (Program mode)		$V_{CC} = 5.5$ V, $\overline{G} = V_{IH}$, Programming in progress		30	mA
I_{CC4}	V_{CC} supply current (Erase mode)		$V_{CC} = 5.5$ V, $\overline{G} = V_{IH}$, Chip Erase in progress		30	mA
I_{CC5}	V_{CC} supply current (Erase Suspend)		$V_{CC} = 5.5$ V, $I_{OUT} = 0$ mA, Erase suspended, Block read at f = 6 MHz		40	mA
I_{PP1}	V_{PP} supply current (Standby)		GND ≤ V_{PP} ≤ V_{CC}, $\overline{E} = V_{IH}$		±10	µA
I_{PP2}	V_{PP} supply current (Read mode)		$V_{PP} = V_{PPH}$ MAX		200	µA
I_{PP3}	V_{PP} supply current (Program mode)		$V_{PP} = V_{PPH}$ MAX, Programming in progress		30	mA
I_{PP4}	V_{PP} supply current (Erase mode)		$V_{PP} = V_{PPH}$ MAX, Chip erase in progress		50	mA
I_{PP5}	V_{PP} supply current (Erase suspend)		$V_{PP} = V_{PPH}$ MAX, Erase suspended, Block read at f = 6 MHz		200	µA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance	$V_I = 0$, f = 1 MHz		4	6	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz		6	12	pF
C_{VPP}	V_{PP} input capacitance	$V_{PP} = 0$, f = 1 MHz		6	12	pF

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TEXAS INSTRUMENTS
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switching characteristics over recommended operating free-air temperature range: read-only operation

DESCRIPTION		ALT. SYMBOL	'28F040-10		'28F040-12		'28F040-15		'28F040-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Read cycle time	t_{RC}	100		120		150		170		ns
t_{AVQV}	Access time from address	t_{ACC}		100		120		150		170	ns
	Output hold from Address, $\overline{E}$, or $\overline{G}$ change	t_{OH}	0		0		0		0		ns
t_{ELQV}	$\overline{E}$ to output valid	t_{CE}		100		120		150		170	ns
t_{ELQX}	$\overline{E}$ to output low Z	t_{LZ}	0		0		0		0		ns
t_{EHQZ}	$\overline{E}$ to output high Z	t_{HZ}		30		30		35		40	ns
t_{GLQV}	$\overline{G}$ to output valid	t_{OE}		50		55		60		65	ns
t_{GLQX}	$\overline{G}$ to output low Z	t_{OL}	0		0		0		0		ns
t_{GHQZ}	$\overline{G}$ to output high Z	t_{DF}		30		30		35		40	ns
t_{VCS}	V_{CC} setup time to valid read	t_{VCS}	20		20		20		20		µs
t_{GLWL}	$\overline{G}$ read setup time to $\overline{E}$ high†	t_{GLWL}	20		20		20		20		ns
t_{GLWH}	$\overline{G}$ read pulse duration†	t_{GLWH}	40		45		50		55		ns

† Required when $V_{PP} = V_{PPH}$.

switching characteristics over recommended operating free-air temperature range: write, erase, program operations

PARAMETER		ALT. SYMBOL	'28F040-10		'28F040-12		'28F040-15		'28F040-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Write cycle time	t_{WC}	100		120		150		170		ns
t_{AVWH}	Address setup time	t_{AS}	0		0		0		0		ns
t_{WHAX}	Address hold time	t_{AH}	45		50		55		60		ns
t_{GHWL}	$\overline{G}$ write setup time	t_{GHWL}	0		0		0		0		ns
t_{GHWH}	$\overline{G}$ write hold time	t_{GHWH}	5		5		5		5		ns
t_{VPWL}	V_{PP} setup to $\overline{E}$ write strobe‡	t_{VPS}	60		60		60		60		ns
t_{WLWH}	$\overline{E}$ write strobe pulse duration	t_{WP}	40		45		50		55		ns
t_{WHWL}	$\overline{E}$ write strobe pulse duration high	t_{WPH}	20		20		20		20		ns
t_{DVWH}	Data setup to $\overline{E}$ high	t_{DS}	20		20		20		20		ns
t_{WHDX}	Data hold time	t_{D}	10		10		10		10		ns
t_{VPPR}	V_{PP} rise time (90% V_{PPH})	t_{VPPR}	500		500		500		500		ns
t_{VPPH}	V_{PP} hold time	t_{VPPH}	0		0		0		0		ns
t_{WHWH1}	Duration of program operation	t_{WHWH1}	8.6	529	8.6	529	8.6	529	8.6	529	µs
t_{WHWH2}	Duration of block erase operation	t_{WHWH2}	0.1	62.5	0.1	62.5	0.1	62.5	0.1	62.5	s
t_{WHWH3}	Duration of chip erase operation	t_{WHWH3}	2.6	184	2.6	184	2.6	184	2.6	184	s

‡ $\overline{E}$ must equal V_{IH} during V_{PP} transitions.

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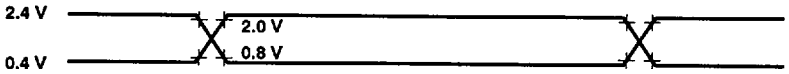
automated erase and programming performance†

PARAMETER	MIN	TYP	MAX	UNIT
Byte programming time	8.60	45	529	µs
Block erase time	0.10	2	62.5	s
Block programming time	0.28	1.5	17.3	s
Chip erase time	2.60	12.2	184	s
Chip programming time	2.26	23.6	277	s
Suspend latency time	0	3	10.1	ms

† All times include on-chip preconditioning, pulse generation, and verification.

PARAMETER MEASUREMENT INFORMATION

AC input/output reference waveform



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 for logic low. Timing measurements are made at 2 V for logic high and 0.8 V logic low on both inputs and outputs. Each device should have a 0.1 µF ceramic capacitor between V_{CC} and V_{SS} as close as possible to the device pins.

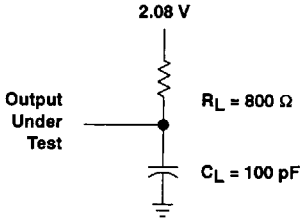


Figure 4. Output Load Circuit

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PARAMETER MEASUREMENT INFORMATION

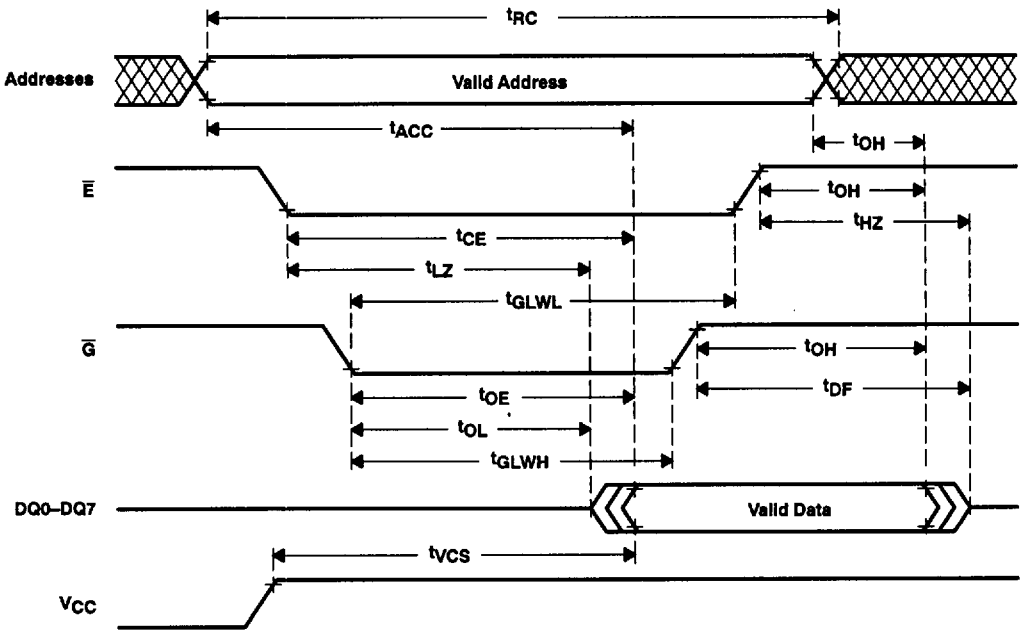
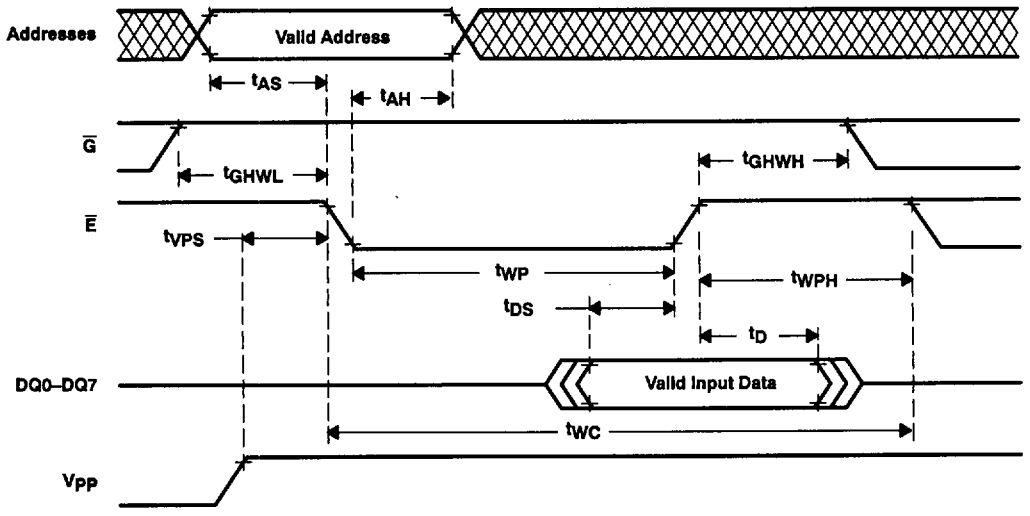


Figure 5. AC Waveform for Read Operations



NOTE: Addresses are latched on the falling edge of Ē.
Command and Program data are latched on the rising edge Ē.

Figure 6. AC Waveform for Write Operations

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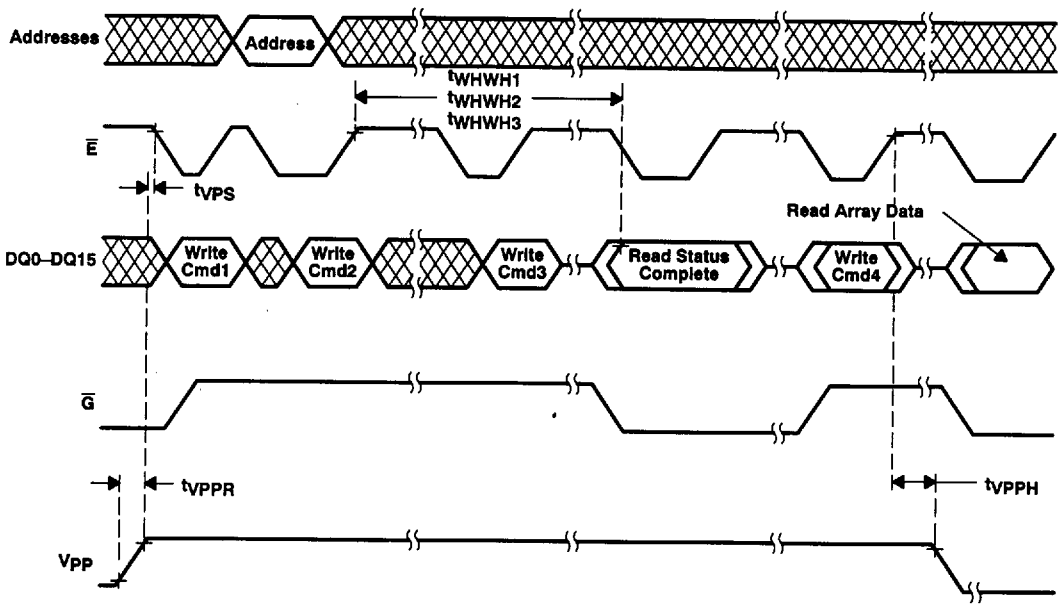
PROGRAM/ERASE INFORMATION



Command	Cmd1		Cmd2		Cmd3		Read		Cmd4		Read
Program	10h		data		70h		status		00h		array
Chip Erase	30h		30h		70h		status		00h		array
Block Erase	20h		D0h		70h		status		00h		array

NOTE: Addresses are latched on the falling edge of $\overline{E}$.
Command and Program data are latched on the rising edge $\overline{E}$.

Figure 7. AC Waveform for Program/Erase Operations

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