MOTOROLA

Advance Information

8K x 8 Bit Static Random Access Memory

ELECTRICALLY TESTED PER:
MPG6264C

6264C

Commercial Plus and Mil/Aero Applications

AVAILABLE AS

1) JAN: N/A
2) SMD: Pending
3) 883: 6264C - XX/BXAJC
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL: X
LCC: U
XX = Speed in ns
(15, 20, 25, 35, 45, 55, 70)

The letter "M" appears after the speed on LCC

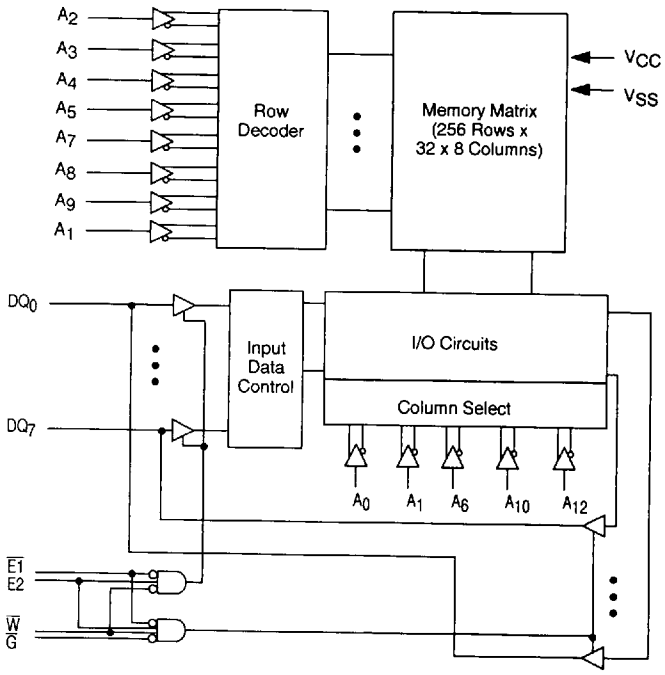
The 6264C is a 65,536-bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low-power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

The 6264C is available in a 600 mil, 28-pin ceramic DIL, and a 32-terminal ceramic LCCC package and features the standard JEDEC pinout.

- Single 5.0 V ± 10% Power Supply
- Output Enable (G) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 15, 20, 25, 35, 45, 55, 70 ns
- Low Power Dissipation — 825 mW
- Fully TTL Compatible
- Three State Data Outputs

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BURN-IN CONDITIONS:									
V_{CC} = 5.0 V(min)/ 6.0 V(max), R_1 = 39.2 kΩ ± 20%, C_1 = 0.1 µF ± 20%, V_H = 3.0 V(min)/5.0 V(max), V_L = − 0.5 V(min)/0.0 V(max),									
CP1:	100 kHz	CP6:	3.125 kHz	CP11:	97.66 Hz	CP16:	3.052 Hz		
CP2:	50 kHz	CP7:	1.563 kHz	CP12:	48.83 Hz	CP17:	1.526 Hz		
CP3:	25 kHz	CP8:	0.781 kHz	CP13:	24.41 Hz	CP18:	0.763 Hz		
CP4:	12.5 kHz	CP9:	0.391 kHz	CP14:	12.21 Hz	CP19:	0.382 Hz		
CP5:	6.25 kHz	CP10:	0.195 kHz	CP15:	6.104 Hz	CP20:	0.191 Hz		

PIN NAME and FUNCTIONS

$A_0 - A_{12}$	Address Inputs
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
$DQ_0 - DQ_7$	Data Input/Output
V_{CC}	+ 5.0 V Power Supply
V_{SS}	Ground
N.C.	No Connection

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{OUT}
L	H	X	L	Write	I_{CC}	D_{IN}

X = Don't Care

PIN ASSIGNMENTS

Function	DIL	LCC 766A-01	Burn-In (Condition-D)
N.C.	1	2	N.C.
A_{12}	2	3	CP4
A_7	3	4	CP5
A_8	4	5	CP6
A_5	5	6	CP7
A_4	6	7	CP8
A_3	7	8	CP9
A_2	8	9	CP10
A_1	9	10	CP11
A_0	10	11	CP12
DQ_0	11	13	R_1 to CP17
DQ_1	12	14	R_1 to CP17
DQ_2	13	15	R_1 to CP17
V_{SS}	14	16	GND
DQ_3	15	18	R_1 to CP17
DQ_4	16	19	R_1 to CP17
DQ_5	17	20	R_1 to CP17
DQ_6	18	21	R_1 to CP17
DQ_7	19	22	R_1 to CP17
$\overline{E1}$	20	23	CP2
A_{10}	21	24	CP13
$\overline{G}$	22	25	CP1
A_{11}	23	27	CP14
A_9	24	28	CP15
A_8	25	29	CP16
E2	26	30	CP3
$\overline{W}$	27	31	CP1
V_{CC}	28	32	V_{CC}, C_1 to GND

ABSOLUTE MAXIMUM RATINGS (See Note)			
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{IN}, V_{OUT}	− 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{OUT}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	− 55 to +125	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C
Operating Temperature Range	T_A	− 55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = – 55°C to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.3 *	0.8	V

* V_{IL} (min) = – 0.5 Vdc; V_{IL} (min) = – 3.0 Vdc (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter			Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})			I_{IL}	—	2.0	µA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, V_{OUT} = 0 to V_{CC})			I_{OZL}	—	2.0	µA
Operating Supply Current Cycle = Min, Duty = 100%	+25, +125°C –55°C	(15) (25)	I_{CCA} I_{CCA}	— —	150 135	mA mA
TTL Standby Current ($\overline{E1}$ = V_{IH}, or E2 = V_{IL})			I_{SB1}	—	35	mA
CMOS Standby Current ($\overline{E1}$ ≥ V_{CC} – 2.0 V, E2 ≥ 0.2 V)			I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)			V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)			V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Sampled at initial device qualification and major redesign rather than 100% tested)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	—	5.0	10	pF
I/O Capacitance	DQ	$C_{I/O}$	—	6.0	12	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55°C to +125°C, Unless Otherwise Noted)

Input Reference Level	1.5 V
Input Pulse levels	0 to 3.0 V
Input Rise/Falls Time	5.0 ns
Output Reference Level	1.5 V
Output Load	See Figure 1

AC TEST LOADS OR EQUIVALENT

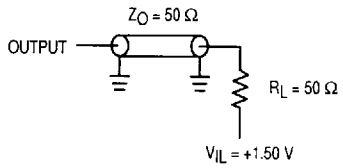


Figure 1A.

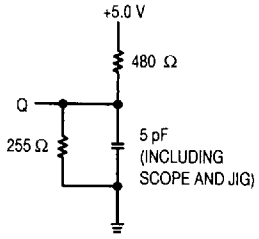


Figure 1B.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

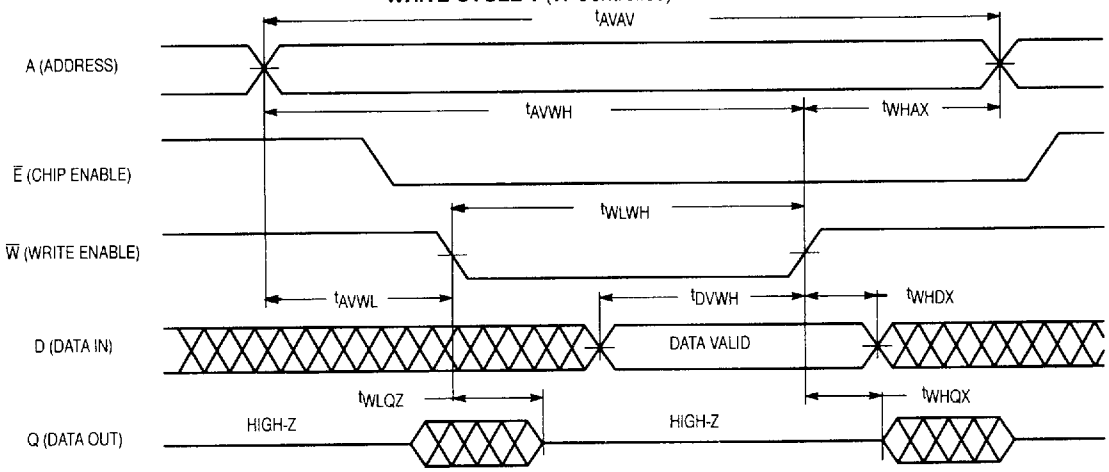
Parameter	Symbol Standard	Symbol Alternate	6264C-15		6264C-20		6264C-25		6264C-35		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	25	—	35	—	ns	—
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	15	—	20	—	30	—	ns	—
Write Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	20	—	30	—	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	5.0	—	10	—	15	—	25	—	ns	—
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	3
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	0	—	0	—	0	—	0	—	ns	4

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol Standard	Symbol Alternate	6264C-45		6264C-55		6264C-70		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	—	55	—	70	—	ns	—
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AVWH}	t_{AW}	40	—	50	—	65	—	ns	—
Write Pulse Width	t_{WLWH}	t_{WP}	40	—	50	—	65	—	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	35	—	45	—	60	—	ns	—
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	3
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	0	—	0	—	0	—	ns	4

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, or low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z AND low-Z parameters are considered in a high or low impedance state when the output has made a 500 mW transition from the previous steady state voltage.

WRITE CYCLE 1 ($\overline{W}$ Controlled)



TIMING LIMITS

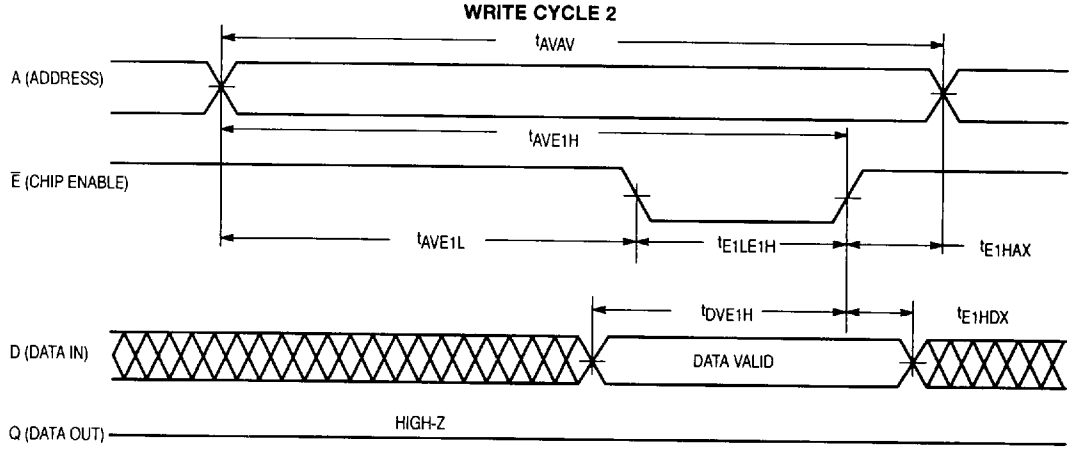
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 (See Note 1)												
Parameter	Symbol Standard	Symbol Alternate	6264C-15		6264C-20		6264C-25		6264C-35		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	25	—	35	—	ns	—
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	—

WRITE CYCLE 2 (See Note 1)										
Parameter	Symbol Standard	Symbol Alternate	6264C-45		6264C-55		6264C-70		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	—	55	—	70	—	ns	—
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	—

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, or low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2
2. $\overline{E1}$ and E2 timing are identical when E2 signals are inverted.

WRITE CYCLE 2



READ CYCLE (See Note 1)												
Parameter	Symbol Standard	Symbol Alternate	6264C-15		6264C-20		6264C-25		6264C-35		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	20	—	25	—	35	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	20	—	25	—	35	ns	—
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	—	15	—	20	—	25	—	35	ns	—
E2 Access Time	t_{E2HQV}	t_{AC2}	—	15	—	20	—	25	—	35	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	12	—	15	—	20	—	25	ns	—
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5.0	—	5.0	—	5.0	—	5.0	—	ns	2
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	2
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	—	5.0	—	10	—	15	—	20	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	—	5.0	—	10	—	15	—	20	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. This parameter is sampled and not 100% tested.

READ CYCLE (See Note 1)										
Parameter	Symbol Standard	Symbol Alternate	6264C-45		6264C-55		6264C-70		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	45	—	55	—	70	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	45	—	55	—	70	ns	—
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	—	45	—	55	—	70	ns	—
E2 Access Time	t_{E2HQV}	t_{AC2}	—	45	—	55	—	70	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	30	—	35	—	40	ns	—
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5.0	—	5.0	—	5.0	—	ns	2
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	2
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	—	25	—	30	—	35	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	—	25	—	30	—	35	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. This parameter is sampled and not 100% tested.

READ CYCLE