LDS8161/41

IXYS Display

6-Channel / 4-Channel High-Side Linear WLED Driver
with LED Temperature Compensation Using LED-Sense™, I²C, and Digital PWM

FEATURES

- **Six (8161) / or Four (8141) Power-Lite™ Linear LDO current regulators with 50 mV dropout in a high-side driver topology.**
- **High temperature LED current de-rating using the LED-Sense™ temperature compensation algorithm, which directly monitors an LED PN junction. No external temperature sensor is required.**
- **I²C compatible serial programming interface**
- **LED current programmable via I²C from 0 to ~32 mA in 256 linear steps. Three (8161) or two (8141) separately controlled driver banks with 2 LED drivers each**
- **Integrated PWM generator for LED dimming with 12-bit resolution and 256 I²C-programmable logarithmic duty cycle steps from 0% to 100% (~0.17 dB per step)**
- **Total combined dimming range of > 16,384:1**
- **Power efficiency up to 98%; average efficiency > 80% in Li-ion battery applications**
- **Low current shutdown mode (< 1 µA);**
- **Soft start and current limiting**
- **LED Short circuit detection and protection, LED open detection**
- **Thermal shutdown protection**
- **Low EMI.**
- **Available in 3 mm x 3 mm x 0.8 mm 16-pin TQFN package**

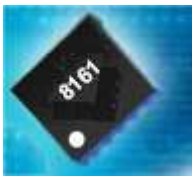
APPLICATIONS

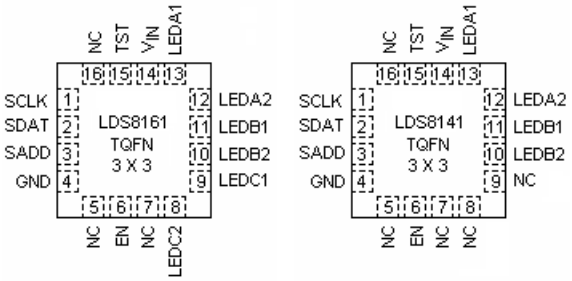
- **Keypad and Display Backlight**
- **Cellular Phone**
- **PDAs and Smartphones**

DESCRIPTION

The LDS8161 is a 6-channel and the LDS8141 is a 4-channel linear LED driver for WLED applications. It includes ultra low dropout LDO current regulators at a maximum 31.875 mA per channel in a common cathode high side driver topology.

The LDS8161/LDS8141 has an average efficiency of > 80% in Li-ion battery applications. It includes three (LDS8161) or two (LDS8141) 8-bit current setting DACs (one per bank) allowing LED currents to be programmed via an I²C-compatible serial interface from 0 to 31.875 mA in 256 steps of 125µA per step.





The LDO drivers have a low dropout voltage of 50 mV typically at maximum rated current. This provides a low power/low EMI solution in Li-ion battery applications without voltage boosting and associated external capacitors and components.

High temperature current de-rating insures LED reliability and provides automatic adjustment of LED current to achieve maximum specified LED brightness across the ambient temperature range. The proprietary LED-Sense™ temperature compensation algorithm directly monitors the junction temperature of an LED and applies current de-rating per a user loadable LUT (look up table) in 5ºC steps. No external temperature-sensing device is needed.

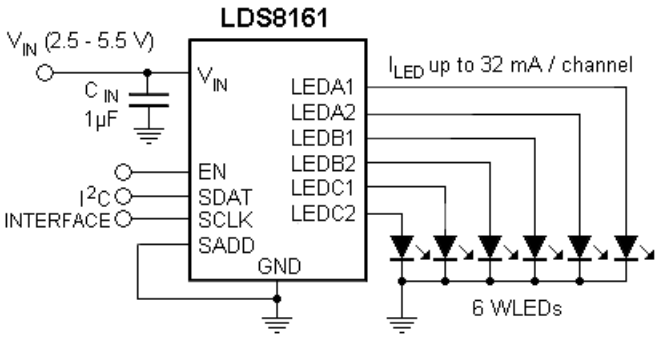
An integrated 12-bit PWM generator with “smooth” logarithmic control supports LED dimming and high temperature current de-rating. The PWM duty cycle is programmable via the I²C serial interface from 0% to 100%. User programmed 8-bit codes are converted to 12-bit resolution logarithmic steps of ~ 0.17 dB per step. The PWM frequency is ~280 Hz to minimize noise generation.

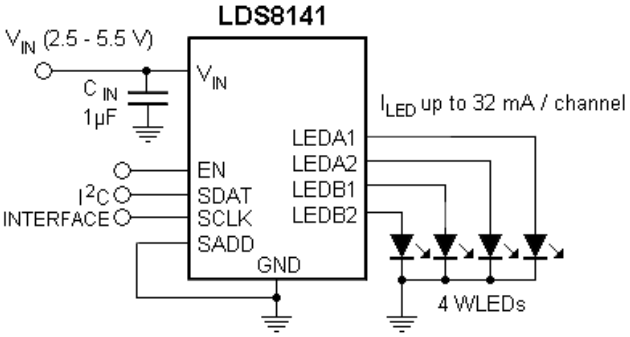
The EN logic input functions as a chip enable. A logic HIGH applied at the EN pin allows the LDS8161/LDS8141 to respond to I²C communications. An external serial interface address pin is available for use in multi-target applications.

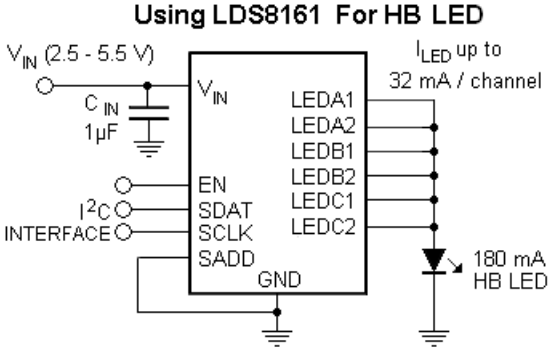
The device operates from 2.5V to 5.5V.

The LDS8160 is available in a 3 x 3 x 0.8 mm³ 16-lead TQFN package.

TYPICAL APPLICATION CIRCUITS







ABSOLUTE MAXIMUM RATINGS

Parameter		Rating	Unit
V_{IN}, LEDx		6	V
EN, SDAT, SCLK, SADD voltage		V_{IN} + 0.7V	V
Storage Temperature Range		-65 to +160	°C
Junction Temperature Range		-40 to +125	°C
Soldering Temperature		300	°C
ESD Protection Level	HBM	2	kV
	MM	200	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
V_{IN}	2.5 to 5.5	V
I_{LED} per LED pin	0 – 31.875	mA
Total Output Current I_{LOAD}	191.25	mA
Junction Temperature Range	-40 to +125	°C

Typical application circuit with external components is shown on page 1.

ELECTRICAL OPERATING CHARACTERISTICS

(Over recommended operating conditions unless specified otherwise) V_{IN} = 3.6V, C_{IN} = 1 µF, EN = High, T_{AMB} = 25°C

Name			Conditions	Min	Typ	Max	Units
LEDx Channel Current DAC Range				0		31.875	mA
# of LEDx Current steps (linear steps)					256		steps
LEDx Current DAC Resolution/step					0.125		mA
Quiescent Current	EN = V_{IN}		Standby (no I^2C clock)		125		µA
	6/4 Channels at 100% DC PWMs and Temp De-Rating Active		I_{LOAD} = 120 mA/ 80 mA		0.6/0.45		mA
			I_{LOAD} = 60 mA / 40 mA		0.45/0.35	0.35	mA
Shutdown Current			V_{EN} = 0V		0.5	1	µA
LED Current Accuracy			5 mA ≤ I_{LED} ≤ 30 mA		±1.5		%
LED Channel Matching			(I_{LED} - I_{LEDAVG}) / I_{LEDAVG}		±1.5		%
Line Regulation			2.7 V ≤ V_{IN} ≤ 4.2 V		2		%/V
Load Regulation[1]			0.2 V < Vdx < 1.2 V		1		%/V
Dropout Voltage[2]			1 mA ≤ I_{LED} ≤ 30 mA		50	75	mV
PWM Frequency					285		Hz
# of PWM duty cycle steps					256		
Minimum PWM On Time					13.7		µs
PWM resolution					12		bits
PWM Step Size					0.17		dB
# of ΔPWM Steps for current de-rating			1-x Scale Mode	-7		0	PWM Steps/5^0C
			2-x Scale Mode	-14		0	
De-rating Temperature Adjust Steps					5		^{0}C
Programmable De-rating Start Temperature (Tj) Range (typical)				30	55	80	^{0}C
Programmable LED Shutdown Temperature(Tj) Range (typical)				80	105	120	^{0}C
EN Pin	Input current		Active or Normal Standby mode; EN = V_{IN}	-1		1	µA
			Shutdown	-0.1		0.1	
	Logic Level	High	Active or Normal Standby Mode	1.2		V_{IN}	V
		Low	Shutdown	0		0.4	
Thermal Shutdown					150		°C
Thermal Hysteresis					20		
Wake-up/Shutdown Delay Time from EN Raising/Falling Edge			Soft ramp disabled		10		ms
			Soft ramp enabled		250		ms
Output short circuit Threshold[3]			I_{LED} = 20 mA		0.4		V

Note: 1. Vdx = Vin – V_F,

2. Vdx = Vin – V_F, at which I_{ILED} decreases by 10% from set value

3. Minimum LED forward voltage, which will be interpreted as “LED SHORT” condition

I²C CHARACTERISTICS

Over recommended operating conditions unless otherwise specified for 2.7 ≤ VIN ≤ 5.5V, over full ambient temperature range -40 to +85ºC.

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL Clock Frequency	0	400	kHz
$t_{HD:STA}$	Hold Time (repeated) START condition	0.6		µs
t_{LOW}	LOW period of the SCL clock	1.3		µs
t_{HIGH}	HIGH period of the SCL clock	0.6		µs
$t_{SU:STA}$	Set-up Time for a repeated START condition	0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0	0.9	ns
$t_{SU:DAT}$	Data In Set-up Time	100		ns
t_R	Rise Time of both SDAT and SCLK signals		300	ns
t_F	Fall Time of both SDAT and SCLK signals		300	ns
$t_{SU:STO}$	Set-up Time for STOP condition	0.6		µs
t_{BUF}	Bus Free Time between a STOP and START condition	1.3		µs
t_{AA}	SCLK Low to SDAT Data Out and ACK Out		0.9	µs
t_{DH}	Data Out Hold Time	300		ns

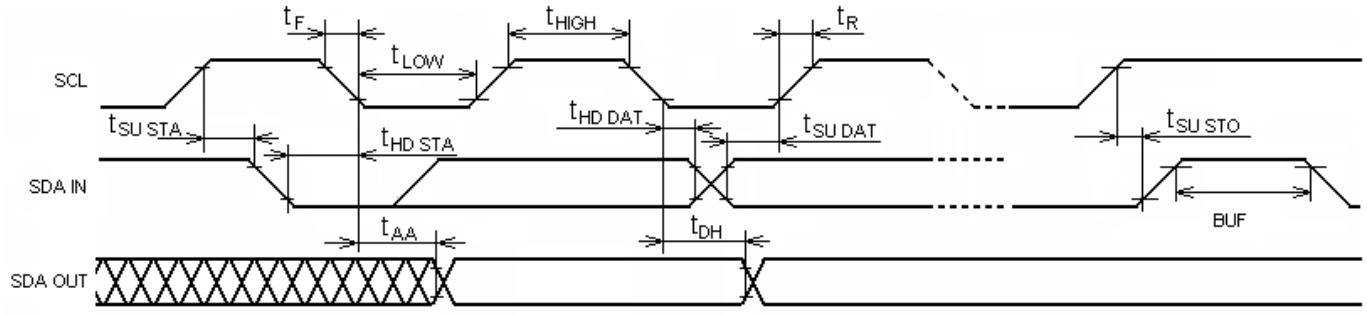


Figure 1: I²C Bus Timing Diagram

READ OPERATION:

Option 1: Standard protocol sequential read:

S	Slave Address	R	A	Data 0	A	Data 1	A	Data 2		Data n	A*	P
				From: Reg. m		Reg. m+1		Reg. m+2		Reg. m+n,		

where Reg. m is the last addressed in the write operation register

Option 2: Random access:

S	Slave Address	R	A	Data m	A*	P
				From reg. m, where Reg. m is the last addressed in the write operation register		

Option 3: Random access with combined (extended) protocol:

S	Slave Address	W	A	Register Address m	A	Sr	Slave Address	R	A	Data m	A*	P

WRITE OPERATION:

Option 1: Standard protocol sequencial write:

S	Slave Address	W	A	Register Address m	A	Data 0	A	Data 1	A	Data 2		Data k	A*	P
						To: Reg. m		Reg. m+1		Reg. m+2		Reg. m+k		

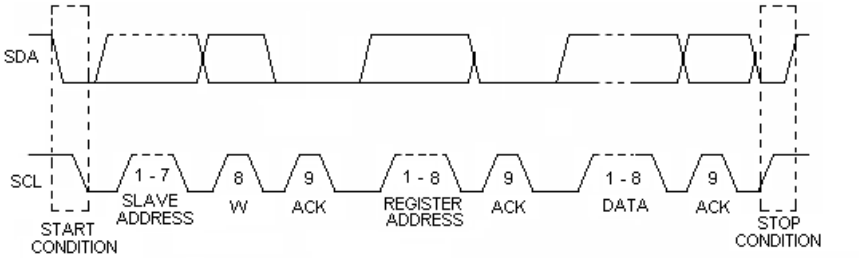
Option 2: Combined (extended) protocol:

S	Slave Address	W	A	Register Address m	A	Sr	Slave Address	W	A	Data	A*	P
										To: Reg. m		

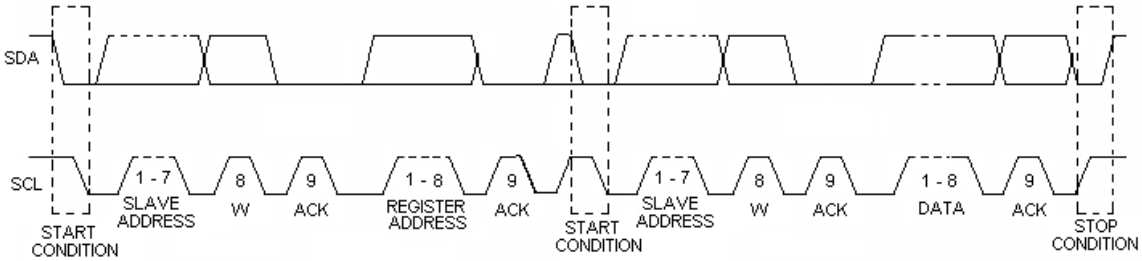
S: Start Condition
Sr Start Repeat Condition
R, W: Read bit (1), Write bit (0)
A: Acknowledge (SDAT high)
A*: Not Acknowledge (SDAT low)
P: Stop Condition
Slave Address: Device address 7 bits (MSB first).
Register Address: Device register address 8 bits
Data: Data to read or write 8 bits
- send by master
- send by slave

I²C BUS PROTOCOL

Standard protocol



Combined protocol:



WRITE INSTRUCTION SEQUENCE

Standard protocol:

Write Instruction Example - Setting 20mA Current in LEDB1 and LEDB2

LDS8161 / 41 REGISTERS DEFINITION AND PROGRAMMING

Note: Unlisted register addresses are for factory use only; For proper operation write only to registers defined.

ADDRESS	DESCRIPTION	BITS	NOTES
00h	Bank A Current setting	8	Reg00h – Reg02h data code = (I_{LED} / 0.125 mA) (decimal) converted into hex format
01h	Bank B Current setting	8	
02h	Bank C Current setting (8161 only; Not for 8141)	8	
03h	Channel Enable (No Bits 5, 4 for C2 and C1 respectively for 8141)	6	Bits 5:0 = 1 enables LEDs C2, C1, B2, B1, A2, A1 respectively (See Table 1). Both LEDs from one bank should be disabled to minimize power consumption.
05h	Bank A, B, C PWM Duty Cycle	8	~ – 0.17dB dimming per LSB for currents > 300 µA; Refer to 8 to 12 bit conversion curve (Figure 3 and Table 10) for resolution in range 0 – 300 µA Data Code 00h = 0% Duty Cycle, FFh = 100% Duty Cycle Example: 50% brightness reduction (– 6dB) requires: 255 – (– 6 dB / – 0.17 dB) = 255 – 35 = 220 (decimal) = DCh steps
19h	LED Diagnostics Test	8	See Table 2; Bit 5 = 1 sets user-initiated LED short/open diagnostic
1Ch	LED Faults Status (shorted to GND)	5	Bits from bit 5 to bit 0 represent LED status for LEDC2 – LEDA1 respectively. Bit = 1 represents LED shorted to GND
1Dh	LED Faults Status (shorted to V_{IN}/open)	5	Bits from bit 5 to bit 0 represent LED status for LEDC2 – LEDA1 respectively. Bit = 1 represents LED shorted to V_{IN}/open
1Eh	Configuration register	8	See Table 3
1Fh	Software reset, Standby	8	See Table 4
49h	Ta-Tj Temperature Offset	8	Since junction temperature is measured, the values loaded here allow an offset to account for Tj – Ta gradient. This allows de-rate tables to be referenced to Ta levels. Two 4 bit offsets value for the LED and the Si Diode; Bit [7:4] = Tj-Ta offset for the LEDs Bit [3:0] = Tj-Ta offset for the Si diode. Typically should set both offsets to be equal. See Table 5 & 6
4Ah	LED Shutdown Temperature	5	Defines T-code, at which LED current shuts down per LED vendor de-rating specification (see Table 5); Factory default value = 11100 (bin) = 1Ch represents 105^0C Tj
4Bh	2-x Table enable and breakpoint (T-code)	6	Bit 5 = 1 – enable 2-x scale LUT ΔPWM code correction (de-rating) starting at the breakpoint set by T-code (bits 4:0) Bit 5 = 0 – 1-x scale (default) for entire temperature range Bit [4:0] defines T-code, where temperature de-rating starts, or where 2-x scaling begins (see Table 5)
56h – 5Dh	Temp De-rating LUT 25C to 100C (one 5C step every nibble) ΔPWM code1[7:4], ΔPWM code0[3:0] – ΔPWM code13[7:4], ΔPWM code12[3:0]	8	Two LUT words per I^2C address. Each word contains two 4-bit numbers representing of ΔPWM codes (See Table 6 and Appendix 1 for LUT programming.) Factory default setting is a table for WLED LED (Nichia NSSW020BT WLED). Default table could be used for WLED de-rating. De-Rating starts at 55ºC junction temperature

A0h	Silicon diode dV_F/dT [7:0]	8	Silicon diode V_F temperature coefficient (K factor) : Factory recommended loaded value is 36h = -1.71 mV/°C = 001 10110 (bin), where bits from bit 7 to bit 5 represent integer part [1(decimal) = 001 (bin)], and bits from bit 4 to bit 0 – fractional part [0.710 / 0.03125 = 22 (decimal) = 10110 (bin)]
A2h	LED dV_F/dT [7:0]	8	User-loaded V_F temperature coefficient @ 1mA for LEDs used at Banks A, B, C respectively. Negative tracking is assumed with temperature; Bits from bit 7 to bit 5 represent integer part and bits from bit 4 to bit 0 - fractional part of the coefficient Example: Temperature coefficient = -2.26 $mV/^0C$; Bit 7 – bit 6 = 2 (decimal) = 010 (bin), and Bit 4 – bit 0 = INT{0.26 / 0.03125} = 8 (decimal) = 01000 (bin) User loads 010 01000 (bin) = 48h = -2.25 (closest setting)
C0h	Silicon diode η [7:0]	8	Silicon diode η (eta, or non-ideality factor): Factory recommended loaded value is default is 1.00 = 01000000(bin) = 40h Bits from bit 7 to bit 5 represent integer part and bits from bit 4 to bit 0 - fractional part (resolution = 0.015625 per LSB) Example: η = 1.00; Bit 7 – bit 6 = 1 (decimal) = 01 (bin), and Bit 5 – bit 0 = INT{0.00 / 0.015625} = 0 (dec) = 000000 (bin) User loads 01 000000 = 40h = 1.00
D4h	Silicon diode R_s offset [7:0]	8	Silicon diode series resistance offset Factory recommended loaded value = 04h = ~ 68 ohms Formula (decimal) = 8192 x [(68 ohms x 8 x 10^{-6} A)/1.14 V]
D6h	LED Rs offset [7:0]	8	LED Rs offset (user-loaded) for Banks A, B, and C LEDs Typically LED Rs = 5 – 30 Ω User loads per LED used. (1/slope of high current region of LED I-V characteristic). Formula (decimal) = 8192 x [(Rs Ω x 8 x 10^{-4} A) / 1.14V]

Table 1

Register Address	Channel Enable Register							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
03h (8161)	LED OT Flag	N/A	Enable C2	Enable C1	Enable B2	Enable B1	Enable A2	Enable A1
(8141)	Same	N/A	N/A	N/A	Same	Same	Same	Same

Table 2

Register Address	Digital Test Modes Register							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
19h	Factory Only	Factory Only	Diagnostics Request	Slow Ramp Bypass = 1	Fast PWM adjust =1	Factory Only	Post ADC Filter Enable =1	Factory Only
	0*	0*	0*	0*	Normal = 0*	0*	Filter Off=0*	0*

Note: *) Value by default

Table 3

Register Address	Configuration Register							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1Eh	Factory Set 1*	Factory Only	Factory Only	Factory Only	Factory Only	dT adjust disabled = 1*	Soft Start disabled = 1	Factory Only
	Factory trimmed; User should write 0	0*	0*	0*	0*	dT adjust enabled = 0	Soft Start enabled = 0*	0*

Note: *) Value by default

Table 4

Register Address	Control Register							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1Fh	Software reset = 1	Standby mode = 1	Temperature request = 1	Calibration request = 1	Custom OSC trim = 1	Osc trim 2 **	Osc trim 1 **	Osc trim 0 **
	Normal operation = 0*				Factory preset = 0*			

Note: *) Value by default
**) Trim code defined by customer
Bit 7 = 1 — Software reset: resets device, all registers reset/cleared.
Bit 6 = 1 — Standby (oscillator disabled, all registers retain programmed values.)

Table 5: Ta-Tj Temperature Gradient Offset
(Set offset code to match reference De-rate point in LUT from LED Tj to Ta. Typically LED and Si are equal)

Register Address	Control Register							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
49h	LED Offset 3	LED Offset 2	LED Offset 1	LED Offset 0	Si Diode Offset 3	Si Diode Offset 2	Si Diode Offset 1	Si Diode Offset 0
	0*	0*	0*	0*	0*	0*	0*	0*

Note: *) Value by default

Table 6: Offset Codes for Tj-Ta Temperature Gradient Offset (both LED and Si per Table 5).

Temperature Offset ^{0}C (Ta-Tj)	Bit3– Bit 0	Temperature Offset ^{0}C (Ta-Tj)	Bit3– Bit 0	Temperature Offset ^{0}C (Ta-Tj)	Bit3– Bit 0	Temperature Offset ^{0}C (Ta-Tj)	Bit3– Bit 0
-40	1000	-20	1100	0	0000	20	0100
-35	1001	-15	1101	5	0001	25	0101
-30	1010	-10	1110	10	0010	30	0110
-25	1011	-5	1111	15	0011	35	0111

Table 7: T-code values vs. Temperature (for registers 4Ah & 4Bh)

Temperature ^{0}C	Bit4 – Bit 0	Temperature ^{0}C	Bit4 – Bit 0	Temperature ^{0}C	Bit4 – Bit 0	Temperature ^{0}C	Bit4 – Bit 0
25	01100	50	10001	75	10110	100	11011
30	01101	55	10010	80	10111	105	11100
35	01110	60	10011	85	11000	110	11101
40	01111	65	10100	90	11001	115	11110
45	10000	70	10101	95	11010	120	11111

Table 8: LDS8161 / 41 Temperature De-rating LUT Register Allocation
(data stored is ΔPWM code per each temperature point)

Register Address	Data bits 7 – 4	Data bits 3 – 0	Register Address	Data bits 7 – 4	Data bits 3 – 0
	ΔPWM code for temperature, ^{0}C			ΔPWM code for temperature, ^{0}C	
56h	30	25	5Ah	70	65
57h	40	35	5Bh	80	75
58h	50	45	5Ch	90	85
59h	60	55	5Dh	100	95

Table 9: Valid ΔPWM Codes vs. Number of Adjustment Steps for LDS8161/ 41 De-rating

Number of steps	Binary Code	Number of steps	Binary Code	Number of steps	Binary Code	Number of steps	Binary Code
Not Used	1000	**-4**	**1100**	**0**	**0000**	Not Used	0100
-7	**1001**	**-3**	**1101**	Not Used	0001	Not Used	0101
-6	**1010**	**-2**	**1110**	Not Used	0010	Not Used	0110
-5	**1011**	**-1**	**1111**	Not Used	0011	Not Used	0111

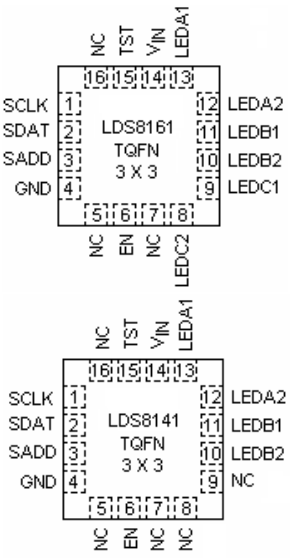
PROGRAMMING EXAMPLES

Operation	Register Address	Register Data	Command (hex)
Set 20 mA current at Bank LEDA	00h	A0h	XX 00 A0
Set 30 mA at LEDA, 30 mA at LEDB, & 20 mA at LEDC banks	00h	F0h F0h A0h	XX F0 F0 A0
Turn LEDs A1, B1 and C1 on, all others off	03h	15h	XX 03 15
Turn LEDs A2, B2, and C2 on, all others off	03h	24h	XX 03 24
Turn all LEDs on	03h	3Fh	XX 03 3F
Set Bank A,B,C PWM duty Cycle at 50% (-6 dB)	05h	DCh	XX 05 DC
Disable Temperature De-rating (DT_Adjust_disable)	1Eh	04h	XX 1E 04
Re-Enable Temperature De-rating	1Eh	00h	XX 1E 00
Short/open LED diagnostic request	19h	20h	XX 19 20
Read out LED short to GND status	1Ch		XX 1C YY
Read out LED short to V_{IN}/open status	1Dh		XX 1D YY
Set Standby Mode	1Fh	40h	XX 1F 40
Resume normal operation from standby mode	1Fh	00h	XX 1F 00
Calibration request (conduct temperature calibration)	1Fh	10h	XX 1F 10
Set LEDs in shutdown mode at junction temperature above 100^{0}C	4Ah	1Bh	XX 4A 1B
Set Ta-Tj offset for LED and Si Diode to -20ºC	49h	CCh	XX 49 CC
Software Reset (to default values) and/or clear of all registers	1Fh	80h	XX 1F 80

Note: XX – The LDS8160 I^{2}C customer-selected slave address followed by binary 1 for write command, i.e. if I^{2}C slave address is 001 0001 (see Table 8), XX = 0010 0011 (bin) = 23h
YY – The LDS8160 I^{2}C customer-selected slave address followed by binary 0 for read command, i.e. if I^{2}C slave address is 001 0001 (see Table 8), YY = 0010 0010 (bin) = 22h

PIN DESCRIPTION

Function	Pin Name	Pin #	
		8161	8141
I^2C Serial clock input	SCLK	1	1
I^2C Serial data input/output	SDAT	2	2
I^2C Serial interface Address Programming	SADD	3	3
Ground Reference	GND	4	4
Device enable (active high)	EN	6	6
LEDC2 anode terminal -8161 (NC for 8141)	LEDC2	8	
LEDC1 anode terminal -8161 (NC for 8141)	LEDC1	9	
LEDB2 anode terminal	LEDB2	10	10
LEDB1 anode terminal	LEDB1	11	11
LEDA2 anode terminal	LEDA2	12	12
LEDA1 anode terminal	LEDA1	13	13
Power Source Input; connect to battery or supply	V_{IN}	14	14
Test pin	TST	15	15
Not connect (no internal connect to the device)	NC	5, 7, 16	5, 7, 8, 9, 16
Connect to GND on the PCB	PAD	PAD	PAD



PIN FUNCTION

V_{IN} is the supply pin. A small 1µF ceramic bypass capacitor is required between the V_{IN} pin and ground near the device. The operating input voltage range is from 2.5 V to 5.5 V.

EN is the enable input for the entire device. Guaranteed levels of logic high and logic low are set at 1.3 V and 0.4V respectively. When EN is initially taken high, the device becomes enabled and may communicate through I^2C interface

SDAT is the I^2C serial data line. This is a bidirectional line allowing data to be written into and read from the four registers in the driver.

SCLK is the I^2C serial clock input.

SADD is I^2C Serial interface Addresses tie to either GND or VIN pin to allow choice of two salve addresses

GND is the ground reference for internal circuitry. The pin must be connected to the ground plane on the PCB.

LEDA1 – LEDC2 provide the internal regulated current source for each of the LED anodes. These pins enter high-impedance zero current state whenever the device is in shutdown mode. LEDC1 and LEDC2 are no connects (NC) for the LDS8141.

PAD is the exposed pad underneath the package. For best thermal performance, the tab should be soldered to the PCB and connected to the ground plane

TST is a test pin used by factory only. Leave it floating (no external connection)

BLOCK DIAGRAM

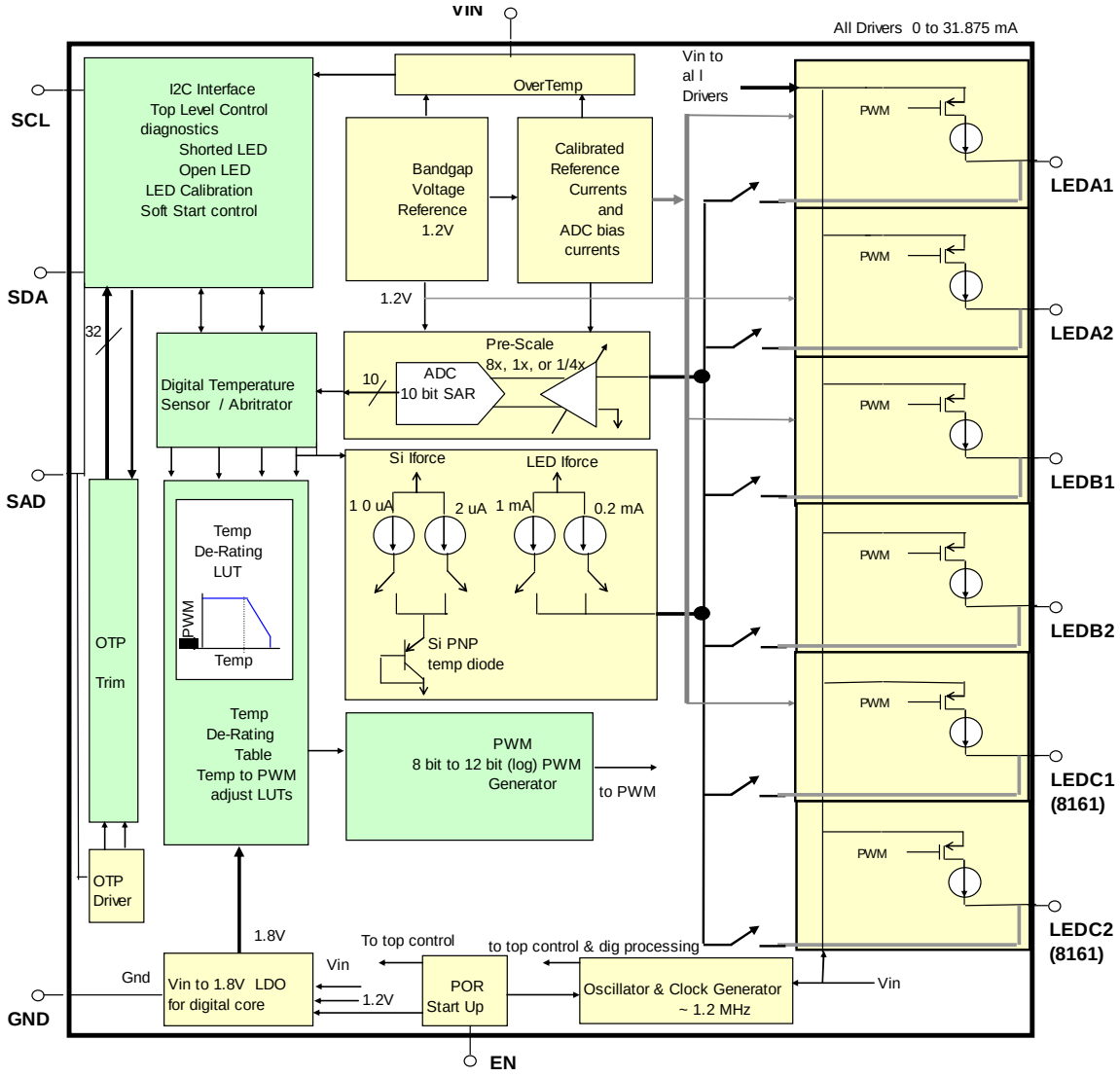


Figure 2: LDS8161/41 Functional Block Diagram

BASIC OPERATION

The LDS8161 / 41 may operate in following modes:

a) Normal Operation Mode
b) Normal Standby Mode
c) Programming Modes
d) Shutdown Mode

NORMAL OPERATION MODE

At power-up, V_{IN} should be in the range from 2.5 V to 5.5 V (max). If V_{IN} is slow rising, EN pin should be logic LOW at least until V_{IN} reaches a 2.5 V level.

When EN is taken HIGH, a soft-start power-up sequence begins and performs an internal circuits reset that requires less than 100 µs.

An initialization sequence then begins, taking less than 10 ms. This sequence determines the user-selected I^2C slave address, loads factory programmed settings, and conducts diagnostics for open/shorted LEDs.

At this point, the I^2C interface is ready for communication and the LDS8161/41 may be user-programmed. Upon programming completion for all required initial parameters and features' settings, a calibration command is given by setting bit 4 of the Control Register (1Fh) HIGH. This starts the calibration sequence of the LDS8161/41 LED-Sense™ temperature de-rating circuits and occurs simultaneous with a gradual ramp-up of LED PWM and current levels to the user programmed values. This initialization is completed in less than 250 ms in

the default soft-start ramp mode, or s less than 10 ms with the soft-start ramp mode disabled by setting bit 1 of the Configuration Register (1Eh) HIGH.

The calibration parameters for the temperature de-rating and all customer-set parameters remain intact until the part is reset or powered-down. Additionally, the user can re-calibrate LDS8161/41 during times when LED currents are brought to zero and thermally stabilized by programming the calibration command bit as discussed.

Factory preset values (upon completion of the power-up initialization) are as follow (see Table 3):

a) All LEDs are disabled and $I_{LEDA, B, C} = 0$;

b) WLED mode (i.e. 1 De-rating LUT) selected and 1 PWM generator drives all 3 banks (8160) or 2 banks (8141).

c) PWM dimming control is enabled with reset duty cycle = 0%.

d) LED-Sense™ temperature de-rating is disabled with the LUT for a Nichia NSSW020BT WLED;

e) Soft start-up PWM ramp feature enabled;

If the factory default loaded de-rating curve is used as shown in Figure 7, then following Table 10 identifies the necessary registers and initialization required after the power-up or reset state to operate the LDS8161/41.

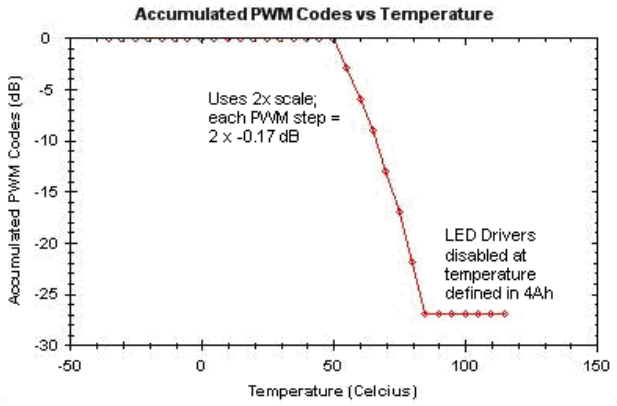


Figure 3: LDS8161/41 Default De-rate Curve

Table 10: Recommended Register Load Sequence for LDS8161/41 (Using the Factory Default De-Rating LUT)

Reg Load Sequence #	Reg (hex)	Value at Start-up (hex)	Value (hex)	Comments
1	49h	00h	CCh	Ta-Tj 0ffset = -20ºC
2	4Ah	1Ch	18h	Set LED Shutdown Temp = 85ºC (Ta referenced)
3	4Bh	31h	20h	Set 2x de-rate mode starting at 55C
4	A0h	38h	36h	Load Si Diode K factor for - 1.71mV/C
5	A2h	70h	User Loads Per LED Used	User loads LED K factor @ 1mA I_F 29h = -1.3mV/C for Nichia NSSW020BT
6	C0h	41h	40h	Load Si Diode η factor = 1.0
7	D4h	19h	04h	Load Si Diode Rs = 68 ohms
8	D6h	3Fh	User Loads Per LED Used	User loads LED Rs 61h = 17 ohms for Nichia NSSW020BT
9	1Eh	84h	00h	Initialize Configuration Register
10	1Fh	00h	10h	User issues temp calibration command
11	00h	00h	User Loads Ex: F0h = 30mA	User sets Current for Bank A.
12	01h	00h	Uer Loads Ex: F0h = 30mA	User sets Current for Bank A.
13	02h	00h	User Loads Ex: F0h = 30mA	User sets Current for Bank B.
14	03h	00h	User Loads Ex: 3Fh = all channels	User enabled LED channels
15	05h	00h	User Loads Ex: FEh = 91% DC	User sets PWM duty cycle for all channels

The de-rate table stored in the correction LUT is referenced to the LED Tj. Register 49h can be used to apply the Ta-Tj temperature offset between the ambient and LED junction temperature. This can effect a +/- shift of the de-rating curve in the Temperature axis to reference the de-rating profile to ambient, and/or set the start of de-rating to the desired ambient temperature level to accommodate different LEDs and current/power levels. The default table will de-rate the current ~ - 9.2 dB (0.348x) from its user set low temperature maximum level over 35ºC (from the start of the de-rate temperature). For example, if the LED current is set to 30mA prior to de-rating, and de-rating begins at 55ºC, at 85ºC the current is de-rated to 0.348 x 30mA = 10.4mA.

Register 4Ah sets the LEDs shutdown junction temperature per the T-codes provided in Table 7. When this temperature is exceeded, all of the LED current driver channels are disabled to insure no damage to the LEDS. Additionally, an LED OT (over temperature) status flag is set HIGH in Bit 7 of the enable channel register 03h. If the flag is set the user can re-enable the channels by re-writing to the channel enable bits in register 03h, however the OT flag will remain HIGH, until the device is power sequenced, reset, or placed in the shutdown mode.

If a Ta-Tj offset is used other than 00h (i.e. 0ºC) in register, 49h, than the shutdown junction temperature loaded in 4Ah should also include this offset. This insures the LED shutdown is also properly referenced to ambient level, Ta.

LED Current Setting

Current setting registers 00h – 02h should be programmed using I^2C interface and desired LEDs should be enabled using register 03h before LEDs turn on.

The standard I^2C interface procedure is used to program I_{LED} current (see chapter "I^2C INTERFACE"). LDS8161/41 should be addressed with slave address chosen (see Table 11 for accessible slave addresses) followed by register address (00h, 01h, or 02h) and data that represents the code for the desired LED current.

Code for LED current is determined as I_{LED}/0.125 mA in hex format, i.e. 20 mA current code = 20/0.125 = 160 (dec) = A0h.

The maximum current setting is 31.875 mA. Since the LDS8161/41 is a low drop-out LDO based linear LED driver, when using maximum current levels, users should select LEDs with V_F < 3.3V to maximize operation with Li-ion batteries.

To turn LEDs ON/OFF register 03h should be addressed with data that represents the desired combination of LEDs turned ON/OFF (see Table 1); i.e. if LEDC1, LEDC2, LEDA1, LEDA2 should be ON, and LEDB1, LEDB2 should be OFF, binary code that should be written into register 03h is 110011 (bin) = 33h.

The LDS8161/41 allows two ways for LED current setting and dimming - analog (static) dimming using the 8 bit current DACs, and dynamic dimming via the integrated 12-bit digital PWM. Combining both methods allows for total dimming capability of > 16,384:1

Analog dimming using the current setting DACs discussed via registers 00h – 02h is referred to as the static mode. Digital dimming using the internal PWM generator changes the duty cycle per the value set in register 05h and therefore adjusts the average LED current. This is referred to as dynamic mode.

For dynamic mode, the LDS8161/41 integrates a digital PWM generator that operates at a frequency of ~ 285 Hz. It operates in Logarithmic Mode. The PWM generator has a 12-bit resolution and it can be programmed with an 8-bit code to provide 256 internally mapped 12-bit logarithmic duty cycle steps to adjust the dimming level

The advantage of PWM dimming is stable LED color temperature / wavelength that is determined by the maximum static mode LED current value set by registers 00h – 02h. The integrated PWM generator reduces the system requirement to provide a continuous pulsed waveform.

To use the dynamic PWM mode for LED current setting, the maximum I_{LED} value should first be set by current DAC registers 00h – 02h as described above for static mode, and desired dimming / duty cycle can be set by register 05h. The logarithmic operating mode provides a dimming resolution of approximately -0.17 dB per step with 0dB dimming (i.e. 100% duty cycle) at the 256th step (i.e. FFh), and 0% duty cycle (~ -80 dB dimming) at 00h.

LED-Sense™ High Temperature Current De-rating

The LDS8161/41 integrates the IXYS LED-Sense™ temperature measurement and high temperature current de-rating algorithm to insure LED reliability and operating lifetimes.

LED current is de-rated via reductions in PWM duty cycle to meet LED vendor power dissipation vs. LED junction temperature specifications.

User programmable de-rating adjustments are stored in a correction LUT comprised of eight 8-bit registers from 56h to 5Dh. Each register stores a 4-bit

adjustment code for two 5ºC temperature steps in its lower (bits 3:0) and higher (bits 7:4) nibble. User loadable de-rating codes in the 1x scale mode represent 0 to -7 PWM de-rating steps. In the 2 x scale mode the de-rating codes represent 0 to -14 PWM steps.

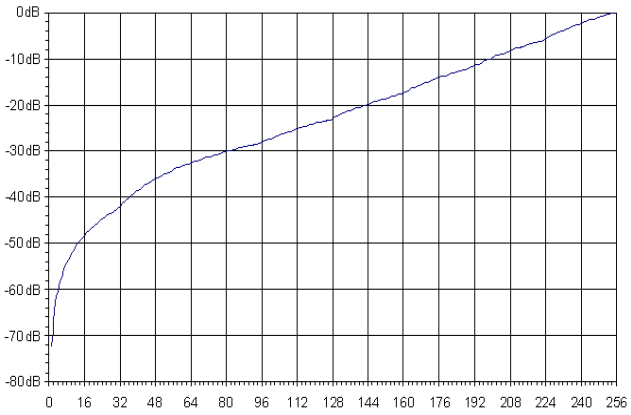


Figure 4: Dynamic Mode Dimming in Logarithmic Mode in dB vs. register 05h data (0dB dimming = full LED brightness)

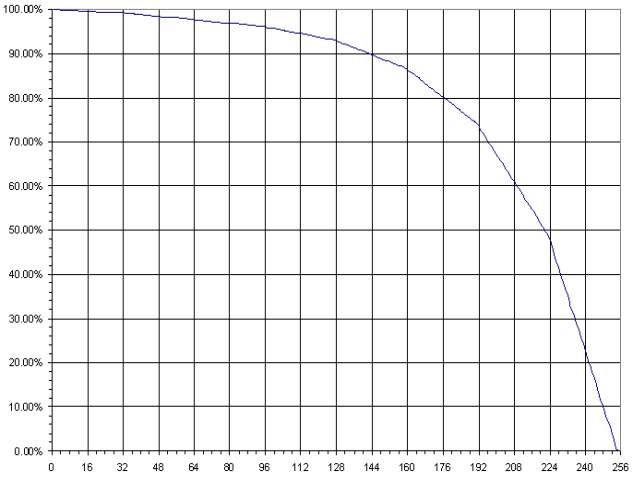


Figure 5: Dynamic Mode Dimming in Logarithmic Mode in percent vs. register 05h data (0% dimming = full LED brightness)

Additionally, the LED drivers are disabled (i.e. 0 DC current) if the measured LED junction temperature exceeds a preset value that is loaded in register 4Ah. The default is set for 1Ch = 105ºC Tj.

The LED-Sense™ engine periodically measures the LED junction temperature on channel LEDA1 and encodes the value into 5-bit T-codes representing 5^0C temperature intervals from -35 to +120^0C.

The measured T-code value addresses the stored ΔPWM de-rating codes stored in the LUT registers to adjust the PWM duty cycle. Therefore, this reduces the average current through the LEDs as defined by the LUT table.

The user loads specific ΔPWM de-rating codes into the LUT (56h – 5Dh) for every 5ºC temperature step from 25ºC to 100ºC to meet desired current and power vs. LED junction temperature.

LUT de-rating correction codes are subtracted from the user-set duty cycle/dimming code (dynamic mode) loaded in register 05h to maintain reliable LED current levels.

The LDS8161/41 includes a 10-bit ADC and digital processing engine to determine LED temperatures approximately every 2.5 seconds. The proprietary LED-Sense™ algorithm allows direct measurement of LED junction temperatures on the LEDA1 driver channel, without the need for an external temperature sensor. Additionally an on-chip silicon temperature sensing diode is also measured to enhance temperature estimation accuracy.

Additionally, the ADC and processing circuits are time-multiplexed to provide an LED opens and shorts diagnostic feature.

A Factory loaded de-rating curve is valid upon reset, and provide the de-rating profile shown at Figure 3.

I²C Interface

The LDS8160 uses a 2-wire serial I²C-bus interface. The SDAT and SCLK lines comply with the I²C electrical specification and should be terminated with pull-up resistors to the logic voltage supply. When the bus is not used, both lines are high. The device supports a maximum bus speed of 400kbit/s. The serial bit sequence is shown at *REGISTER DEFINITION AND PROGRAMMING* section for read and write operations into the registers. Read and write instructions are initiated by the master controller/CPU and acknowledged by the slave LED driver.

The LDS8161/41 allows user to choose between two I²C addresses by connecting SADD pin (#3) either to ground, or V_{IN} pin (see Table).

Table 11: LDS8161/41 I²C Slave Addresses

SADD pin connected to	I²C Address	
	Binary code	Hex
Ground	001 0001	11h
V_{IN}	101 0101	55h

For further details on the I²C protocol, please refer to the I²C-Bus Specification, document number 9398-393-40011, from Philips Semiconductors.

Unused LED Channels

For applications with less than six (8161) or four (8141) LEDs, the unused LED channels can be disabled via the I^2C interface by addressing register 03h with data that represents the desired combination of LEDs turned ON/OFF (see Table 1).

The LDS8161/41 unused LED outputs can be left open.

Parallel-Connected LED Channels for Higher Current LEDs

In higher power LED applications requiring more than 31.875 mA DC current, LED driver channels can be connected in parallel.

For example, ½ watt, 150 mA LEDs can be driven with the LDS8161 by paralleling all 6 channels with 25 mA per channel. Likewise, the LDS8141 can drive up to 127.5 mA by connecting all 4 channels in parallel at the maximum 31.875 mA per channel.

LED short/open protection

The LDS8161/41 runs a LED short/open diagnostic routine upon the power up sequence. It detects both LED pins shorted to ground and LED pins that are open or shorted to V_{IN} (fault conditions).
The results for short to GND detection are stored in Diagnostics Register 1Ch. Bits from bit 5 to bit 0 indicate a short status as bit = 1 for LEDC2 - LEDA1 respectively. A short to GND is detected, if the measured LED pin voltage is less than ~ 0.14 V independent of the programmed LED current. Every channel, detected as shorted, is disabled

Test results for open or short to V_{IN} LED pins are stored in Diagnostics Register 1Dh, Bits from bit 5 to bit 0 represent LEDC2 - LEDA1 respectively with bit = 1 indicates fault condition at this particular LED pin.

An open LED pin fault causes no harm in the LDS8161/41 or the LED as the high side driver has no current path from V_{IN} or GND. Therefore, the fault detection status indicates only in the 1Dh diagnostic register, and no further action is required.

In the case of an LED directly shorted to V_{IN}, the full V_{IN} voltage will be connected to the LED and current can flow independent of the LDS8161/41 LED driver circuit directly to GND. The LDS8161/41 will detect the fault and indicate the status in Register 1Dh, however further action needs taken at the system level to shutdown V_{IN} power to prevent possible damage to the LED. The combined series resistance of the LED (typically ~ 10Ω or more) and additional board series resistance will result in current limiting but not sufficient to insure no damage to low power LEDs.

Besides the power-up diagnostic sequence, the user can re-initiate a diagnostic command at any time by setting bit 5 of the Digital Test Modes Register, 19h, to HIGH.

The LDS8161/41 restores LED current to programmed value at channels with detected shorts to GND after the fault condition is removed and device restarted.

Over-Temperature Protection

If the die temperature exceeds +150°C, the driver will enter shutdown mode. The LDS8161/41 requires restart after die temperature falls below 130°C.

LED Selection

If the power source is a Li-ion battery, LEDs with V_F = 1.9 V - 3.3 V are recommended to achieve highest efficiency performance and extended operation on a single battery charge.

External Components

The driver requires one external 1 µF ceramic capacitors (C_{IN}) X5R or X7R type.

CONFIGURATION MODES

The LDS8161/41 allows the option to choose special operating modes overwriting content of Configuration Register 1Eh (see Table 2).

Bit 1 allows bypass soft start / ramp down if fast raising/falling LED current required.

Bit 2 allows disable LED temperature compensation if desired.

The LDS8161/41 also provides the option for using an external remote temperature-sensing diode device such as a 2N3904. To use this option the diode anode should be connected to channel LEDA1. The cathode connected to GND. In this case, channel LEDA1 should be disabled via register 03h and it cannot operate as an LED current source.

Bits 0, 3, 4, 5, 6, and 7 of the Configuration Register 1Eh are for factory use only and should be set to 0 or the user should use the power-on-reset values.

STANDBY MODES

The LDS8161/41 has a “soft” standby or sleep mode, which the customer may set by I^2C interface addressing register 1Fh with bit 6 = 1 (see Table 4).

In the Standby Mode, the I^2C interface remains active and all registers retain their programmed information.

In Standby Mode the LED drivers and internal clock are powered off; however, internal regulators and reference circuits remain active to insure power to the digital sections to hold register values and maintain I^2C interface communications. This results in standby current ~ 125 µA typical. For this mode, the EN pin should be logic HIGH with signal level from 1.3 to V_{IN} voltage.

SHUTDOWN MODE

To set LDS8161/41 into the shutdown mode, the EN pin should be logic low more than 10 ms. The LDS8161/41 shutdown current is less than 1 µA.

The LDS8161/41 wakes up from shutdown mode with factory-preset default data. To preserve customer-programmed data, use Normal standby mode.

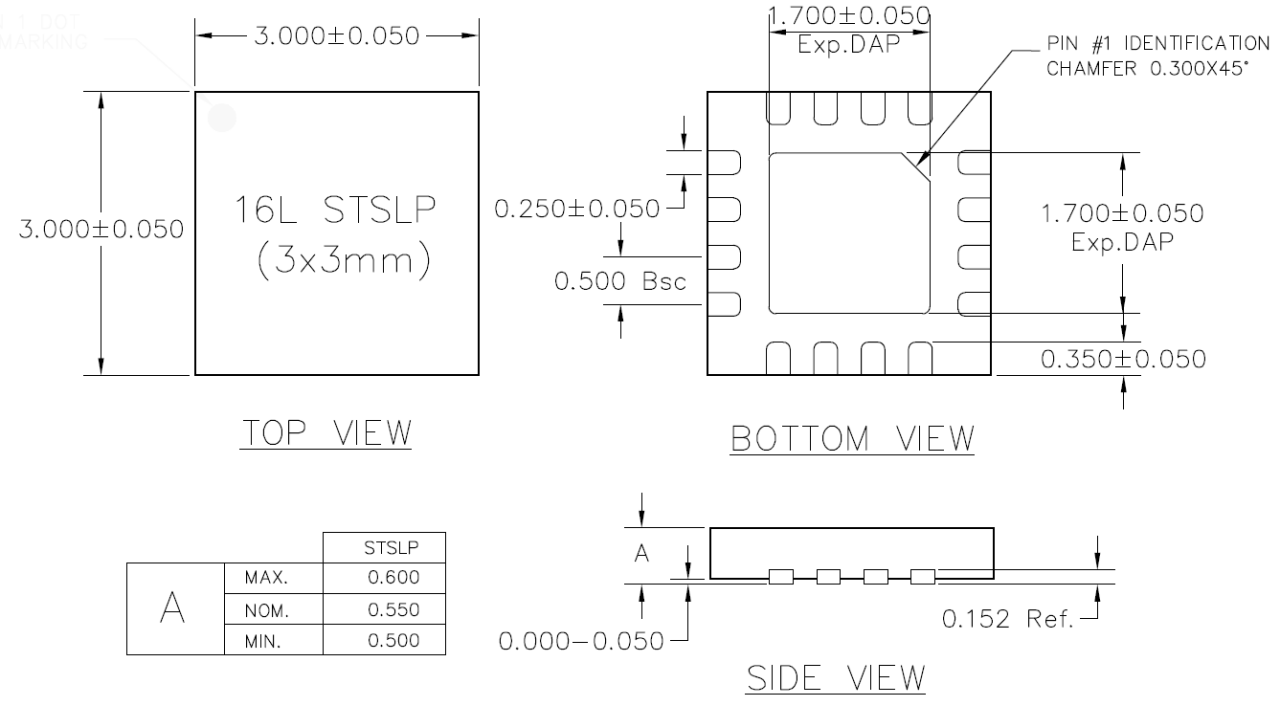
PROGRAMMING MODES

The LDS8161/41 is factory preprogrammed with a default temperature de-rating LUT that works with the Nichia NSSW020BT WLEDs or equivalent. However, specific LEDs and other user system conditions may require user programming of the temperature compensation LUTs and other LED specific parameters.

After initialization and user programming the user should conduct an I^2C calibration sequence command by writing Bit 4 = 1 in the Control register 1Fh. This conducts a real time calibration of the initial starting temperature and actual LED parameters. Upon completion, Bit 4 will be internally reset to 0, and the LDS8161/41 is ready for use.

PACKAGE DRAWING AND DIMENSIONS

16L (STSLP), 3mm x 3mm x 0.55mm, 0.5mm PITCH



		STSLP
A	MAX.	0.600
	NOM.	0.550
	MIN.	0.500

Note:

1. All dimensions are in millimeters
2. Complies with JEDEC Standard MO-220

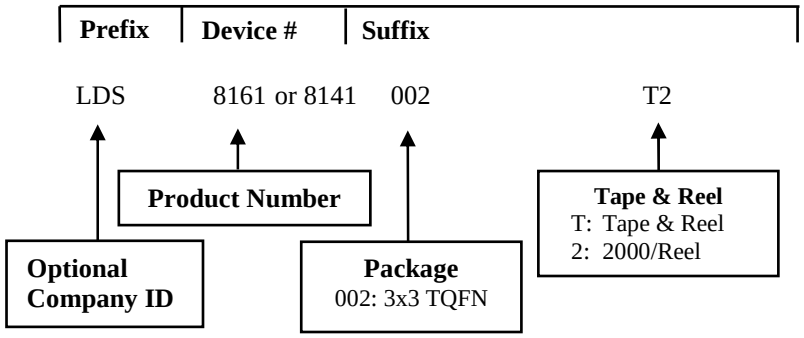
ORDERING INFORMATION

Part Number	Package	Package Marking
LDS8161 002-T2	TQFN-16 3 x 3mm(1)	8161
LDS8141 002-T2	TQFN-16 3 x 3mm(1)	8141

Notes:

1. Matte-Tin Plated Finish (RoHS-compliant)
2. Quantity per reel is 2000

EXAMPLE OF ORDERING INFORMATION



Notes:

1) All packages are RoHS-compliant (Lead-free, Halogen-free).
2) The standard lead finish is Matte-Tin.
3) The device used in the above example is a LDS8161A 002–T2 (3x3 TQFN, Tape & Reel).
4) For additional package and temperature options, please contact your nearest IXYS Corp. Sales office.

Appendix 1

Table 5 Dynamic Mode Dimming in Logarithmic Mode vs. register 05h data

# of steps	Hex code	Dimming, dB	Dimming, %	# of steps	Hex code	Dimming, dB	Dimming, %	# of steps	Hex code	Dimming, dB	Dimming, %
0	00		100	32	20	-41.9	99.19	64	40	-32.6	97.63
1	01	-72.3	99.98	33	21	-41.4	99.15	65	41	-32.4	97.58
2	02	-66.3	99.95	34	22	-40.9	99.10	66	42	-32.2	97.53
3	03	-62.8	99.93	35	23	-40.5	99.05	67	43	-32.1	97.49
4	04	-60.3	99.90	36	24	-40.1	99.00	68	44	-31.9	97.44
5	05	-58.3	99.88	37	25	-39.6	98.95	69	45	-31.7	97.39
6	06	-56.7	99.85	38	26	-39.2	98.90	70	46	-31.6	97.34
7	07	-55.4	99.83	39	27	-38.9	98.85	71	47	-31.4	97.29
8	08	-54.3	99.80	40	28	-38.5	98.80	72	48	-31.3	97.24
9	09	-53.2	99.78	41	29	-38.2	98.75	73	49	-31.1	97.19
10	0A	-52.3	99.76	42	2A	-37.8	98.71	74	4A	-30.9	97.14
11	0B	-51.5	99.73	43	2B	-37.5	98.66	75	4B	-30.8	97.09
12	0C	-50.7	99.71	44	2C	-37.2	98.61	76	4C	-30.7	97.05
13	0D	-50	99.68	45	2D	-36.9	98.56	77	4D	-30.5	97.00
14	0E	-49.4	99.66	46	2E	-36.6	98.51	78	4E	-30.4	96.95
15	0F	-48.8	99.63	47	2F	-36.3	98.46	79	4F	-30.2	96.90
16	10	-48.2	99.61	48	30	-36.1	98.41	80	50	-30.1	96.85
17	11	-47.7	99.58	49	31	-35.8	98.36	81	51	-30	96.80
18	12	-47.2	99.56	50	32	-35.5	98.32	82	52	-29.8	96.75
19	13	-46.7	99.54	51	33	-35.3	98.27	83	53	-29.7	96.70
20	14	-46.3	99.51	52	34	-35	98.22	84	54	-29.6	96.66
21	15	-45.9	99.49	53	35	-34.8	98.17	85	55	-29.5	96.61
22	16	-45.5	99.46	54	36	-34.6	98.12	86	56	-29.3	96.56
23	17	-45.1	99.44	55	37	-34.4	98.07	87	57	-29.2	96.51
24	18	-44.7	99.41	56	38	-34.1	98.02	88	58	-29.1	96.46
25	19	-44.4	99.39	57	39	-33.9	97.97	89	59	-29	96.41
26	1A	-44	99.37	58	3A	-33.7	97.92	90	5A	-28.8	96.36
27	1B	-43.7	99.34	59	3B	-33.5	97.88	91	5B	-28.7	96.31
28	1C	-43.4	99.32	60	3C	-33.3	97.83	92	5C	-28.6	96.26
29	1D	-43.1	99.29	61	3D	-33.1	97.78	93	5D	-28.5	96.22
30	1E	-42.8	99.27	62	3E	-32.9	97.73	94	5E	-28.4	96.17
31	1F	-42.5	99.24	63	3F	-32.8	97.68	95	5F	-28.3	96.12

Continued

Table 10 Dynamic Mode Dimming in Logarithmic Mode vs. register 05h data

Continue

# of steps	Hex code	Dimming, dB	Dimming, %	# of steps	Hex code	Dimming, dB	Dimming, %	# of steps	Hex code	Dimming, dB	Dimming, %
96	60	-28.1	96.02	128	80	-22.9	92.80	160	A0	-17.4	86.35
97	61	-27.9	95.92	129	81	-22.7	92.60	161	A1	-17.1	85.96
98	62	-27.7	95.83	130	82	-22.5	92.41	162	A2	-16.9	85.57
99	63	-27.5	95.73	131	83	-22.2	92.21	163	A3	-16.6	85.18
100	64	-27.3	95.63	132	84	-22	92.02	164	A4	-16.4	84.79
101	65	-27.1	95.53	133	85	-21.8	91.82	165	A5	-16.2	84.40
102	66	-26.9	95.43	134	86	-21.6	91.63	166	A6	-16	84.01
103	67	-26.7	95.34	135	87	-21.4	91.43	167	A7	-15.8	83.62
104	68	-26.5	95.24	136	88	-21.2	91.24	168	A8	-15.6	83.23
105	69	-26.3	95.14	137	89	-21	91.04	169	A9	-15.4	82.84
106	6A	-26.2	95.04	138	8A	-20.8	90.84	170	AA	-15.2	82.45
107	6B	-26	94.95	139	8B	-20.6	90.65	171	AB	-15	82.06
108	6C	-25.8	94.85	140	8C	-20.5	90.45	172	AC	-14.8	81.67
109	6D	-25.7	94.75	141	8D	-20.3	90.26	173	AD	-14.6	81.27
110	6E	-25.5	94.65	142	8E	-20.1	90.06	174	AE	-14.4	80.88
111	6F	-25.3	94.56	143	8F	-20	89.87	175	AF	-14.3	80.49
112	70	-25.2	94.46	144	90	-19.8	89.67	176	B0	-14.1	80.10
113	71	-25	94.36	145	91	-19.6	89.48	177	B1	-13.9	79.71
114	72	-24.9	94.26	146	92	-19.5	89.28	178	B2	-13.8	79.32
115	73	-24.7	94.17	147	93	-19.3	89.09	179	B3	-13.6	78.93
116	74	-24.6	94.07	148	94	-19.2	88.89	180	B4	-13.4	78.54
117	75	-24.5	93.97	149	95	-19	88.70	181	B5	-13.3	78.15
118	76	-24.3	93.87	150	96	-18.9	88.50	182	B6	-13.1	77.76
119	77	-24.2	93.77	151	97	-18.7	88.31	183	B7	-13	77.37
120	78	-24	93.68	152	98	-18.6	88.11	184	B8	-12.8	76.98
121	79	-23.9	93.58	153	99	-18.4	87.92	185	B9	-12.7	76.59
122	7A	-23.8	93.48	154	9A	-18.3	87.72	186	BA	-12.5	76.20
123	7B	-23.7	93.38	155	9B	-18.1	87.52	187	BB	-12.4	75.81
124	7C	-23.5	93.29	156	9C	-18	87.33	188	BC	-12.3	75.42
125	7D	-23.4	93.19	157	9D	-17.9	87.13	189	BD	-12.1	75.02
126	7E	-23.3	93.09	158	9E	-17.7	86.94	190	BE	-12	74.63
127	7F	-23.2	92.99	159	9F	-17.6	86.74	191	BF	-11.8	74.24

Continued

Table 10 Dynamic Mode Dimming in Logarithmic Mode vs. register 05h data

Continue

# of steps	Hex code	Dimming, dB	Dimming, %	# of steps	Hex code	Dimming, dB	Dimming, %
192	C0	-11.6	73.46	224	E0	-5.7	47.68
193	C1	-11.3	72.68	225	E1	-5.4	46.12
194	C2	-11.1	71.90	226	E2	-5.2	44.56
195	C3	-10.9	71.12	227	E3	-4.9	42.99
196	C4	-10.6	70.34	228	E4	-4.7	41.43
197	C5	-10.4	69.56	229	E5	-4.5	39.87
198	C6	-10.2	68.77	230	E6	-4.3	38.31
199	C7	-10	67.99	231	E7	-4	36.74
200	C8	-9.8	67.21	232	E8	-3.8	35.18
201	C9	-9.5	66.43	233	E9	-3.6	33.62
202	CA	-9.3	65.65	234	EA	-3.4	32.06
203	CB	-9.2	64.87	235	EB	-3.2	30.49
204	CC	-9	64.09	236	EC	-3	28.93
205	CD	-8.8	63.31	237	ED	-2.8	27.37
206	CE	-8.6	62.52	238	EE	-2.7	25.81
207	CF	-8.4	61.74	239	EF	-2.5	24.24
208	D0	-8.2	60.96	240	F0	-2.3	22.68
209	D1	-8.1	60.18	241	F1	-2.1	21.12
210	D2	-7.9	59.40	242	F2	-2	19.56
211	D3	-7.7	58.62	243	F3	-1.8	17.99
212	D4	-7.6	57.84	244	F4	-1.6	16.43
213	D5	-7.4	57.06	245	F5	-1.5	14.87
214	D6	-7.3	56.27	246	F6	-1.3	13.31
215	D7	-7.1	55.49	247	F7	-1.2	11.74
216	D8	-6.9	54.71	248	F8	-1	10.18
217	D9	-6.8	53.93	249	F9	-0.8	8.62
218	DA	-6.7	53.15	250	FA	-0.7	7.06
219	DB	-6.5	52.37	251	FB	-0.6	5.49
220	DC	-6.4	51.59	252	FC	-0.4	3.93
221	DD	-6.2	50.81	253	FD	-0.3	2.37
222	DE	-6.1	50.02	254	FE	-0.1	0.81
223	DF	-6	49.24	255	FF	0	0.00

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