MOTOROLA

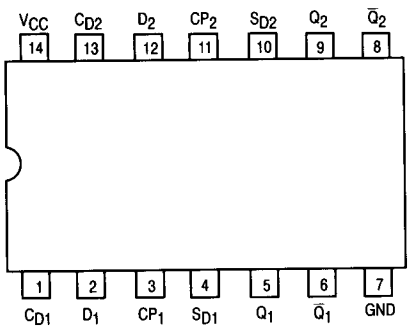
Dual D-Type Flip-Flop With Clear and Preset

ELECTRICALLY TESTED PER:
MIL-M-38510/30102

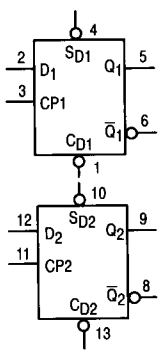
The 54LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high-speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

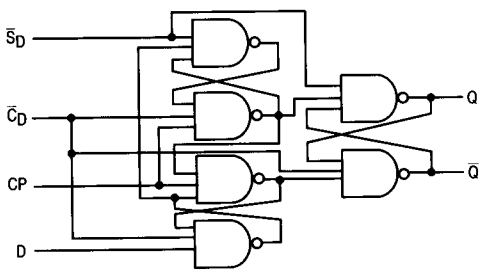
CONNECTION DIAGRAM



LOGIC SYMBOL



LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

* Both outputs will be High while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go High simultaneously. If the levels at the set and clear near V_{IL} maximum then we cannot guarantee to meet the minimum level for V_{OH}.

Military 54LS74A

AVAILABLE AS:

1) JAN: JM38510/30102BXA
2) SMD: N/A
3) 883: 54LS74A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
C_{D1}	1	1	2	GND
D_1	2	2	3	V_{CC}
CP_1	3	3	4	V_{CC}
S_{D1}	4	4	6	GND
Q_1	5	5	8	V_{CC}
$\overline{Q}_1$	6	6	9	V_{CC}
GND	7	7	10	GND
$\overline{Q}_2$	8	8	12	V_{CC}
Q_2	9	9	13	V_{CC}
S_{D2}	10	10	14	GND
CP_2	11	11	16	V_{CC}
D_2	12	12	18	V_{CC}
C_{D2}	13	13	19	GND
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

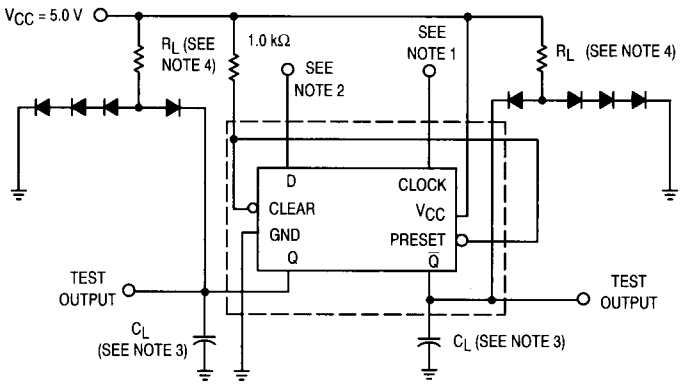
MODE SELECT – TRUTH TABLE

Operating Mode	Inputs			Outputs	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

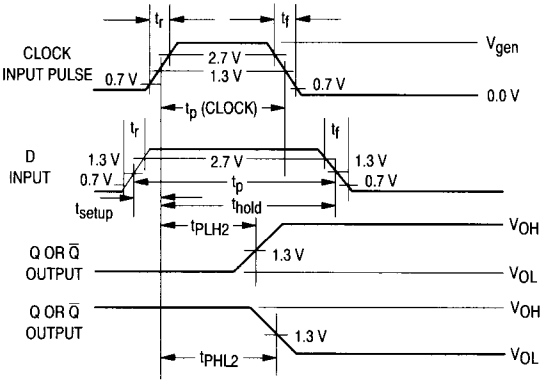
H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h, (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

5

SYNCHRONOUS SWITCHING TEST CIRCUIT



WAVEFORMS

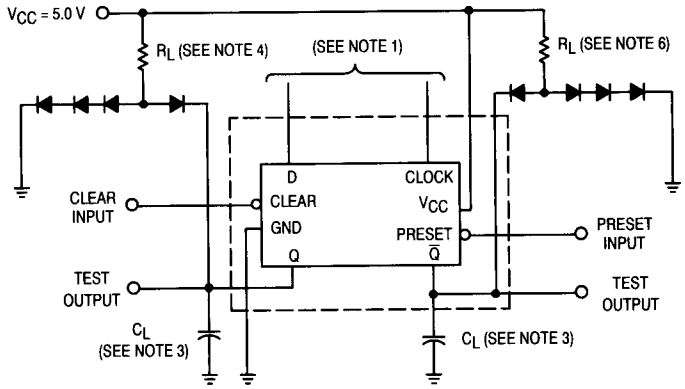


NOTES:

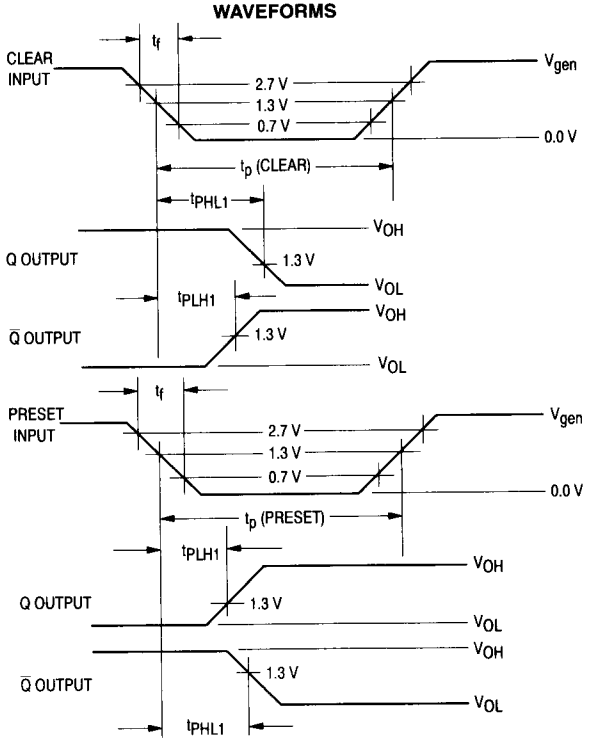
1. Clock input pulse has the following characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, t_f = 6.0 ns, t_p (clock) = 30 ns and PRR ≤ 1.0 MHz. When testing f_{MAX} see table, t_p (clock) ≤ 30 ns, $t_r = t_f \leq 6.0$ ns.
2. D input has the following characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, t_{setup} = 20 ns, t_{hold} = 5.0 ns, t_p = 25 ns and PRR is 50% of the clock PRR. When testing f_{MAX}, $t_r = t_f \leq 6.0$ ns.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.
5. All diodes are 1N3064, or equivalent.

5

CLEAR & PRESET SWITCHING TEST CIRCUIT



WAVEFORMS



NOTES:

1. Clear or preset inputs dominate regardless of the state of the clock or D inputs.
2. Clear or preset input pulse characteristics: V_{gen} = 3.0 V, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz, t_p (clear) = t_p (preset) = 35 ns.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied (see table).

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IN} = 2.0 V, V_{IL} = 0.7 V, CP = GND and (See Note 1).
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.7 V, CP = (See Note 1) and GND.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.
I_{IH1}	Logical "1" Input Current (D inputs)		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = 4.5 V, CD = GND.
I_{IHH1}	Logical "1" Input Current (D inputs)		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, CD = GND, other inputs = 4.5 V.
I_{IH2}	Logical "1" Input Current (CP & SD)		40		40		40	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = 4.5 V, CD = GND.
I_{IHH2}	Logical "1" Input Current (CP & SD)		200		200		200	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs = 4.5 V, CP = (See Note 2).
I_{IH3}	Logical "1" Input Current (CD inputs)		60		60		60	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, CP = (See Note 2), SD = 4.5 V, D = GND.
I_{IHH3}	Logical "1" Input Current (CD inputs)		300		300		300	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, CP = (See Note 2), SD = 4.5 V, D = GND.
I_{IL1}	Logical "0" Input Current (D inputs)	− 135	− 370	− 135	− 370	− 135	− 370	µA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, SD = GND, other inputs = 4.5 V.
I_{IL2}	Logical "0" Input Current (CP inputs)	− 120	− 360	− 120	− 360	− 120	− 360	µA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, CD = 4.5 V, other inputs = GND.
I_{IL3}	Logical "0" Input Current (SD inputs)	− 280	− 760	− 280	− 760	− 280	− 760	µA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs = GND.
I_{IL4}	Logical "0" Input Current (CD inputs)	− 280	− 760	− 280	− 760	− 280	− 760	µA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, SD = GND, other inputs = 4.5 V.
I_{OS}	Output Short Circuit Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, CD = GND, V_{OUT} = GND, other inputs are open.
I_{CC}	Power Supply Current		8.0		8.0		8.0	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are open.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTES:

1. 

2. 

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay SD_n or CD_n to Q_n to $\overline{Q}_n$	5.0 —	46 40	5.0 —	59 54	5.0 —	59 54	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH1} t_{PLH1}	Propagation Delay SD_n or CD_n to Q_n to $\overline{Q}_n$	5.0 —	30 25	5.0 —	39 34	5.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PHL2}	Propagation Delay /Data-Output $\overline{\ }$ CP_n to Q_n or $\overline{Q}_n$	5.0	46	5.0	59	5.0	59	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH2}	Propagation Delay /Data-Output $\overline{\ }$ CP_n to Q_n or $\overline{Q}_n$	5.0	30	5.0	39	5.0	39	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	20		20		20		MHz	V_{CC} = 5.0 V, V_{IN} = 2.7 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	25						MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.

NOTES:

1. f_{MAX}, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C_L = 15 pF are guaranteed but not tested.

5