ICS840004I
FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS840004I is a 4 output LVCMOS/LVTTL Synthesizer optimized to generate Fibre Channel reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 26.5625MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL1:0): 212.5MHz, 159.375MHz, 156.25MHz, 106.25MHz, and 53.125MHz. The ICS840004I uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical random rms phase jitter, easily meeting Fibre Channel jitter requirements. The ICS840004I is packaged in a small 20-pin TSSOP package.

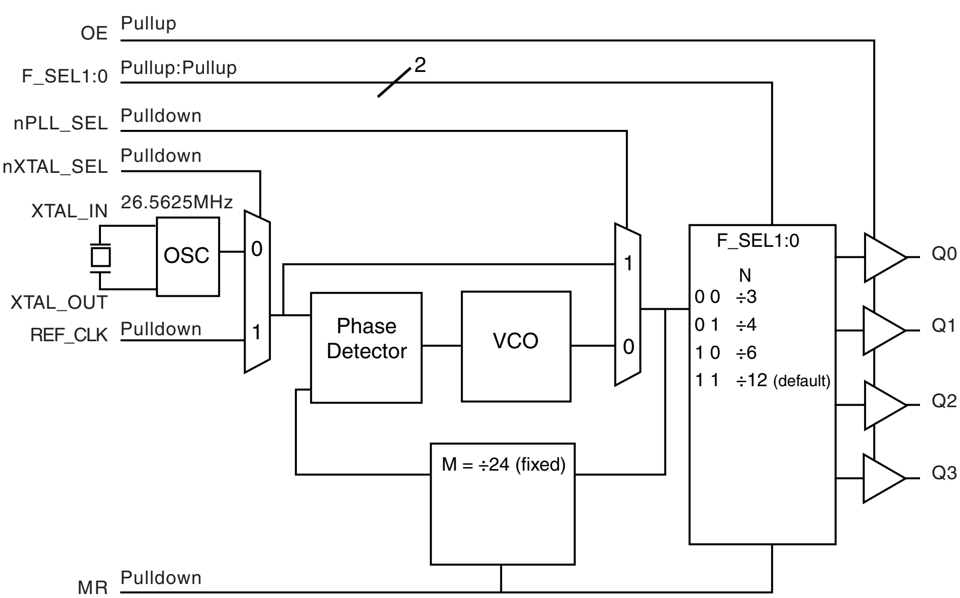
FEATURES

- Four LVCMOS/LVTTL outputs, 17Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS single-ended input
- Supports the following input frequencies: 212.5MHz, 159.375MHz, 156.25MHz, 106.25MHz and 53.125MHz
- VCO range: 560MHz - 700MHz
- RMS phase jitter @ 212.5MHz (2.55MHz - 20MHz): 0.49ps (typical)
- Output supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

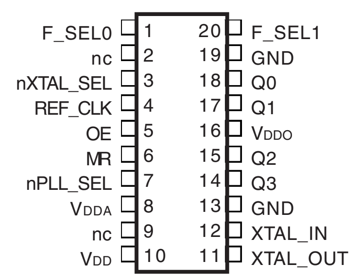
FREQUENCY SELECT FUNCTION TABLE

Inputs						Output Frequency Range (MHz)
Input Frequency (MHz)	F_SEL1	F_SEL0	M Divider Value	N Divider Value	M/N Ratio Value	
26.5625	0	0	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125 (default)
26.04166	0	1	24	4	6	156.25

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840004I
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	F_SEL0	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
2, 9	nc	Unused		No connect.
3	nXTAL_SEL	Input	Pulldown	Selects between the crystal or REF_CLK inputs as the PLL reference source. When HIGH, selects REF_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.
4	REF_CLK	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
5	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the otuputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	PLL Bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = reference clock frequency/N output divider. LVCMOS/LVTTL interface levels.
8	V_{DDA}	Power		Analog supply pin.
10	V_{DD}	Power		Core supply pin.
11, 12	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.
13, 19	GND	Power		Power supply ground.
14, 15 17, 18	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels. 17Ω typical output impedance.
16	V_{DDO}	Power		Output supply pin.
20	F_SEL1	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance			8		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.3V±5%		17		Ω
		V_{DDO} = 2.5V±5%		21		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{DDD} = V_{DDA} = 3.3V±5%, V_{DDO} = 3.3V±5% OR 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				10	mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				95	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				8	mA

TABLE 3D. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5% OR 2.5V±5%, OR $V_{DD} = V_{DDA}$ = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE, F_SEL0, F_SEL1	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
		nPLL_SEL, MR, nXTAL_SEL, REF_CLK	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	OE, F_SEL0, F_SEL1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		nPLL_SEL, MR, nXTAL_SEL, REF_CLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.3V ± 5%	2.6			V
			V_{DDO} = 2.5V ± 5%	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.3V or 2.5V ± 5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, Output Load Test Circuit.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	186.67	212.5	226.66	MHz
		F_SEL[1:0] = 01	140	159.375	170	MHz
		F_SEL[1:0] = 10	93.33	156.25	113.33	MHz
		F_SEL[1:0] = 11	46.67	106.25	56.66	MHz
*t*sk(o)	Output Skew; NOTE 1, 3				60	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	212.5MHz (637kHz - 10MHz)		0.49		ps
		159.375MHz (637kHz - 10MHz)		0.55		ps
		156.25MHz (1.875MHz - 20MHz)		0.56		ps
		106.25MHz (637kHz - 10MHz)		0.79		ps
		53.125MHz (637kHz - 10MHz)		0.65		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	F_SEL[1:0] = 00	41		59	%
		F_SEL[1:0] = 01	43		57	%
		F_SEL[1:0] = 10 or 11	48		52	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	186.67	212.5	226.66	MHz
		F_SEL[1:0] = 01	140	159.375	170	MHz
		F_SEL[1:0] = 10	93.33	156.25	113.33	MHz
		F_SEL[1:0] = 11	46.67	106.25	56.66	MHz
*t*sk(o)	Output Skew; NOTE 1, 3				60	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	212.5MHz (637kHz - 10MHz)		0.46		ps
		159.375MHz (637kHz - 10MHz)		0.54		ps
		156.25MHz (1.875MHz - 20MHz)		0.57		ps
		106.25MHz (637kHz - 10MHz)		0.73		ps
		53.125MHz (637kHz - 10MHz)		0.63		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	F_SEL[1:0] = 00	42		58	%
		F_SEL[1:0] = 01	44		56	%
		F_SEL[1:0] = 10 or 11	48		52	%

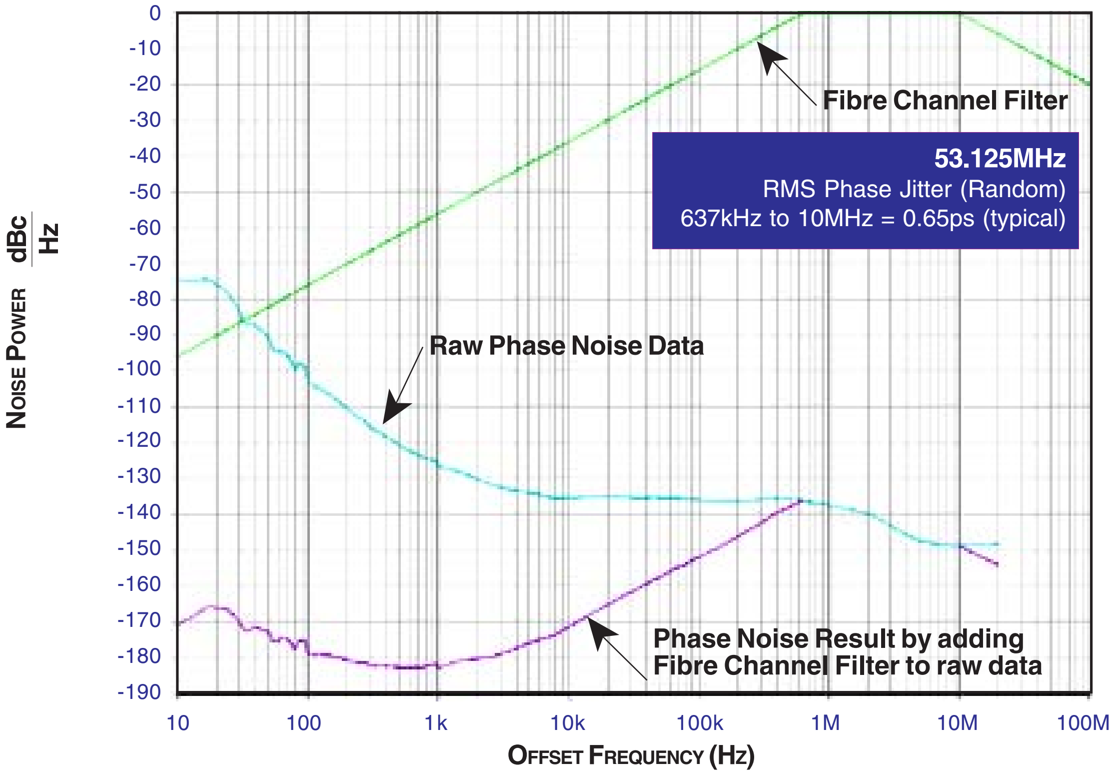
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5\%$, TA = -40°C TO 85°C

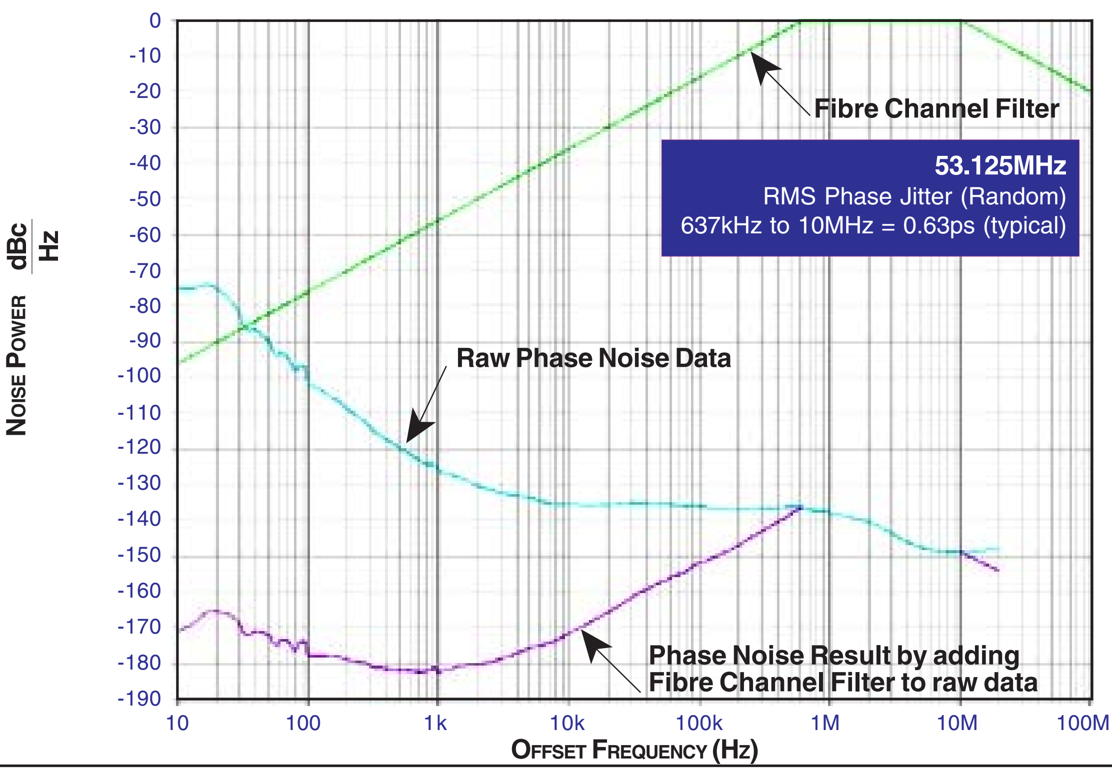
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	186.67	212.5	226.66	MHz
		F_SEL[1:0] = 01	140	159.375	170	MHz
		F_SEL[1:0] = 10	93.33	156.25	113.33	MHz
		F_SEL[1:0] = 11	46.67	106.25	56.66	MHz
*t*sk(o)	Output Skew; NOTE 1, 3				60	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	212.5MHz (637kHz - 10MHz)		0.51		ps
		159.375MHz (637kHz - 10MHz)		0.51		ps
		156.25MHz (1.875MHz - 20MHz)		0.54		ps
		106.25MHz (637kHz - 10MHz)		0.72		ps
		53.125MHz (637kHz - 10MHz)		0.71		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	F_SEL[1:0] = 00	41		59	%
		F_SEL[1:0] = 01	43		57	%
		F_SEL[1:0] = 10 or 11	48		52	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

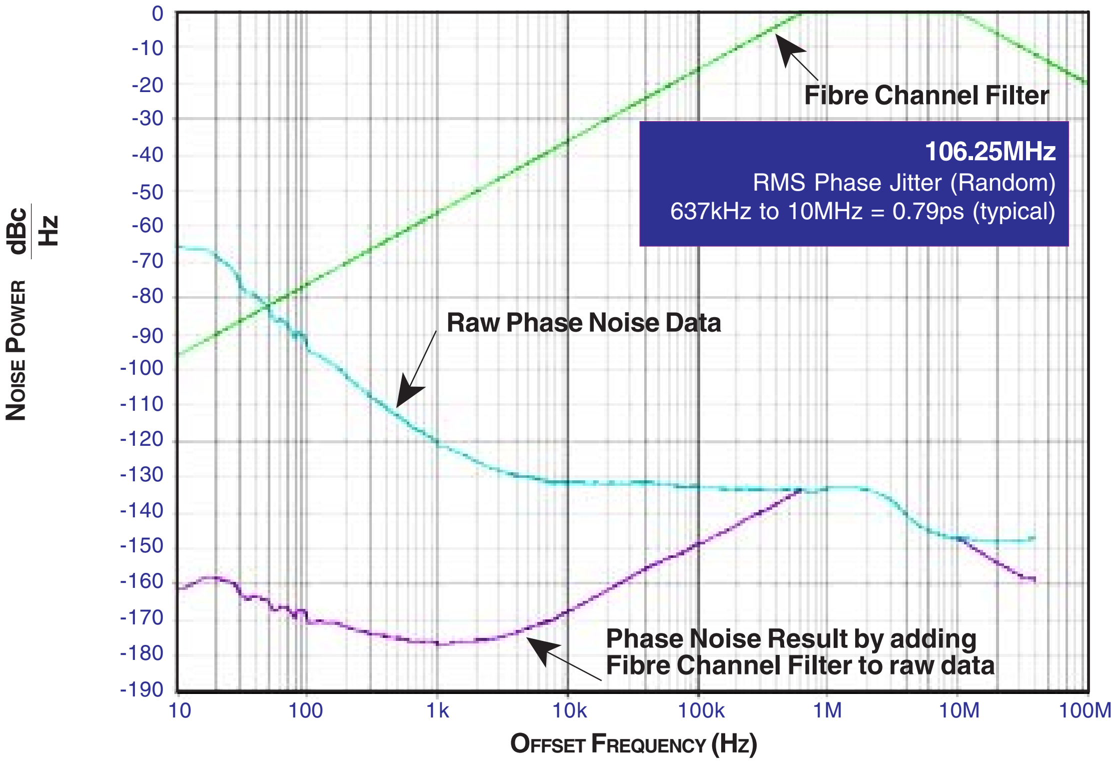
TYPICAL PHASE NOISE AT 53.125MHz @3.3V



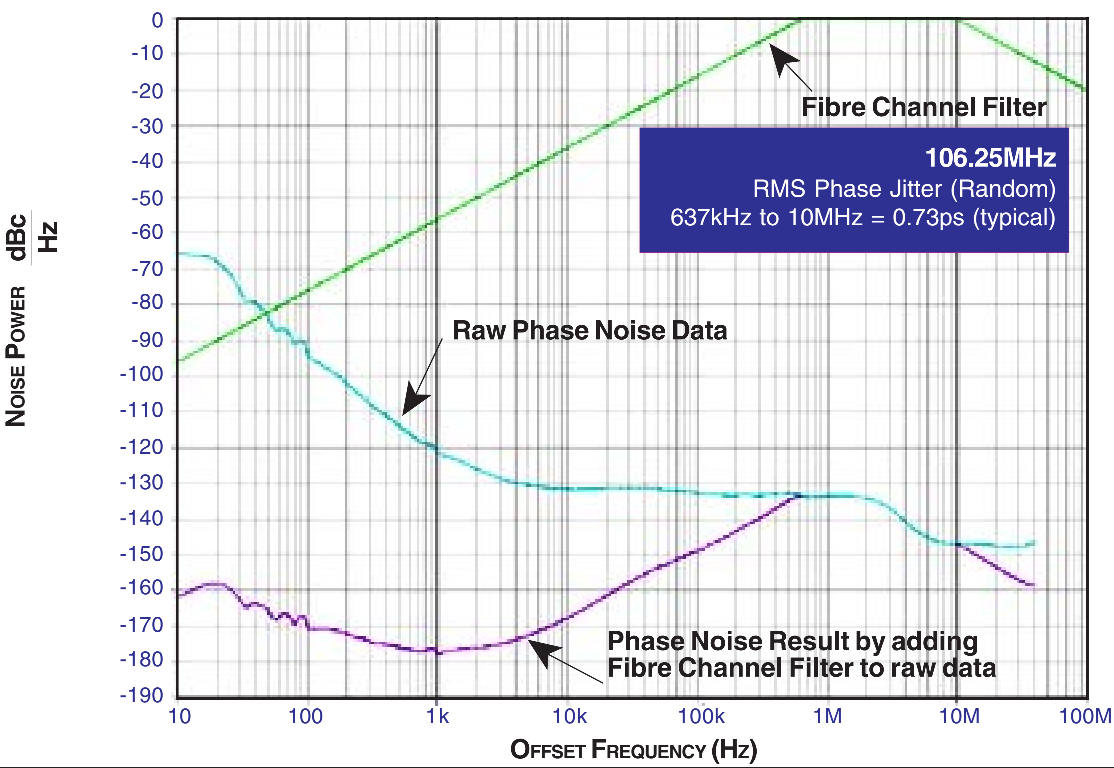
TYPICAL PHASE NOISE AT 53.125MHz @2.5V



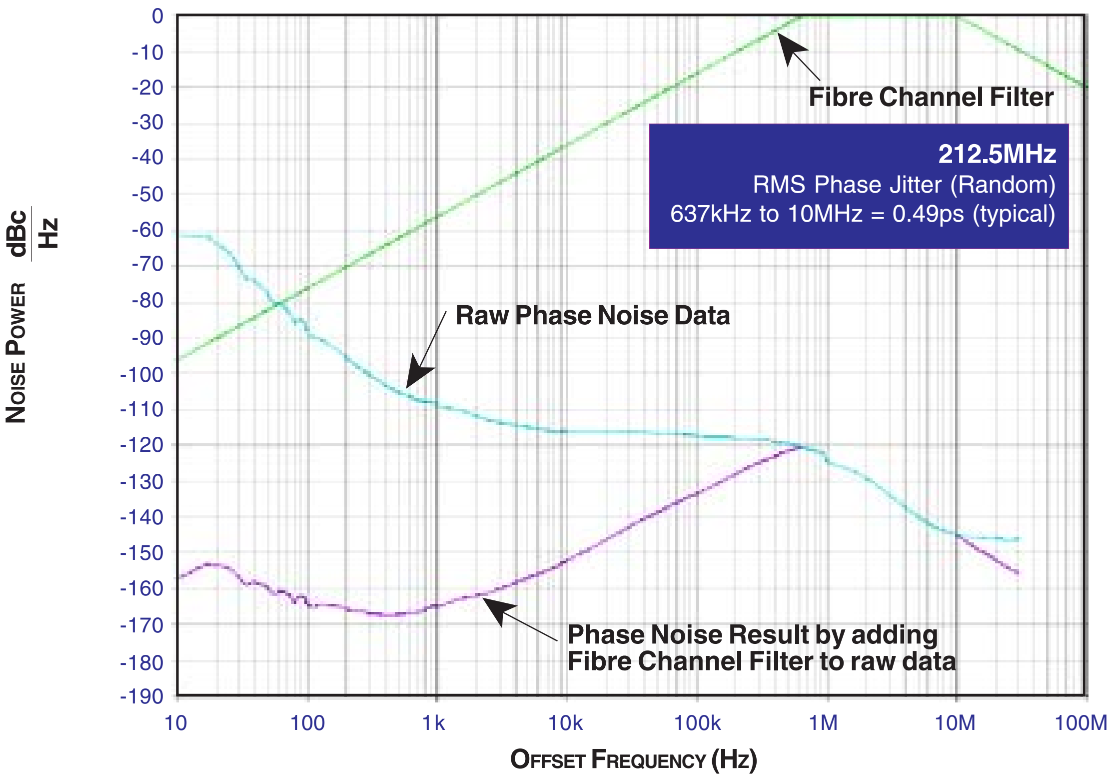
TYPICAL PHASE NOISE AT 106.25MHZ @3.3V



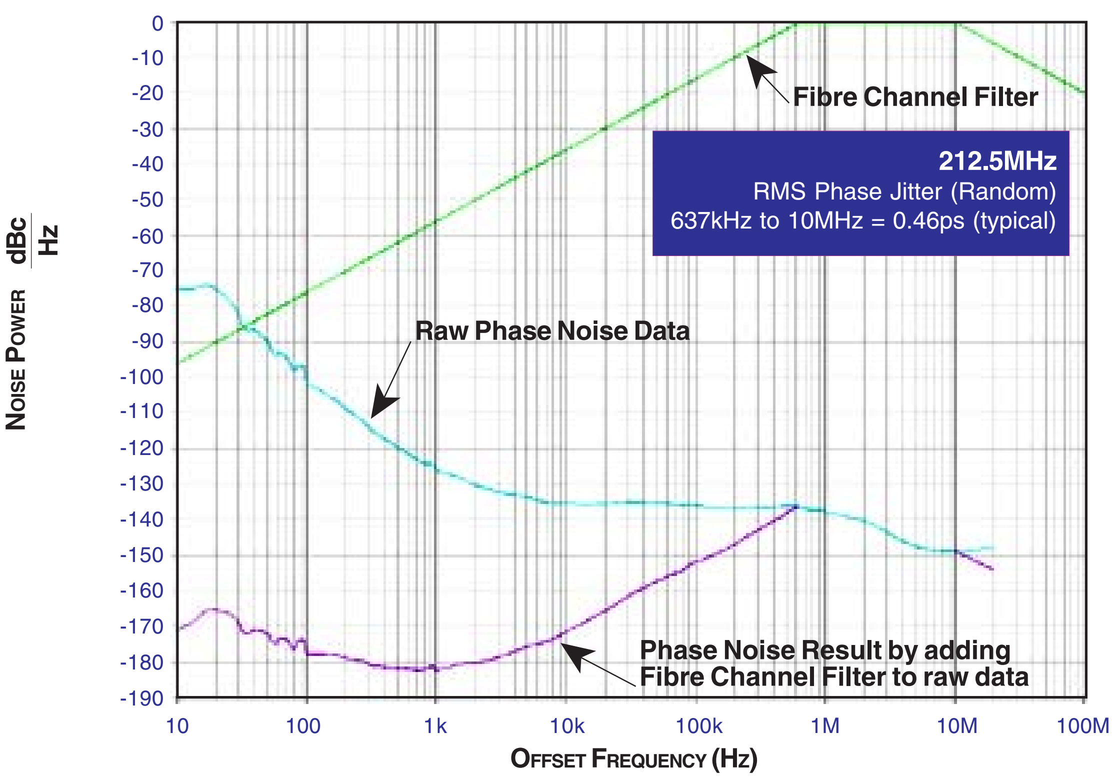
TYPICAL PHASE NOISE AT 106.25MHZ @ 2.5V



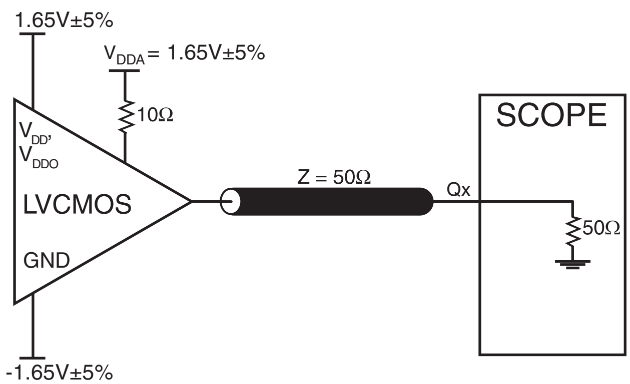
TYPICAL PHASE NOISE AT 212.5MHZ @ 3.3V



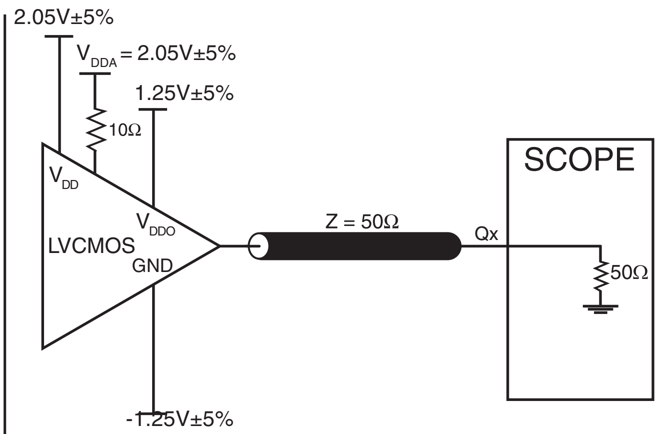
TYPICAL PHASE NOISE AT 212.5MHZ @ 2.5V



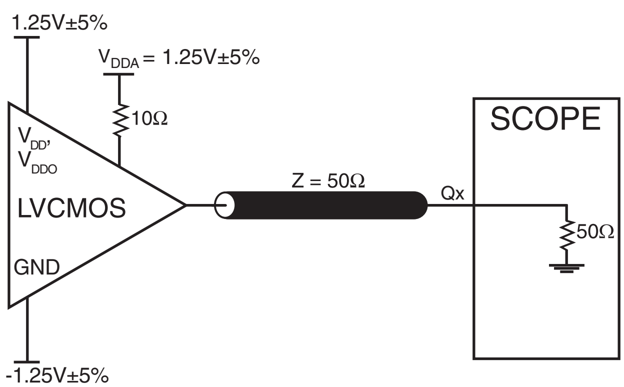
PARAMETER MEASUREMENT INFORMATION



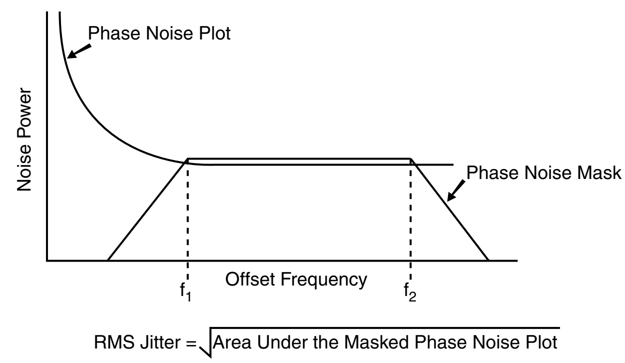
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



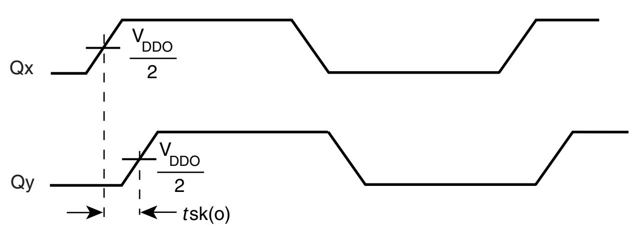
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



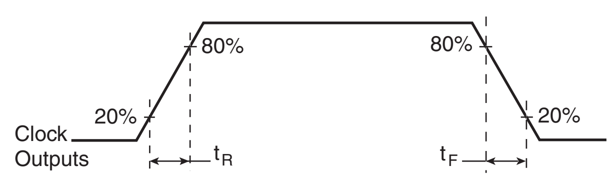
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



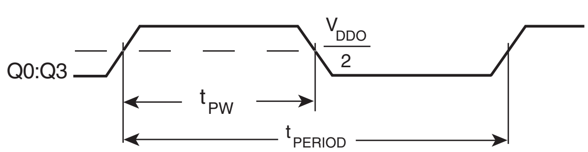
RMS PHASE JITTER



OUTPUT SKEW



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840004I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

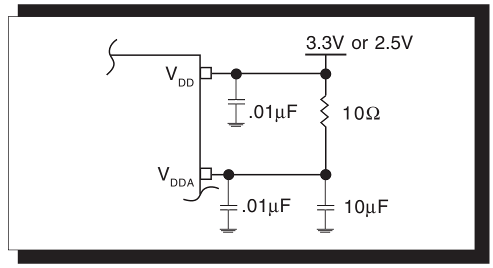


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840004I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

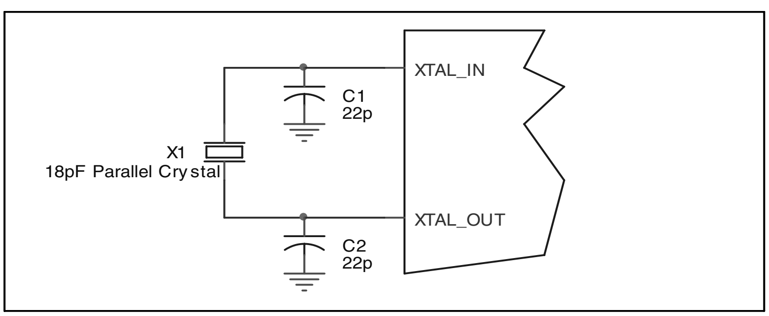


Figure 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

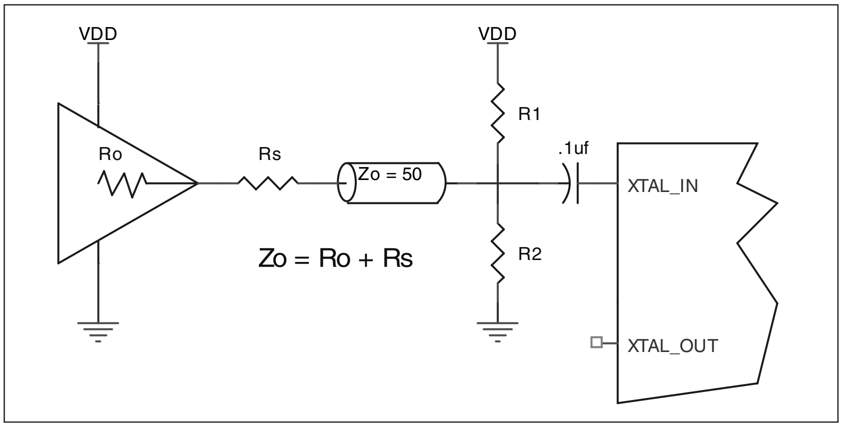


Figure 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT:
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

LAYOUT GUIDELINE

Figure 4 shows a schematic example of the ICS840004I. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18pF parallel resonant 26.5625MHz crystal is used. The C1=22pF and C2=22pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. The 1kΩ pullup or pulldown resistors can be used for the logic control input pins.

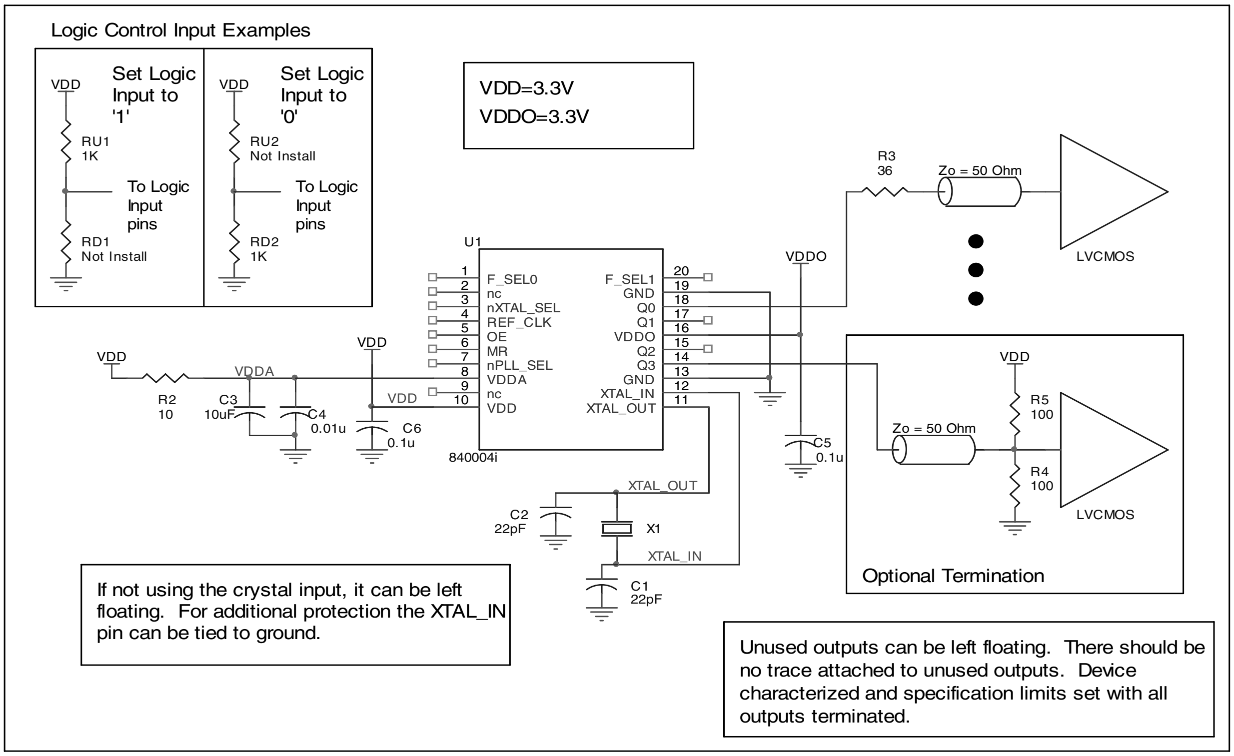


FIGURE 4. ICS840004I SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)

	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS840004I is: 3796

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

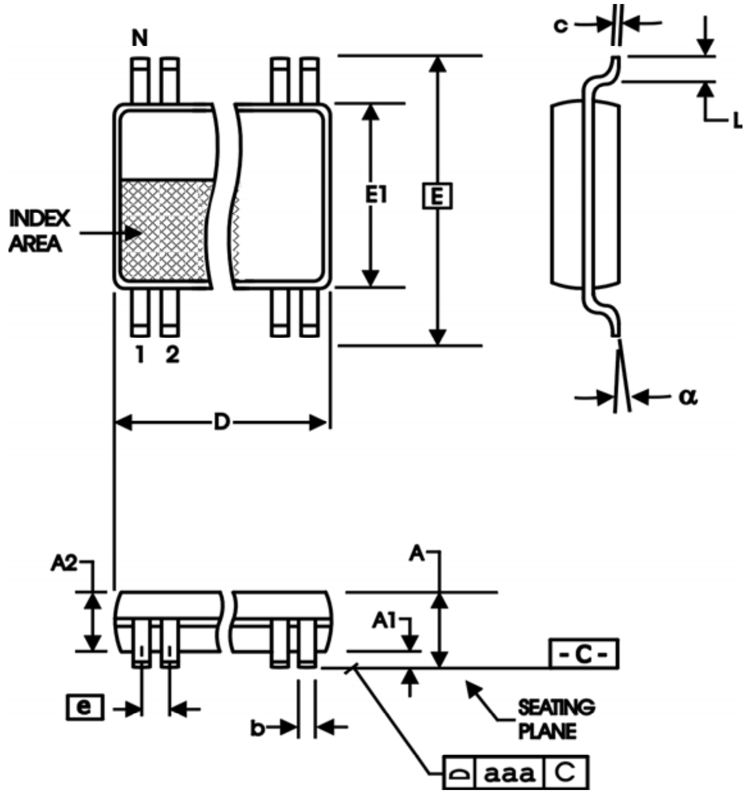


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840004AGI	ICS840004AGI	20 Lead TSSOP	tube	-40°C to 85°C
ICS840004AGIT	ICS840004AGI	20 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS840004AGILF	TBD	20 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS840004AGILFT	TBD	20 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.