

SN74CBTLV16800 LOW-VOLTAGE 20-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS

SCDS045E – DECEMBER 1997 – REVISED NOVEMBER 1998

- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- B-Port Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

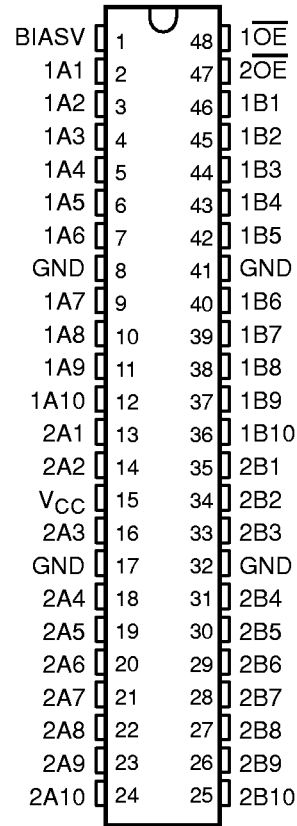
The SN74CBTLV16800 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The device is organized as dual 10-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 10-bit bus switches or one 20-bit bus switch. When \overline{OE} is low, the associated 10-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, a high-impedance state exists between the two ports, and port B is precharged to BIASV through the equivalent of a 10-kΩ resistor.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV16800 is characterized for operation from -40°C to 85°C .

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 10-bit bus switch)

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV



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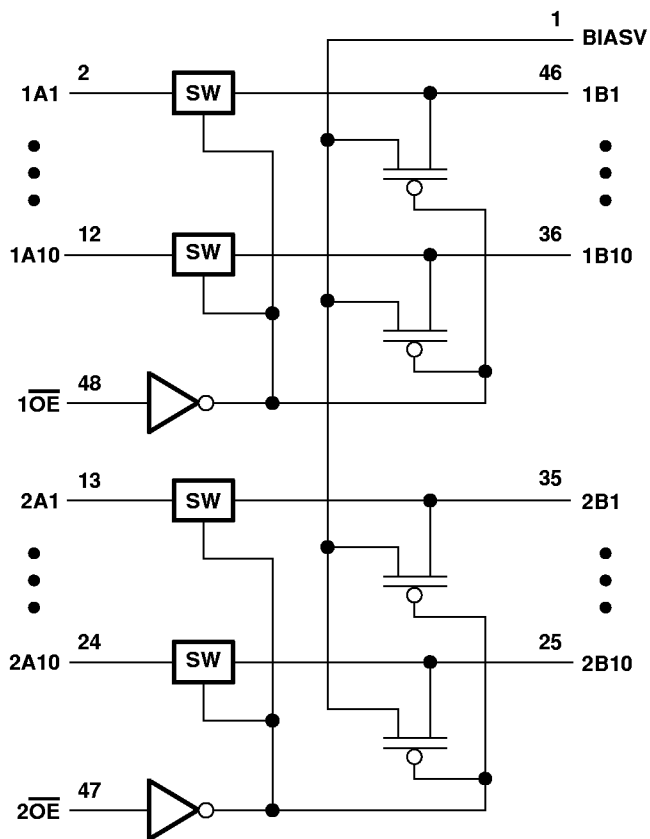
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PRODUCT PREVIEW

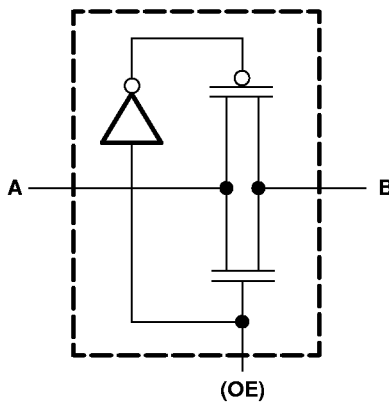
SN74CBTLV16800
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logic diagram (positive logic)



simplified schematic, each FET switch



PRODUCT PREVIEW

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LOW-VOLTAGE 20-BIT FET BUS SWITCH

WITH PRECHARGED OUTPUTS

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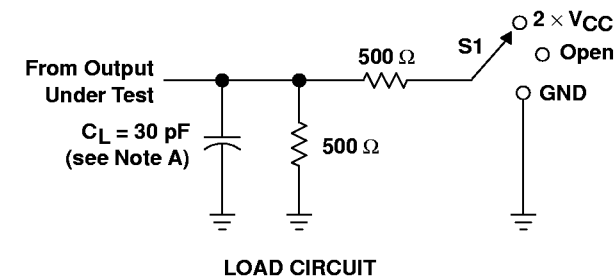
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}^\dagger		A or B	B or A					ns
t_{pZH}	BIASV = GND	\overline{OE}	A or B					ns
t_{pZL}	BIASV = 3 V							
t_{pHZ}	BIASV = GND	\overline{OE}	A or B					ns
t_{pLZ}	BIASV = 3 V							

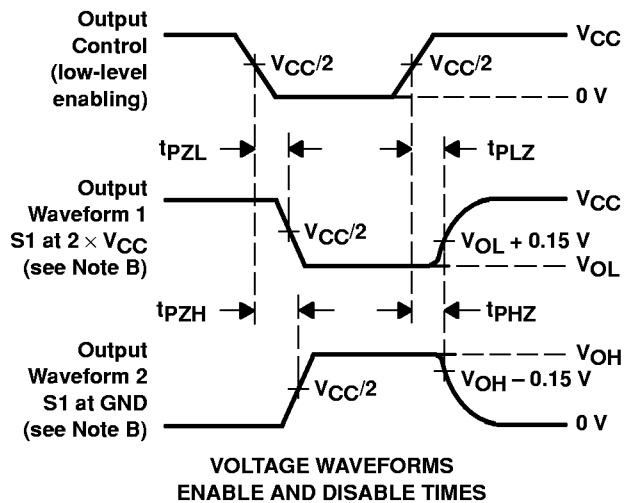
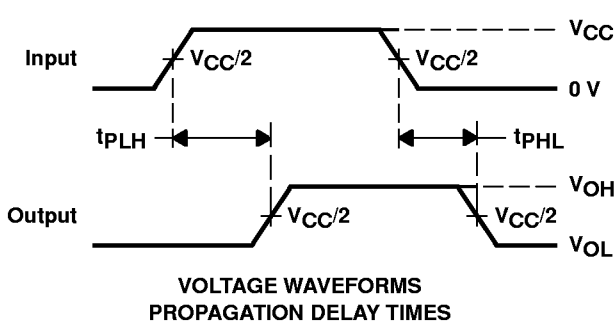
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



TEST	S1
t_{pd}	Open
t_{pLZ}/t_{pZL}	$2 \times V_{CC}$
t_{pHZ}/t_{pZH}	GND



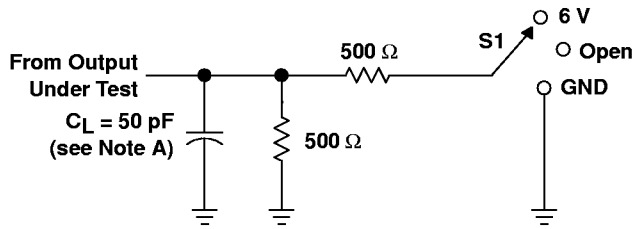
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

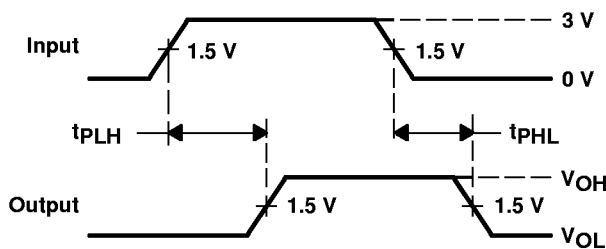
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

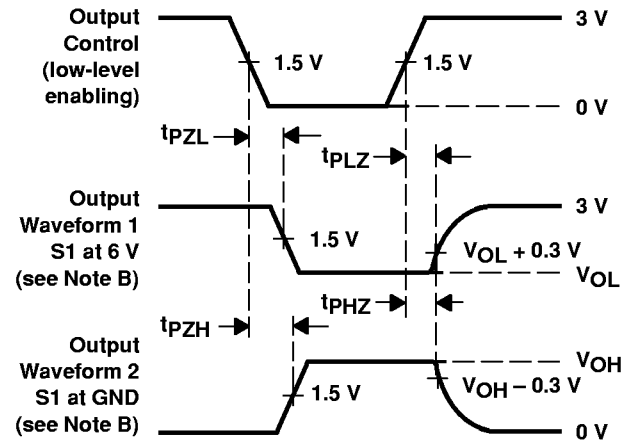


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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