SN74CBTLV16800 LOW-VOLTAGE 20-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS

SCDS045E - DECEMBER 1997 - REVISED NOVEMBER 1998

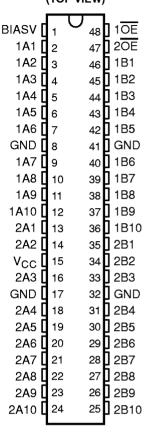
- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- B-Port Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBTLV16800 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The device is organized as dual 10-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 10-bit bus switches or one 20-bit bus switch. When \overline{OE} is low, the associated 10-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, a high-impedance state exists between the two ports, and port B is precharged to BIASV through the equivalent of a 10-k Ω resistor.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV16800 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 10-bit bus switch)

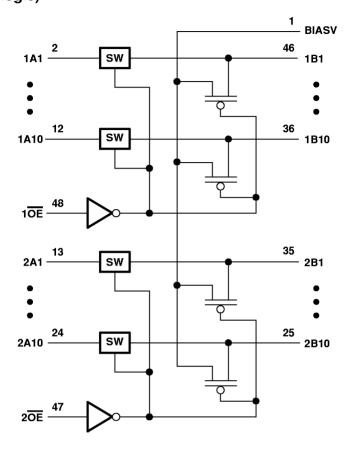
INPUT OE	FUNCTION		
L	A port = B port		
Н	A port = Z B port = BIASV		



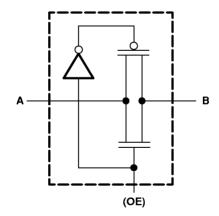
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logic diagram (positive logic)



simplified schematic, each FET switch



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V	' to 4.6 V
Bias voltage range, BIASV		–0.5 V	' to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V	' to 4.6 V
Continuous channel current			128 mA
Input clamp current, I_{IK} ($V_I < 0$)			-50 mA
Package thermal impedance, θ _{JA} (see Note 2)): DGG package		89°C/W
	DGV package		93°C/W
	DL package		94°C/W
Storage temperature range, T _{sto}		. –65°C f	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT	
V _{CC} Supply voltage			2.3	3.6	٧	
BIASV	Bias voltage		0	VCC	V	
V _{IH} F	High-level control input voltage	to 2.7 V	1.7		V	
	V _{CC} = 2.7 V	to 3.6 V	2		'	
V _{IL}	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V		
	Low-level control input voltage $V_{CC} = 2.7 \text{ V}$	to 3.6 V		0.8	'	
TA	Operating free-air temperature		-40	85	°C	

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	PARAMETER TEST CONDITIONS		MIN	TYP‡	MAX	UNIT		
VIK		V _{CC} = 3 V,	I _I = -18 mA				-1.2	V
l _l		$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND				±1	μΑ
loff		$V_{CC} = 0$,	V_{I} or $V_{O}= 0$ to 3.6 V	1			10	μΑ
Ю		V _{CC} = 3 V,	BIASV = 2.4 V,	V _O = 0	0.25			mA
Icc		$V_{CC} = 3.6 \text{ V},$	$I_{O} = 0$,	$V_I = V_{CC}$ or GND			10	μΑ
∆ICC§	Control inputs	$V_{CC} = 3.6 \text{ V},$	One input at 3 V,	Other inputs at $V_{\hbox{CC}}$ or GND			300	μΑ
Ci	Control inputs	V _I = 3 V or 0						pF
C _{o(OFF)}		$V_O = 3 \text{ V or } 0,$	Switch off					pF
r _{on} ¶		$V_{CC} = 2.3 \text{ V},$ TYP at $V_{CC} = 2.5 \text{ V}$	V _I = 0	I _I = 64 mA				Ω
				I _I = 24 mA				
			$V_{I} = 1.7 V$	I _I = 15 mA				
		VCC = 3 V	V _I = 0	I _I = 64 mA				
				I _I = 24 mA				
			V _I = 2.4 V,	I _I = 15 mA				

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51.

[§] This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

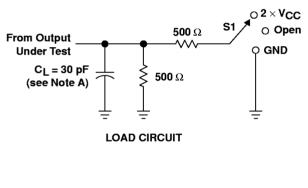
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

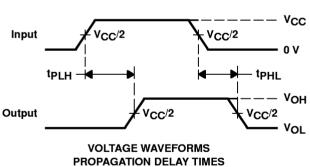
PARAMETER	TEST CONDITIONS	FROM (INPUT)			TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	CONDITIONS		(0011 01)	MIN MAX	MIN MAX			
_{tpd} †		A or B	B or A			ns		
^t PZH	BIASV = GND	ŌĒ	A or B					
^t PZL	BIASV = 3 V		AUID			ns		
^t PHZ	BIASV = GND	ŌĒ	A or B			ns		
^t PLZ	BIASV = 3 V	OE .	AUB			115		

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

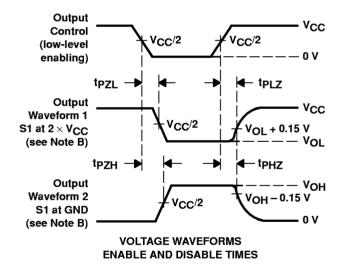
PARAMETER MEASUREMENT INFORMATION

 V_{CC} = 2.5 V \pm 0.2 V





TEST	S1
tpd	Open
tpLZ/tpZL	2×V _{CC}
tPHZ/tPZH	GND



NOTES: A. C_I includes probe and jig capacitance.

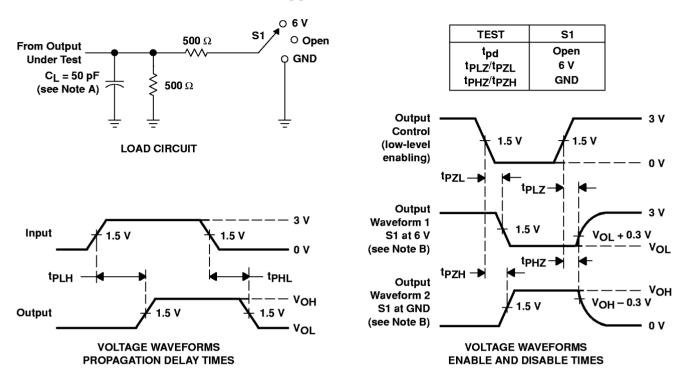
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns,
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

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