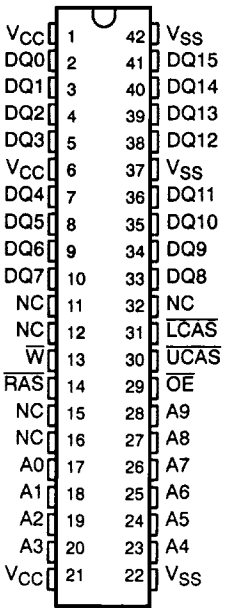
- **Organization . . . 1 048 576 × 16**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

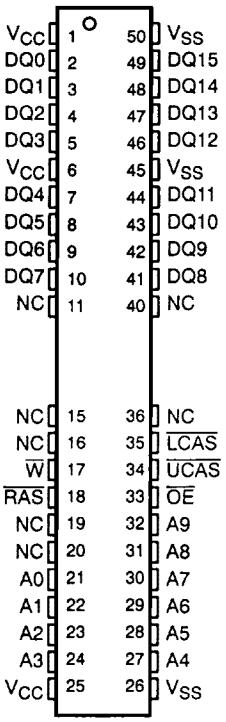
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'418160/P-60	60 ns	15 ns	30 ns	110 ns
'418160/P-70	70 ns	18 ns	35 ns	130 ns
'418160/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  1024-Cycle Refresh in 16 ms (Max)
  128 ms Max for Low-Power, Self-Refresh Version (TMS418160P)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Self-Refresh With Low Power**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **High-Reliability Plastic 42-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 44/50-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

RE PACKAGE† (TOP VIEW)



DC PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only

PIN NOMENCLATURE	
A0–A9	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{LCAS}$	Lower Column-Address Strobe
$\overline{UCAS}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS418160 series are high-speed, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

The TMS418160P series are high-speed, low-power, self-refresh, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power dissipation is as low as 11 mW standby on 80 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

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PRODUCT PREVIEW

The TMS418160 and TMS418160P are each offered in a 42-lead plastic surface mount SOJ (RE suffix) package, and a 44/50-lead plastic surface mount TSOP (DC suffix). These packages are characterized for operation from 0°C to 70°C.

operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$–$\overline{UCAS}$) are provided to give independent control of the sixteen data I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ pin going low enables its corresponding DQ pin with data coming from the column address to be latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge.The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{CAS}$ to its corresponding DQx pin.

In order to latch in a new column address, all $\overline{xCAS}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first falling $\overline{xCAS}$ edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early write cycles, the data is latched on the first falling $\overline{xCAS}$ edge. Only the DQs that have the corresponding $\overline{xCAS}$ low will be written into. Each $\overline{xCAS}$ will have to meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, all $\overline{xCAS}$ pins need to come high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts, because data retrieval begins as soon as column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{xCAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

address (A0–A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on pins A0 through A9 and latched onto the chip by $\overline{RAS}$. Then, ten column–address bits are set up on pins A0 through A9 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

PRODUCT PREVIEW

write enable ($\overline{W}$)

The read or write mode is selected through the $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output buffers to go into low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every sixteen milliseconds (128 ms for TMS418160P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding all $\overline{xCAS}$ at the high (inactive) level, thus conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{xCAS}$-before-$\overline{RAS}$ refresh

$\overline{xCAS}$-before-$\overline{RAS}$ refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{xCAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

A low-power battery-backup refresh mode that requires less than 500 μA refresh current is available on the TMS418160P. Data integrity is maintained using $\overline{xCAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

PRODUCT PREVIEW

self refresh (TMS418160P)

The self-refresh mode is entered by dropping $\overline{\text{xCAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{xCAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode both $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{\text{RAS}}$ cycles is required after power-up to the full V_{CC} level.

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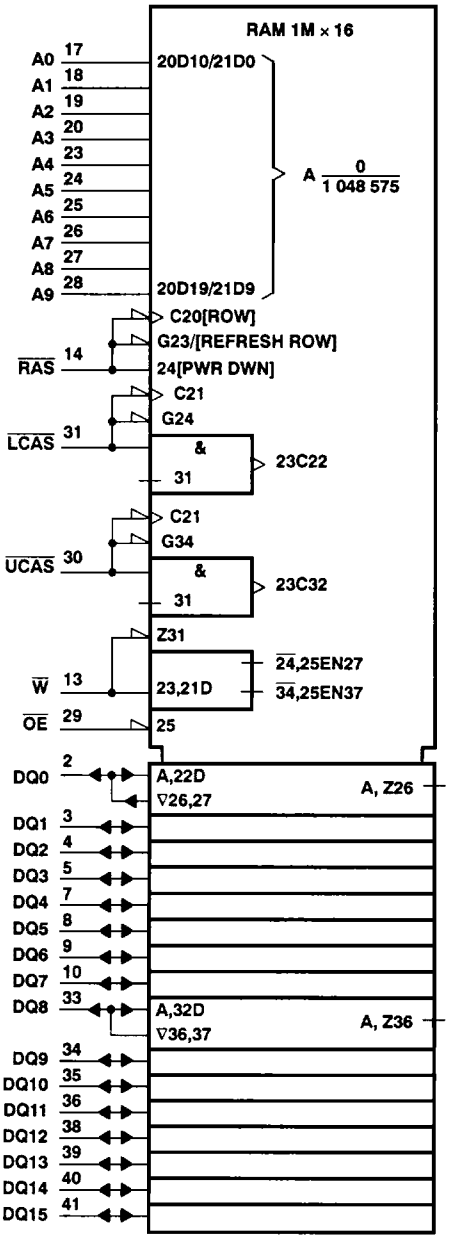
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the RE package.

PRODUCT PREVIEW

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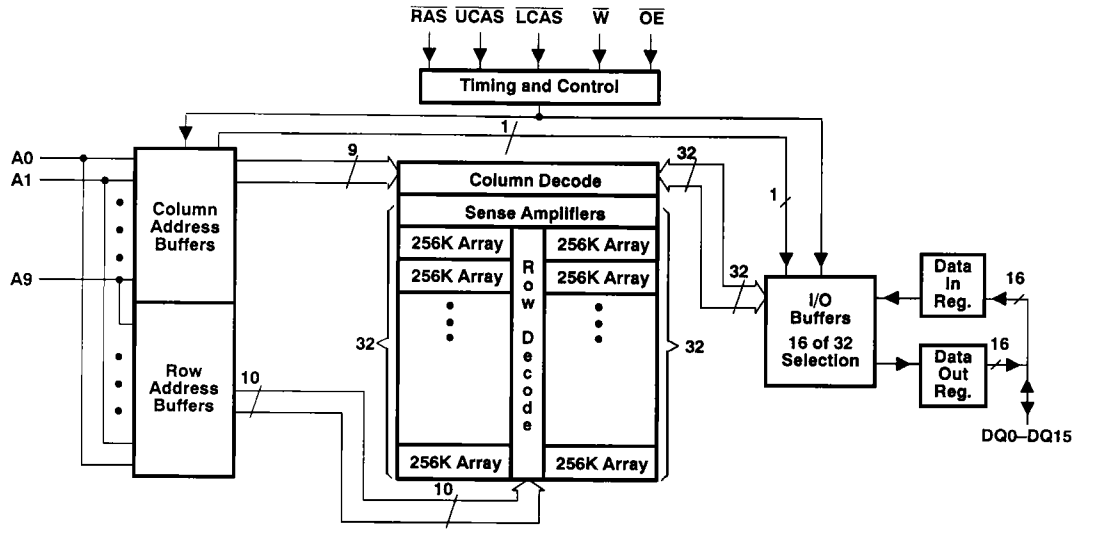
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... –1 V to 7 V
Supply voltage range on V_{CC} ..... –1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†‡	Read or write cycle current	V_{CC} = 5.5 V, Minimum cycle			TBD		TBD		TBD	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'418160		1		1		1	mA
			'418160P		500		500		500	µA
I_{CC3}‡	Average refresh current ($\overline{RAS}$-only or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			TBD		TBD		TBD	mA
I_{CC4}†§	Average page current	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			TBD		TBD		TBD	mA
I_{CC6}¶	Self refresh	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			500		500		500	µA
I_{CC7}†	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{xCAS}$ = V_{IL}, Data out = enabled			5		5		5	mA
I_{CC10}¶	Battery back-up operating current (equivalent refresh time is 128 ms). CBR only.	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			500		500		500	µA

† Measured with outputs open.
‡ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
§ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}.
¶ For TMS418160P only.

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{xCAS}$ low		15		18		20	ns
t_{AA}	Access time from column address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low Z	0		0		0		ns
t_{OH}	Output data hold time (from $\overline{xCAS}$)	3		3		3		ns
t_{OHO}	Output data hold time (from $\overline{OE}$)	3		3		3		ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 4)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	0	15	0	18	0	20	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	110		130		150		ns
t_{WC}	Write cycle time	110		130		150		ns
t_{RWC}	Read-write/read-modify-write cycle time	155		181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	40		45		50		ns
t_{PRWC}	Page-mode read-modify-write cycle time	85		96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{xCAS}$ high (precharge)	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low (see Note 10)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{xCAS}$ high	15		18		20		ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
8. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
9. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{xCAS}$ low time (t_{CAS}).
10. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 5)

		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $x\overline{CAS}$ low (see Note 12)	0		0		0		ns
t_{CAH}	Column-address hold time after $x\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time after $x\overline{CAS}$ low (see Note 10)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $x\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		ns
t_{WCH}	Write hold time after $x\overline{CAS}$ low (see Note 12)	15		15		15		ns
t_{CLCH}	Hold time, $x\overline{CAS}$ low to $x\overline{CAS}$ high	5		5		5		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 14)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $x\overline{CAS}$ high (see Note 11)	20		20		20		ns
t_{CRP}	Delay time, $x\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $x\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $x\overline{CAS}$ low to $\overline{RAS}$ low (see Note 11)	10		10		10		ns
t_{CWD}	Delay time, $x\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	40		46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	15		18		20		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $x\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $x\overline{CAS}$ low (see Note 15)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $x\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $x\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ from $x\overline{CAS}$ precharge	60		68		75		ns
t_{CPRH}	$\overline{RAS}$ hold time from $x\overline{CAS}$ precharge	35		40		45		ns
t_{CPR}	$x\overline{CAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	110		130		150		ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
10. Reference to the first $x\overline{CAS}$ or $\overline{W}$, whichever occurs last.
11. $x\overline{CAS}$-before-$\overline{RAS}$ refresh only.
12. Early write operation only.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. Read-modify-write operation only.
15. Maximum value specified only to assure access time.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded) (see Note 5)

		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{CHS}	$\overline{xCAS}$ low hold time after $\overline{RAS}$ high (self refresh)	– 50		– 50		– 50		ns
t_{REF}	Refresh time interval (TMS418160 only)		16		16		16	ms
t_{REF}	Refresh time interval, low power (TMS418160P only)		128		128		128	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.

PARAMETER MEASUREMENT INFORMATION

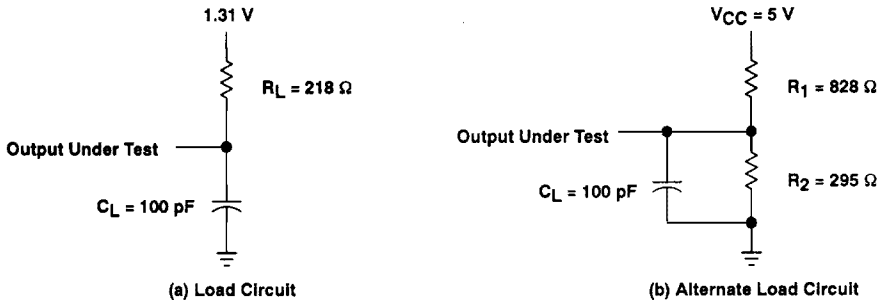
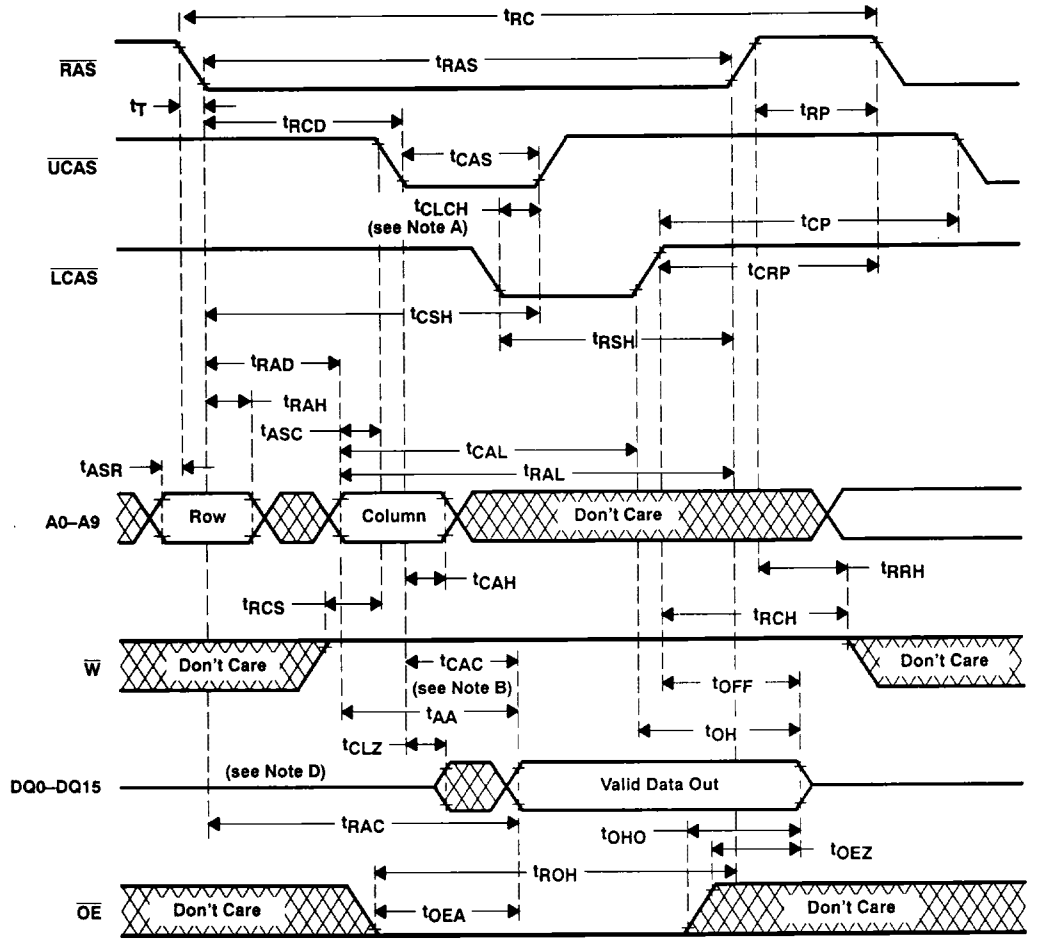


Figure 1. Load Circuits for Timing Parameters

PRODUCT PREVIEW

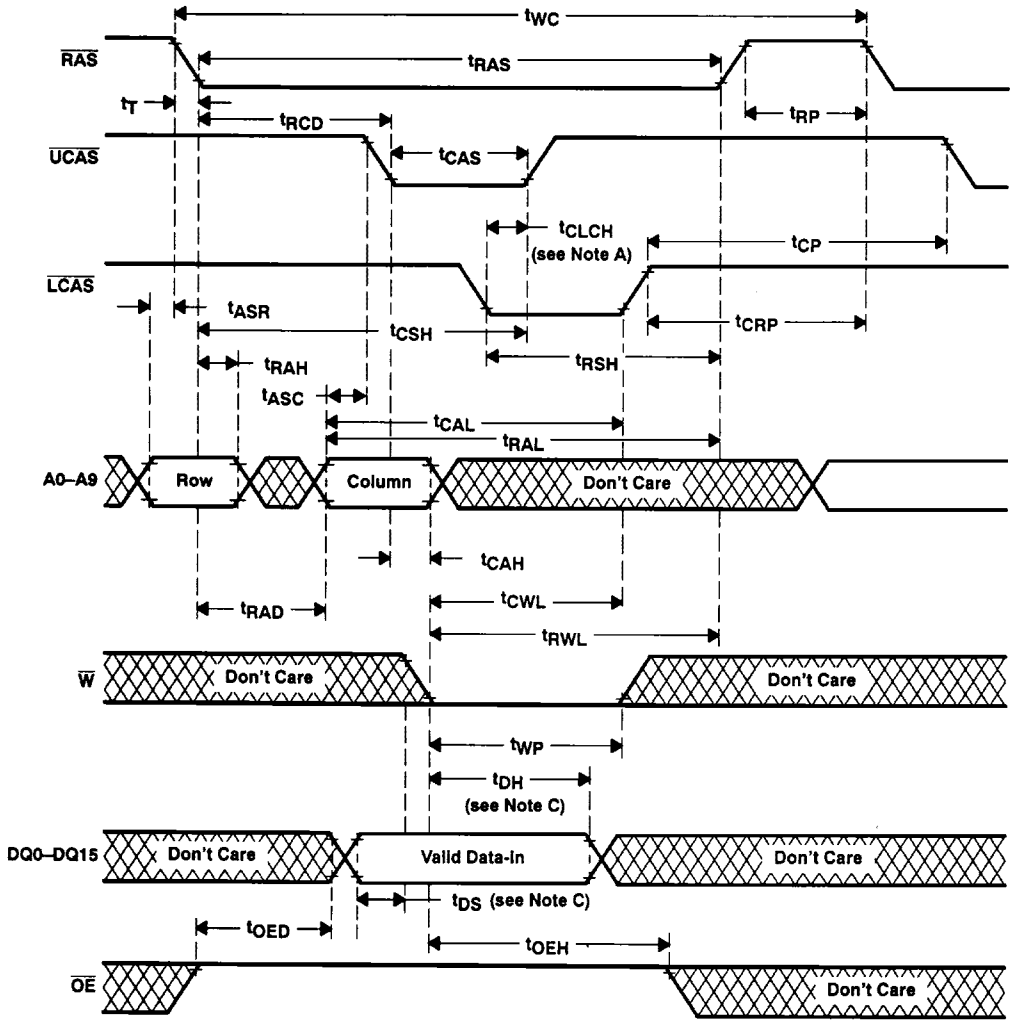
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

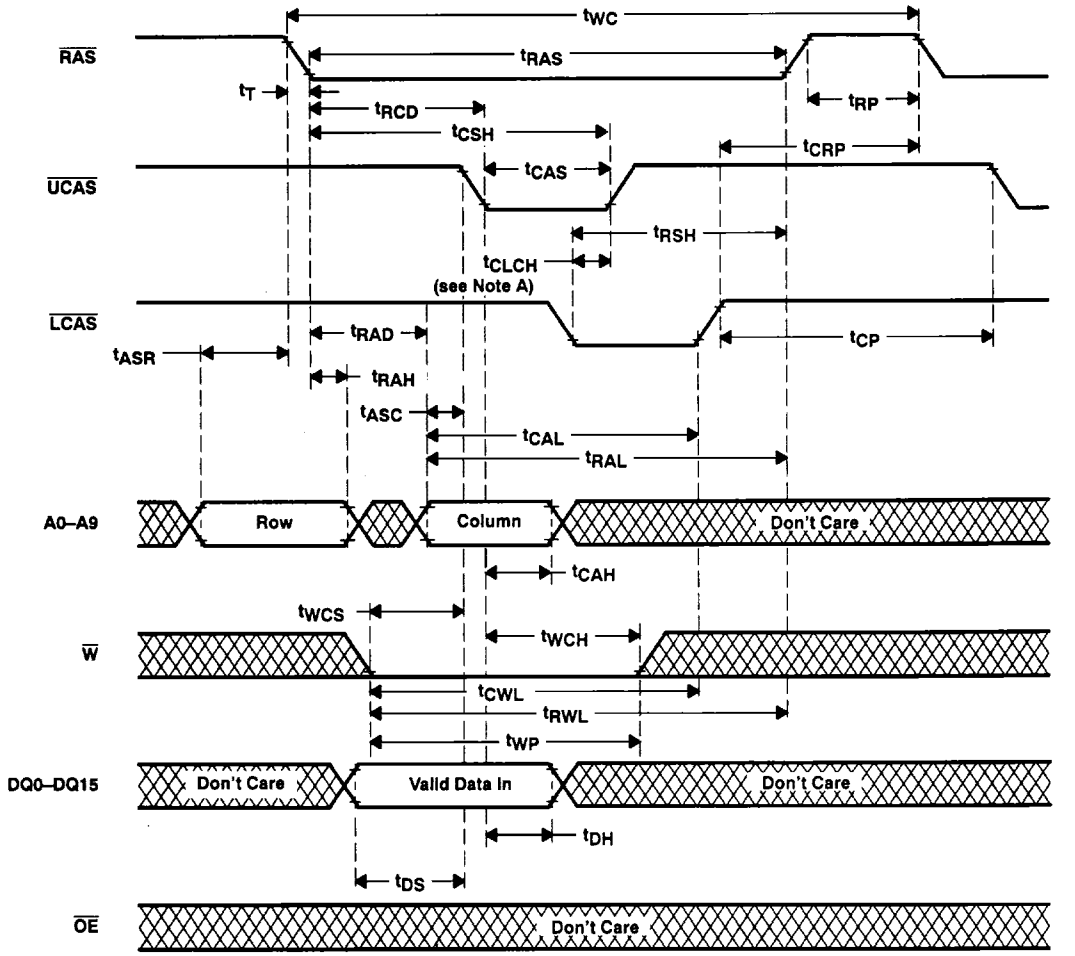


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

Figure 3. Write Cycle Timing

PRODUCT PREVIEW

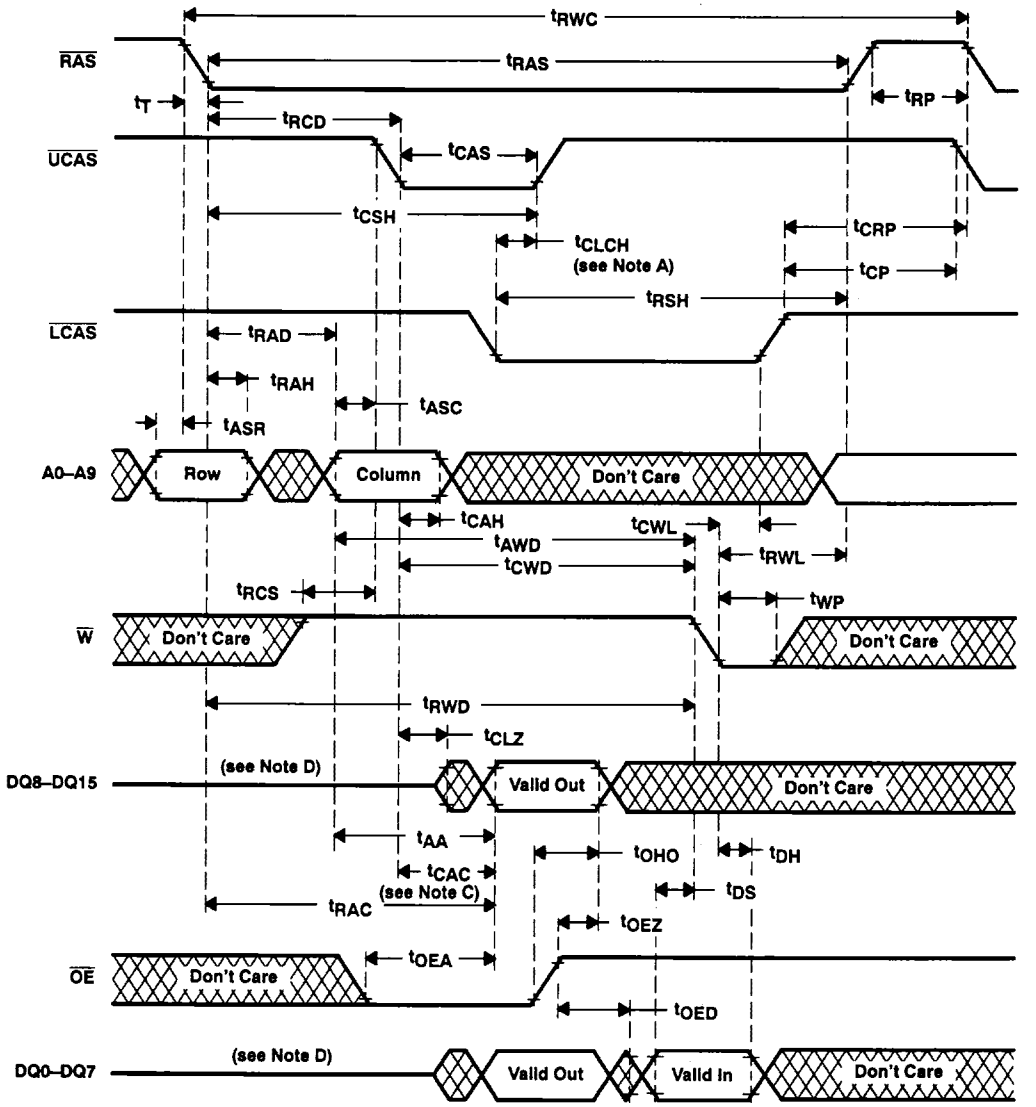
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.

Figure 4. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

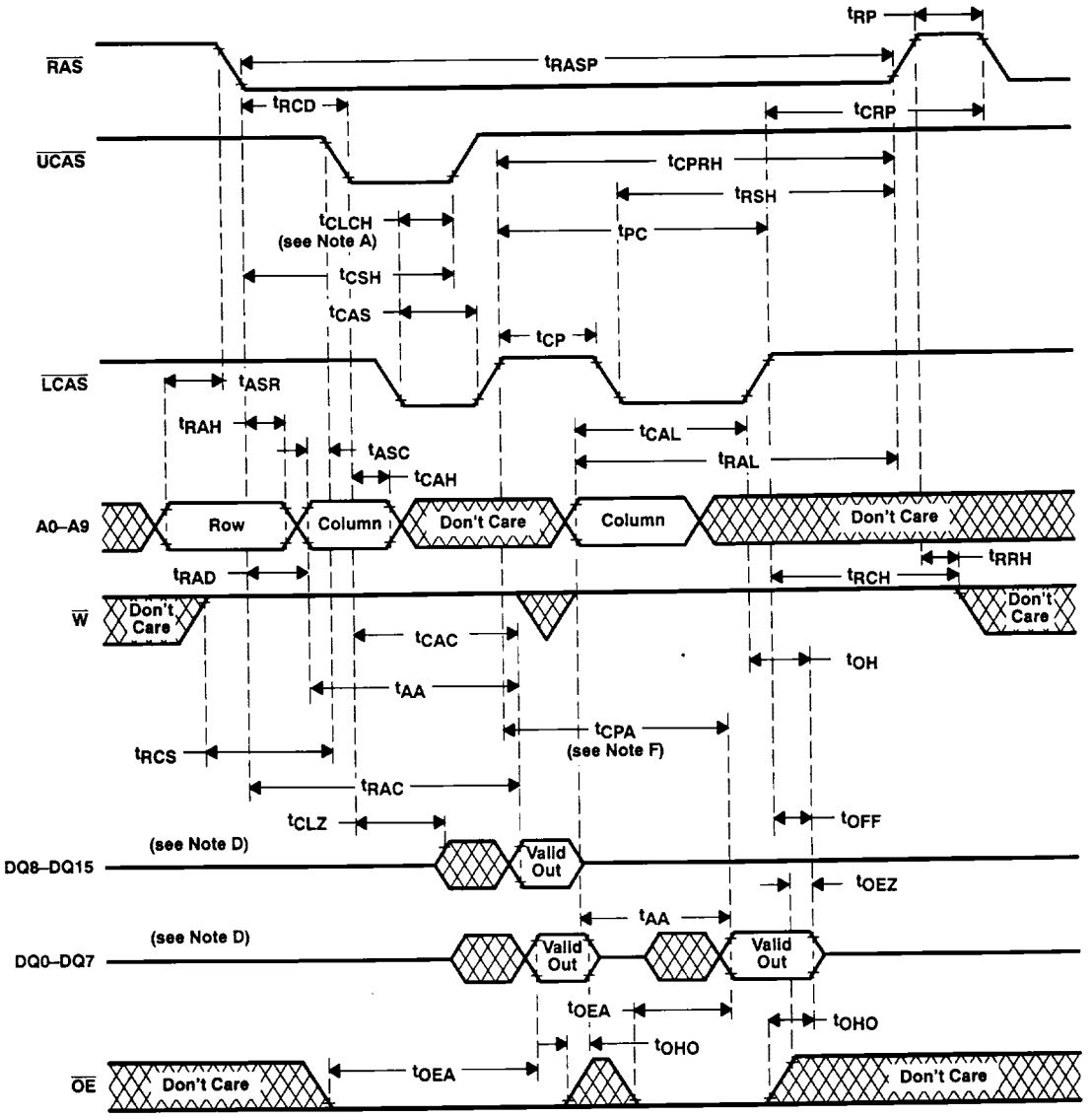


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. t_{CAC} in measured from $\overline{xCAS}$ to its corresponding DQx.
D. Output might go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

PRODUCT PREVIEW

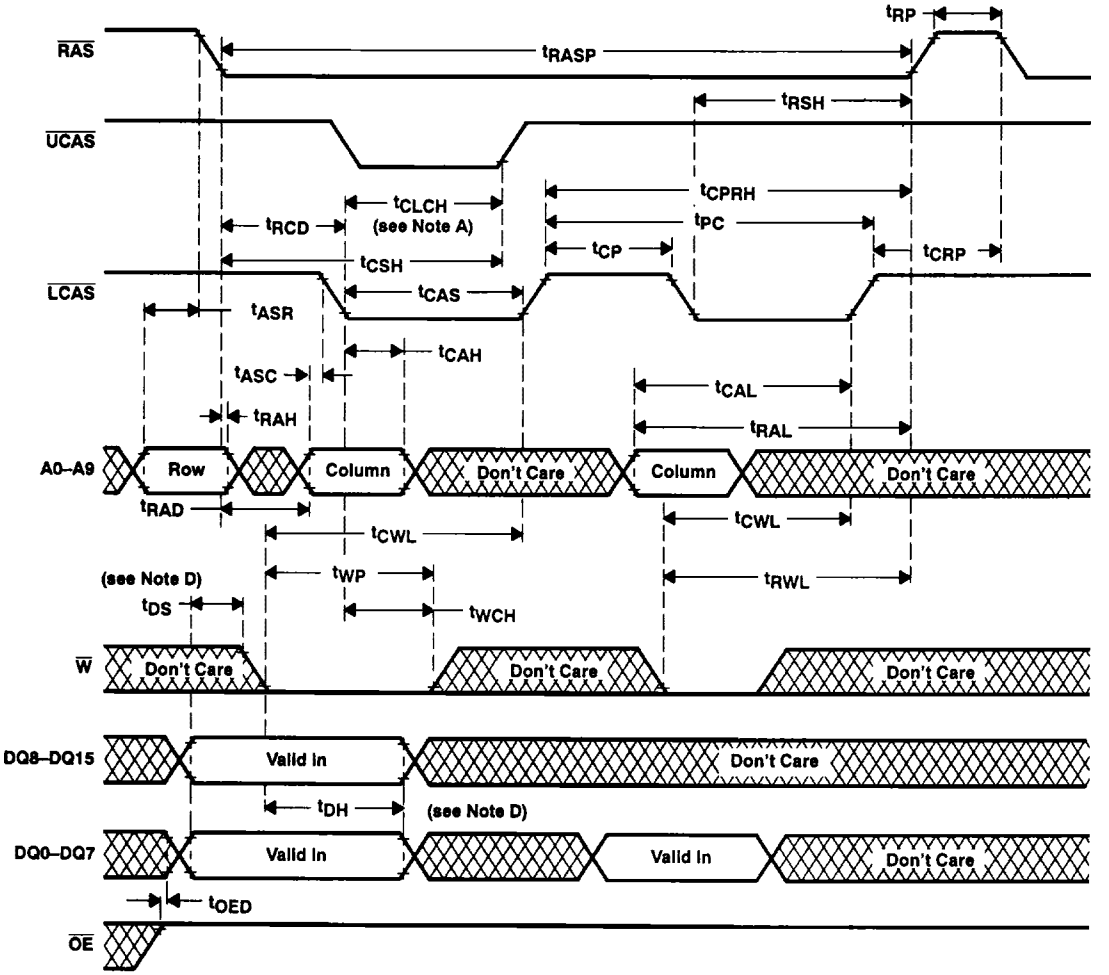
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

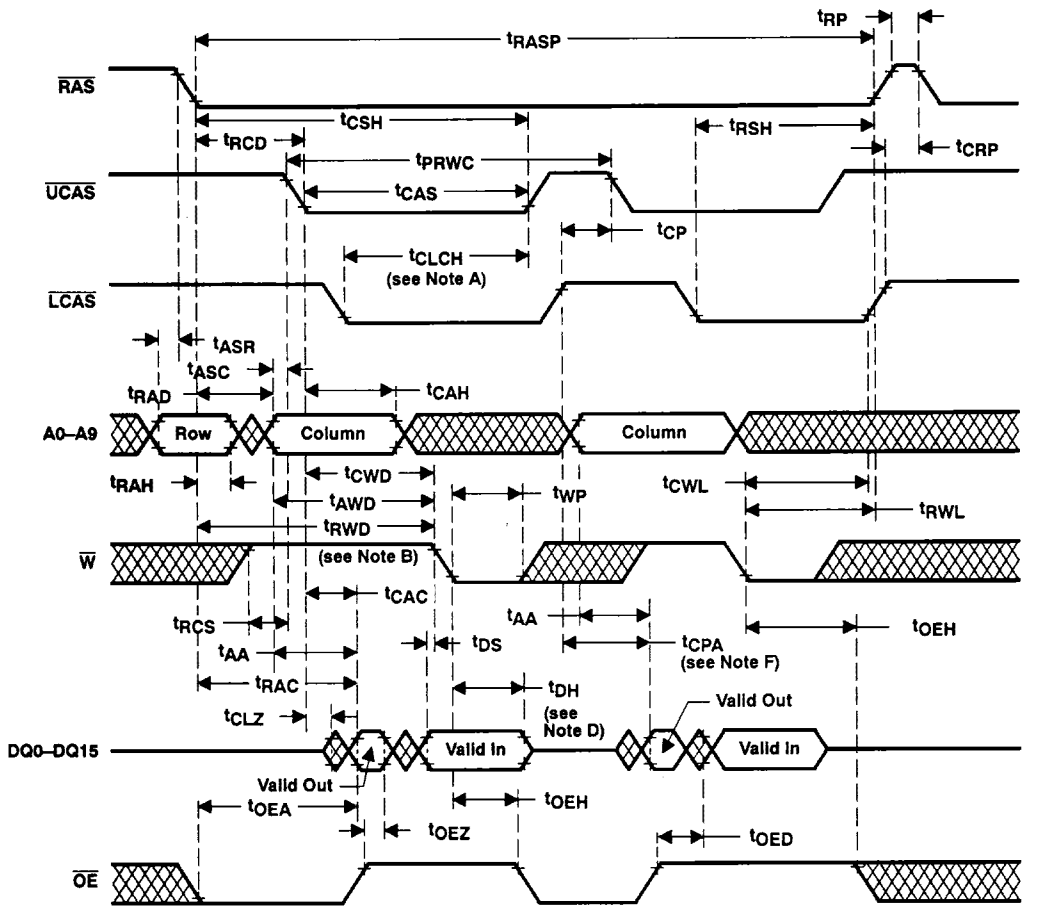


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
D. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PRODUCT PREVIEW

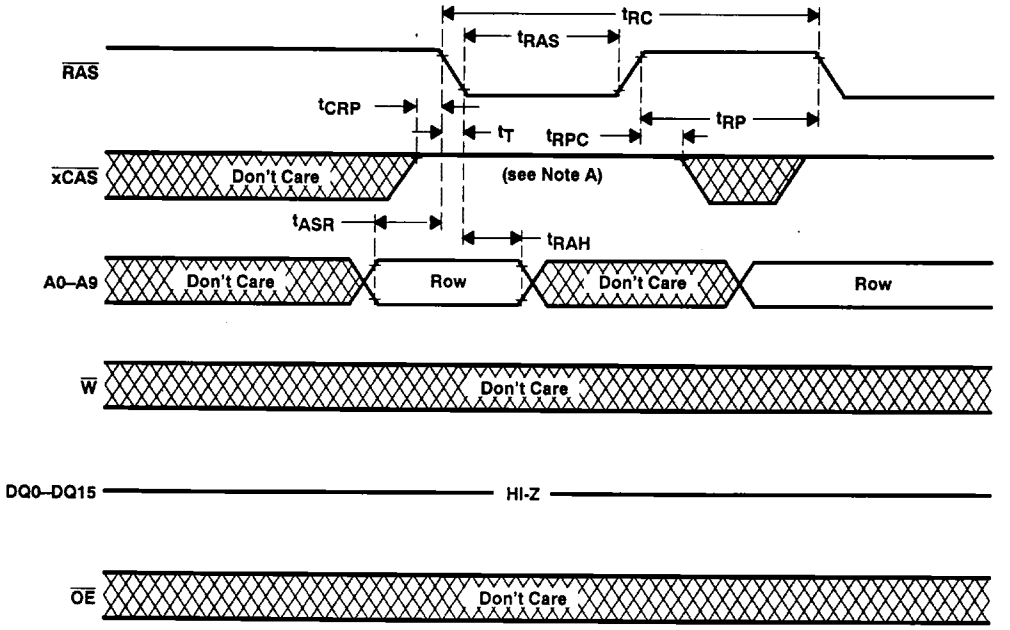
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: All $\overline{xCAS}$ must be high.

Figure 9. $\overline{RAS}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

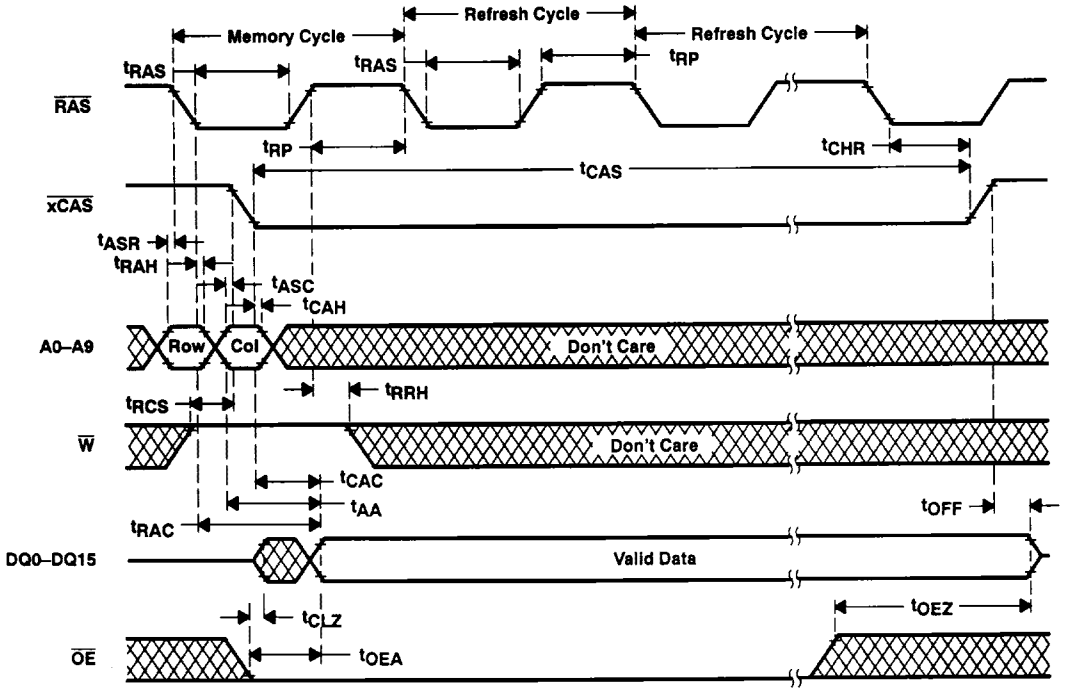

Figure 10. Hidden Refresh Cycle Timing

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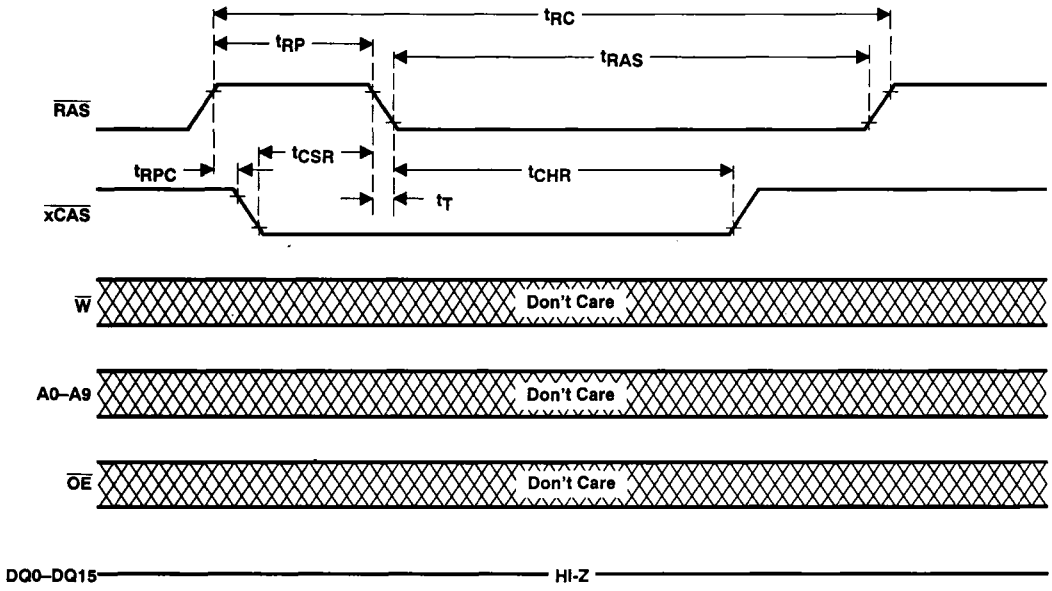
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Any $\overline{xCAS}$ may be used.

Figure 11. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

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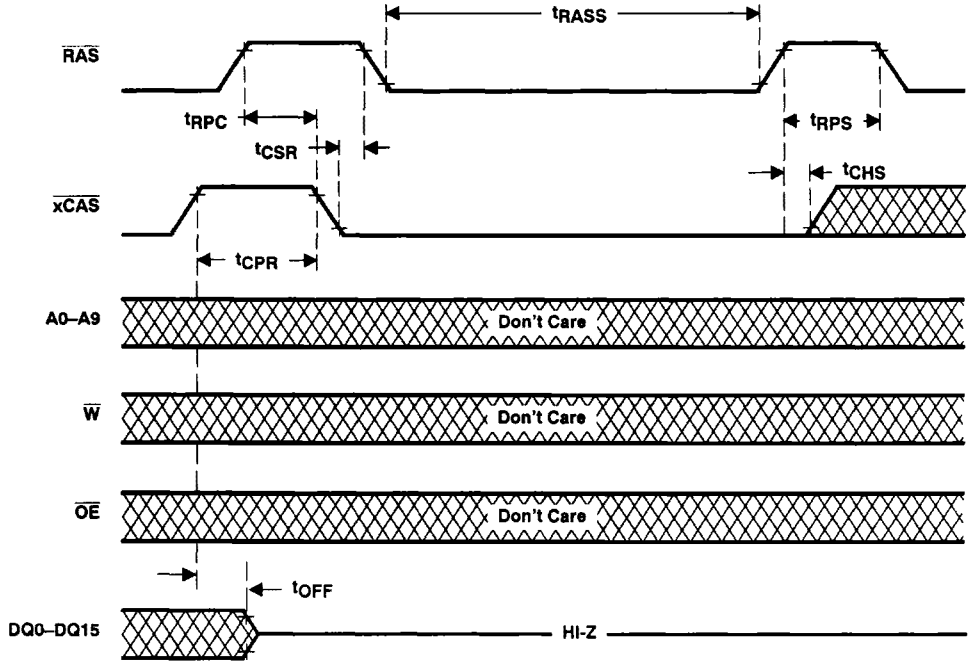
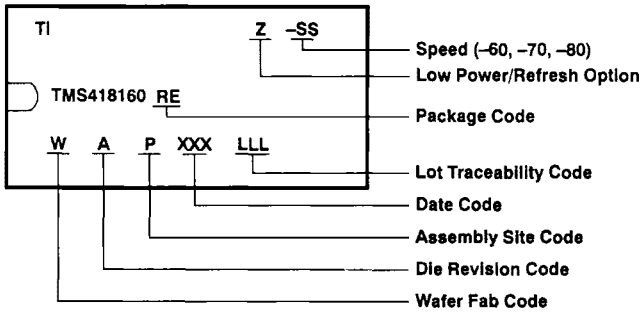


Figure 12. Self Refresh Timing

device symbolization



PRODUCT PREVIEW

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