DG200A

Dual Monolithic SPST CMOS Analog Switch

Siliconix incorporated

T-51-11

FEATURES

- ±15 V Input Signal Range
- 44 Volt Maximum Supply Ratings
- ON Resistance < 70 Ω
- TTL and CMOS Compatability
- Static Protected Logic Inputs

BENEFITS

- Wide Dynamic Capabilities
- Higher Power Supply Tolerance
- Simple Interfacing
- Reduced External Component Count

APPLICATIONS

- Servo Control Switching
- Programmable Gain Amplifiers
- Integration Reset Switching

DESCRIPTION

The DG200A is a dual, single-pole, single-throw analog switch designed to provide general purpose switching of analog signals. This device is ideally suited for designs requiring a wide analog voltage range coupled with low ON resistance.

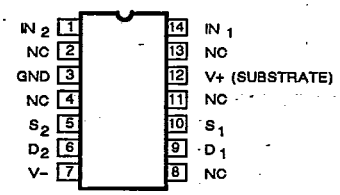
The DG200A is designed on Siliconix' PLUS-40 CMOS process to achieve a high voltage rating and superior switch performance. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. In the ON condition, this bi-directional switch introduces no offset voltage of its own.

Packaging for the DG200A include a 14-pin CerDIP, metal can, and plastic DIP options. Performance grades include military, A suffix (–55 to 125°C), industrial, B suffix (–25 to 85°C), and commercial, C suffix (0 to 70°C) temperature ranges.

PIN CONFIGURATION

Dual-In-Line Package



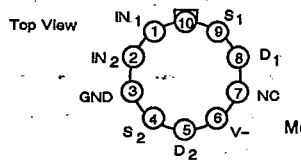
Top View

Order Numbers:

CerDIP: DG200AAK, DG200AAK/883
DG200ABK, DG200ACK

Plastic: DG200ACJ

V+ (SUBSTRATE AND CASE)

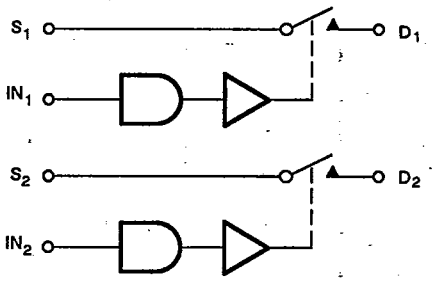


Metal Can Package

Order Numbers:

DG200AAA, DG200AAA/883
DG200ABA, DG200ACA

FUNCTIONAL BLOCK DIAGRAM



Two SPST Switches per Package*

TRUTH TABLE

LOGIC	SWITCH
0	ON
1	OFF

LOGIC "0" ≤ 0.8 V
LOGIC "1" ≥ 2.4 V

* Switches Shown for Logic "1" Input

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ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V

GND to V- ..... 25 V

Digital Inputs[1], V_S, V_D ..... (V-) -2 V to (V+) +2 V or ..... 30 mA, whichever occure first

Current (Any Terminal) Continuous ..... 30 mA

Current S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 100 mA

Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
(C Suffix) ..... 0 to 70°C

Storage Temperature (A & B Suffix) ..... -65 to 150°C
(C Suffix) ..... -65 to 125°C

Power Dissipation (Package)*
Metal Can** ..... 450 mW
14-Pin Ceramic DIP*** ..... 825 mW
14-Pin Plastic DIP**** ..... 470 mW

* All leads soldered or welded to PC board.
** Derate 6 mW/°C above 75°C.
*** Derate 11 mW/°C above 75°C.
**** Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = +15 V, V- = -15 V, GND = 0 V		LIMITS 1=25°C 2=125,85,70°C 3=-55,-25,0°C		A SUFFIX -55 to 125°C		B,C SUFFIX		UNIT
				TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
SUPPLY										
Analog Signal Range [c]	V_{ANALOG}			1,2,3		-15	15	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V_D = ±10 V, V_{IN} = 0.8 V, I_S = -1 mA		1,3 2	45		70 100		80 100	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2.4 V	V_S = 14 V, V_D = -14 V	1 2	0.01		2 100		5 100	nA
			V_S = -14 V, V_D = 14 V	1 2	-0.02	-2 -100		-5 -100		
Drain OFF Leakage Current	$I_{D(OFF)}$		V_D = 14 V, V_S = -14 V	1 2	0.01		2 100		5 100	
			V_D = -14 V, V_S = 14 V	1 2	-0.02	-2 -100		-5 -100		
Channel ON Leakage Current [f]	$I_{D(ON)}$ + $I_{S(ON)}$	V_S = V_D = 14 V, V_{IN} = 0.8 V		1 2	0.1		2 200		5 200	
		V_S = V_D = -14 V, V_{IN} = 0.8 V		1 2	-0.1	-2 -200		-5 -200		
INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 2.4 V		1 2	0.0009	-0.5 -1		-1 -10		µA
		V_{IN} = 15 V		1 2	0.005		.5 1		1 10	
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		1 2	-0.0015	-0.5 -1		-1 -10		

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ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = +15 V, V- = -15 V, GND = 0 V	LIMITS 1=25°C, 2=125,85,70°C, 3=-55,-25,0°C		A SUFFIX -55 to 125°C		B,C SUFFIX		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
DYNAMIC									
Turn-ON Time	t_{ON}	See Switching Time Test Circuit	1	440		1000		1000	ns
Turn-OFF Time	t_{OFF}		1	340		425		425	
Charge Injection	Q	C_L = 1000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	1	-10					pC
Source-OFF Capacitance	$C_{S(OFF)}$	V_S = 0 V, V_{IN} = 5 V, f = 140 kHz	1	9					pF
Drain-OFF Capacitance	$C_{D(OFF)}$	V_D = 0 V, V_{IN} = 5 V, f = 140 kHz	1	9					
Channel ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	V_D = V_S = 0 V, V_{IN} = 0 V	1	25					
OFF Isolation [e]		V_{IN} = 5 V, Z_L = 75 Ω, V_S = 2 V, f = 1 MHz	1	75					dB
Crosstalk (Channel-to-Channel)			1	90					
SUPPLY									
Positive Supply Current	I+	Both Channels ON or OFF, V_{IN} = 0 V and 2.4 V	1	0.8		2		2	mA
Negative Supply Current	I-		1	-0.23	-1		-1		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. OFF Isolation = 20 log V_S/V_D, V_S = input to OFF switch, V_D = output.
f. $I_{D(ON)}$ is leakage from driver into "ON" switch.

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DIE TOPOGRAPHY

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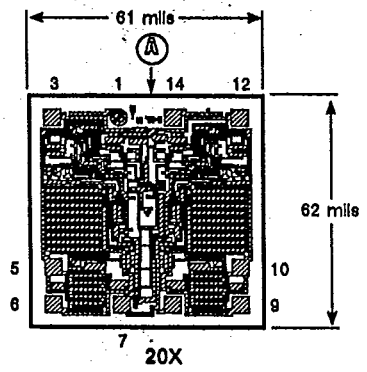


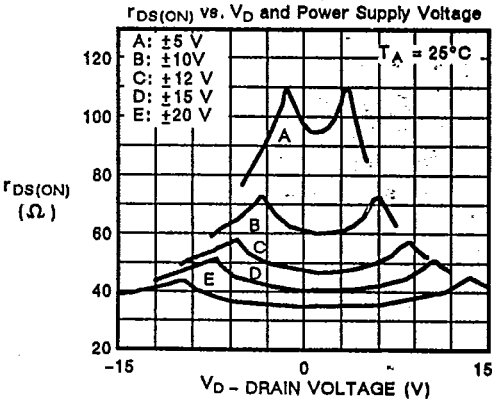
Pad No.	Function
1	Input 2
3	Ground
5	Source 2
6	Drain 2
7	V-
9	Drain 1
10	Source 1
12	V+ (Substrate)
14	Input 1

ICMEA

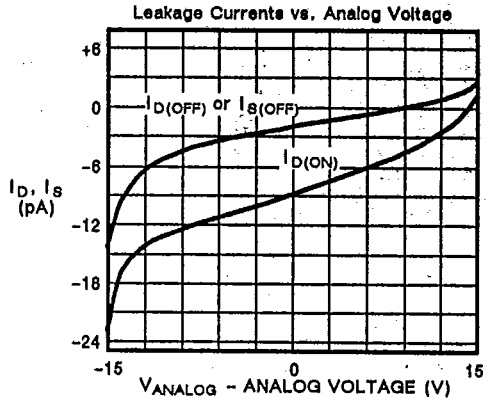
4 Capacitors
7 Resistors
25 P-channel enhancement MOSFETs
23 N-channel enhancement MOSFETs
8 Diodes

TYPICAL CHARACTERSITICS

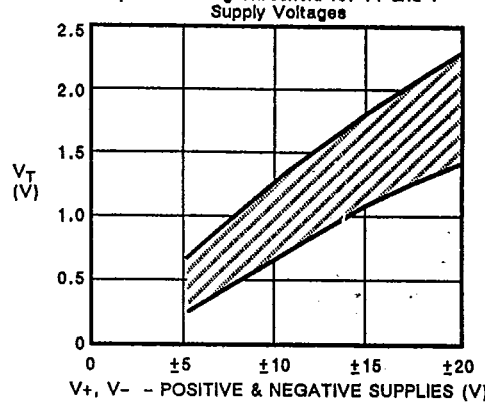
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



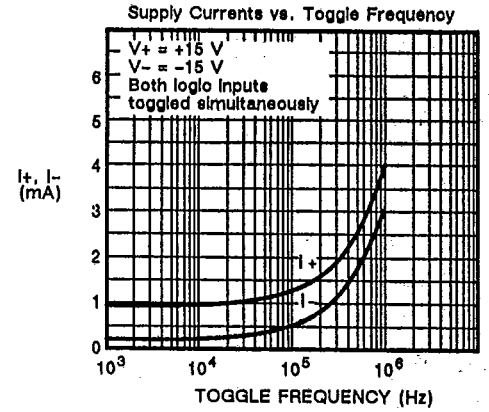
Leakage Currents vs. Analog Voltage



Input Switching Threshold vs. V+ and V- Supply Voltages



Supply Currents vs. Toggle Frequency



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SWITCHING TIME TEST CIRCUIT

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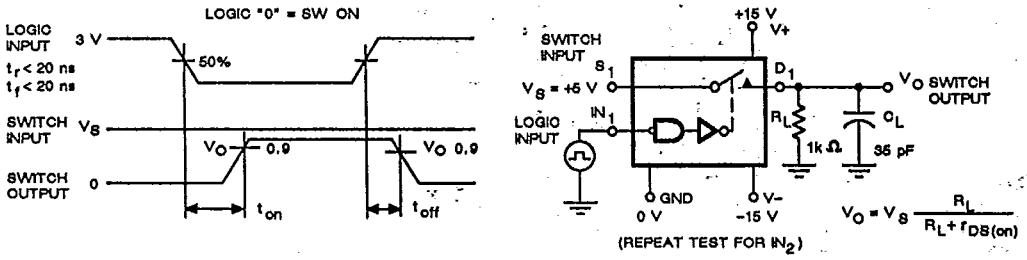
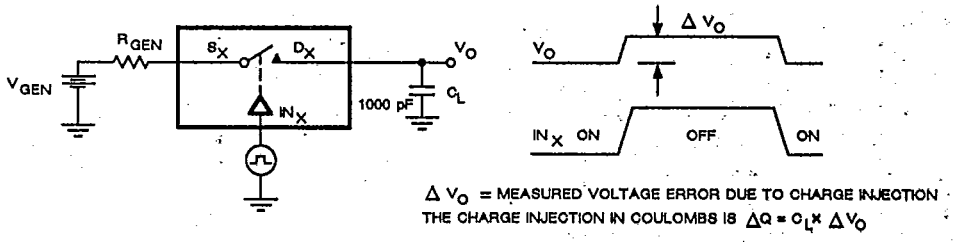
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

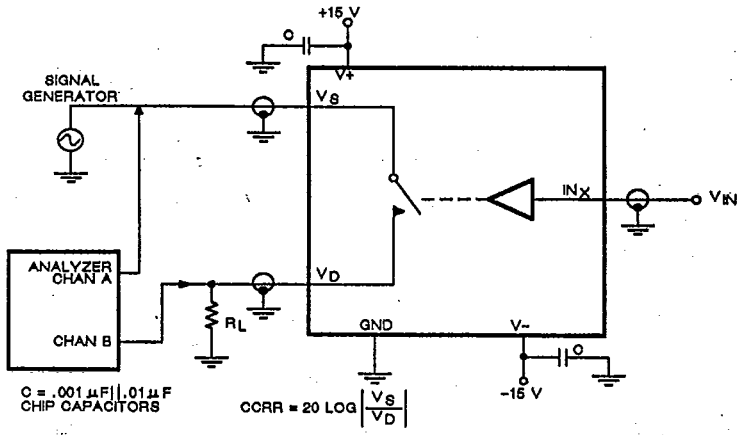


CHARGE INJECTION TEST CIRCUIT



ΔV_O = MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION
THE CHARGE INJECTION IN COULOMBS IS $\Delta Q = C_L \times \Delta V_O$

OFF ISOLATION TEST CIRCUIT



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CHANNEL-TO-CHANNEL CROSSTALK TEST CIRCUIT

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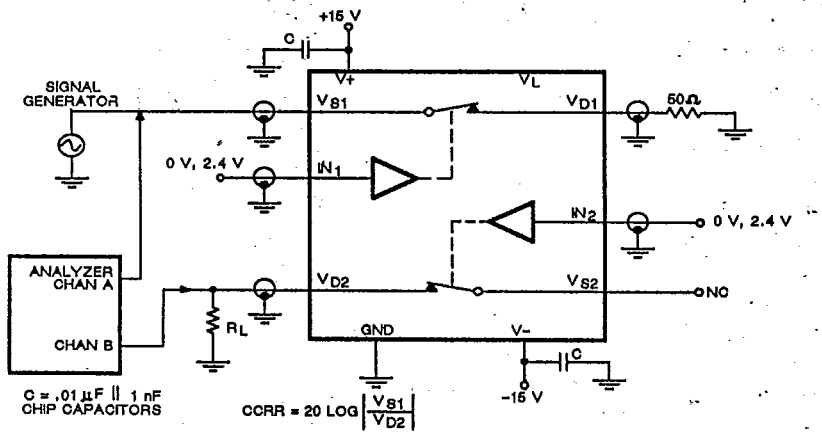
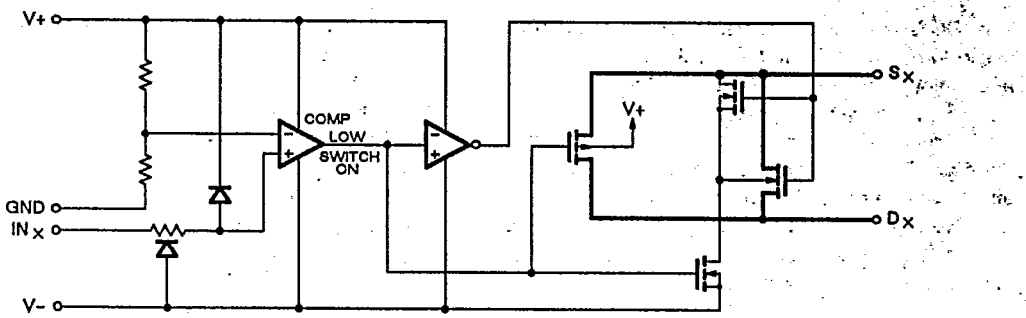
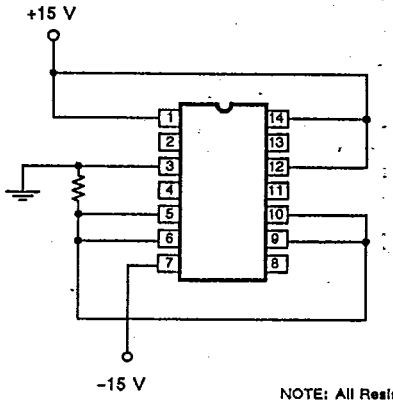


SCHEMATIC DIAGRAM (Typical Channel)

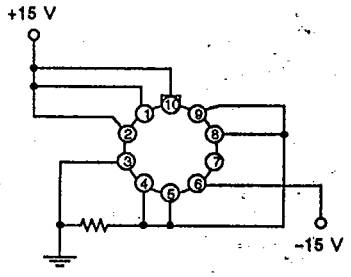


BURN-IN DIAGRAMS

Dual-In-Line Packages



Metal Can Package



NOTE: All Resistors are 10 kΩ unless otherwise specified.

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