PRELIMINARY

CY2273

Pentium™ and Pentium II™ Clock Synthesizer/Driver for the Intel 82430TX and ALI Chipsets with 3 DIMM Support

Features

- **Mixed 2.5V and 3.3V operation**
- **Complete clock solution for Pentium™, Pentium II™, Cyrix, and AMD processor-based motherboards**
  - **— Four CPU clocks at 2.5V or 3.3V**
  - **— Twelve 3.3V SDRAM clocks**
  - **— Seven synchronous PCI clocks, one free-running**
  - **— One 3.3V 48 MHz USB clock**
  - **— One 3.3V Ref. clock at 14.318 MHz**
- **1 ns–4 ns delay between CPU and PCI clocks on -1 and -2, no delay on -3.**
- **I^2C™ Serial Configuration Interface**
- **Factory-EPROM programmable output drive and slew rate for optimal EMI control. Improved output drivers are designed for low EMI.**
- **Factory-EPROM programmable CPU clock frequencies for custom configurations**
- **Power-down, CPU stop and PCI stop pins**
- **Low CPU clock jitter ≤ 250 ps cycle-cycle.**
- **Available in space-saving 48-pin SSOP package**

Functional Description

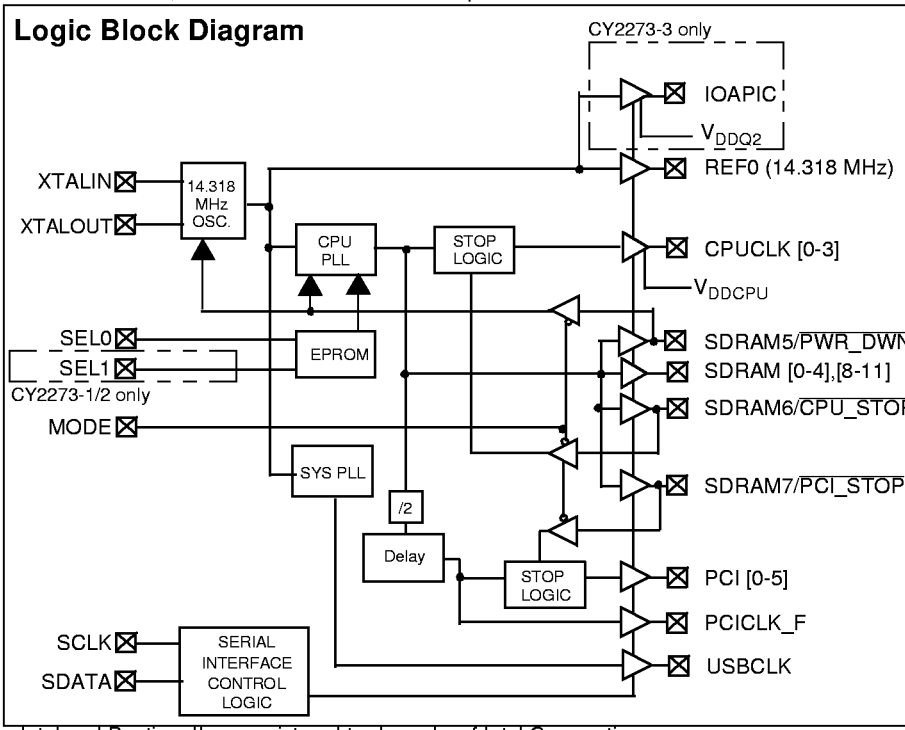
The CY2273 family are clock Synthesizer/Driver devices for a Pentium, Pentium II, Cyrix, or AMD processor-based PC using Intel's 82430TX, Aladdin IV or Aladdin V chipsets.

The CY2273-1 outputs four CPU clocks at 2.5V or 3.3V. There are seven PCI clocks, running at one half the CPU clock frequency. One of the PCI clocks is free-running. Additionally, the part outputs twelve 3.3V SDRAM clocks, one 3.3V USB clock at 48 MHz, and one 3.3V reference clock at 14.318 MHz. All output clocks meet Intel's drive strength, rise/fall time, jitter, accuracy, and skew requirements. The CY2273-2 is similar, except that PCICLK4 and PCICLK5 are now AGP clocks. The CY2273-3 is more suited to Pentium II systems, as it outputs one 2.5V IOAPIC clock.

The part possesses power-down, CPU stop, and PCI stop pins for power management control. These inputs are multiplexed with SDRAM clock outputs, and are selected when the MODE pin is driven low. Additionally, the signals are synchronized on-chip, and ensure glitch-free transitions on the outputs. When the $\overline{\text{CPU\_STOP}}$ input is asserted, the CPU clock outputs are driven LOW. When the $\overline{\text{PCI\_STOP}}$ input is asserted, the PCI clock outputs (except the free-running PCI clock) are driven LOW. When the $\overline{\text{PWR\_DWN}}$ pin is asserted, the reference oscillator and PLLs are shut down, and all outputs are driven LOW.

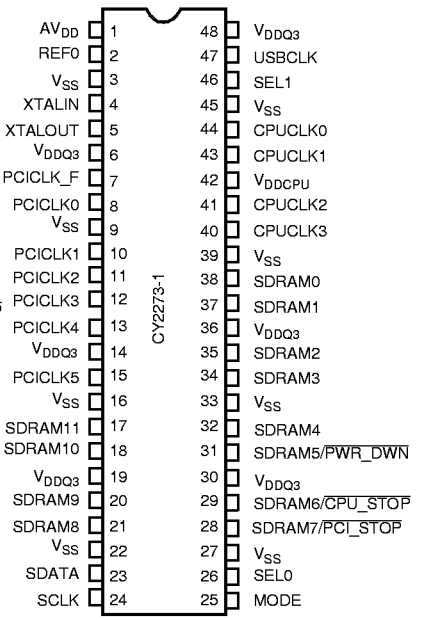
The CY2273 clock outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2273 to have lower EMI than clock devices from other manufacturers. Additionally, factory-EPROM programmable output drive and slew-rate control enable optimal configurations.

Logic Block Diagram

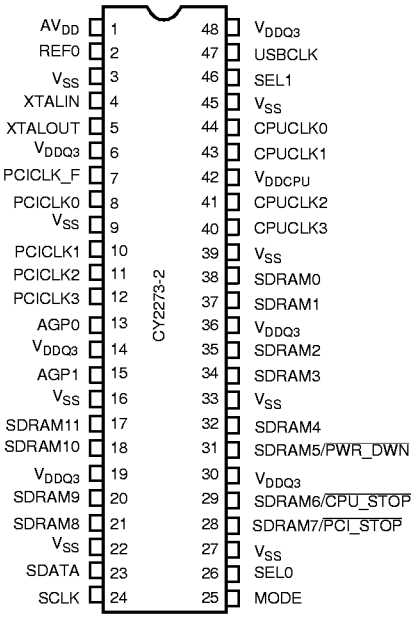


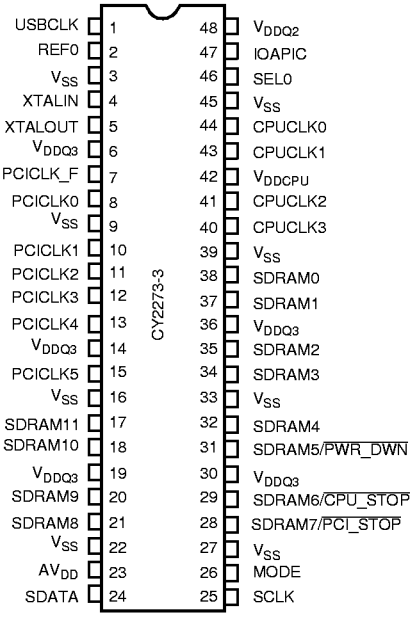
Pin Configuration

SSOP
Top View



Pin Configurations (continued)





Pin Summary

Name	Pins (-1, -2)	Pins (-3)	Description
V_{DDQ3}	6, 14, 19, 30, 36, 48	6, 14, 19, 30, 36	3.3V Digital voltage supply
V_{DDQ2}	N/A	48	IOAPIC Digital voltage supply, 2.5V
V_{DDCPU}	42	42	CPU Digital voltage supply, 2.5V or 3.3V
AV_{DD}	1	23	Analog voltage supply, 3.3V
V_{SS}	3, 9, 16, 22, 27, 33, 39, 45	3, 9, 16, 22, 27, 33, 39, 45	Ground
XTALIN[1]	4	4	Reference crystal input
XTALOUT[1]	5	5	Reference crystal feedback
SDRAM7/ $\overline{\text{PCI\_STOP}}$	28	28	SDRAM clock output. Also, active low control input to stop PCI clocks, enabled when MODE is Low
SDRAM6/ $\overline{\text{CPU\_STOP}}$	29	29	SDRAM clock output. Also, active low control input to stop CPU clocks, enabled when MODE is Low.
SDRAM5/ $\overline{\text{PWR\_DWN}}$	31	31	SDRAM clock output. Also, active low control input to power down device, enabled when MODE is Low.
SDRAM[0:4],[8:11]	38, 37, 35, 34, 32, 21, 20, 18, 17	38, 37, 35, 34, 32, 21, 20, 18, 17	SDRAM clock outputs
SEL0	26	46	CPU frequency select input, bit 0 (See table below.)
SEL1	46	N/A	CPU frequency select input, bit 0 (See table below.)
CPUCLK[0:3]	44, 43, 41, 40	44, 43, 41, 40	CPU clock outputs
PCICLK[0:5]	8, 10, 11, 12, 13, 15	8, 10, 11, 12, 13, 15	PCI clock outputs, at one-half the CPU frequency. Pins 13 and 15 are AGP clocks in -2
PCICLK_F	7	7	Free-running PCI clock output
IOAPIC	N/A	47	IOAPIC clock output
REF0	2	2	3.3V Reference clock output
USBCLK	47	1	USB Clock output
SDATA	23	24	Serial data input for serial configuration port
SCLK	24	25	Serial clock input for serial configuration port
MODE	25	26	Mode Select pin for enabling power management features

Note:
1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.

Function Table

SEL1	SEL0	CPU/PCI Ratio	CPUCLK[0:3] SDRAM[0:11]	PCICLK[0:5] PCICLK_F	AGP (-2 Only)	REF0 IOAPIC	USBCLK
0	0	2	60.0 MHz	30.0 MHz	60.0 MHz	14.318 MHz	48 MHz
0	1	2	66.67 MHz	33.33 MHz	66.66 MHz	14.318 MHz	48 MHz
1	0	2.5	75.0 MHz	30.0 MHz	60.0 MHz	14.318 MHz	48 MHz
1	1	2.5	83.33 MHz	33.33 MHz	66.66 MHz	14.318 MHz	48 MHz

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	–195
CPUCLK	60.0	60.0	0
CPUCLK	75.0	75.0	0
CPUCLK	83.33	83.138	–1947
USBCLK	48.0	48.008	167

CPU and PCI Clock Driver Strengths

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V.

Power Management Logic[2] - Active when MODE pin is held 'LOW'

CPU_STOP	PCI_STOP	PWR_DWN	CPUCLK	PCICLK	PCICLK_F	Other Clocks	Osc.	PLLs
X	X	0	Low	Low	Stopped	Stopped	Off	Off
0	0	1	Low	Low	Running	Running	Running	Running
0	1	1	Low	33/30 MHz	Running	Running	Running	Running
1	0	1	60/66/75/83 MHz	Low	Running	Running	Running	Running
1	1	1	60/66/75/83 MHz	30/33/30/33 MHz	Running	Running	Running	Running

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  .

  .

  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to "0".
- I^2C Address for the CY2273 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Byte 0: Functional and Frequency Select Clock Register (1 = Enable, 0 = Disable)

Bit	Pin #	Description	
Bit 7	--	(Reserved) drive to '0'	
Bit 6	--	(Reserved) drive to '0'	
Bit 5	--	(Reserved) drive to '0'	
Bit 4	--	(Reserved) drive to '0'	
Bit 3	--	(Reserved) drive to '0'	
Bit 2	--	(Reserved) drive to '0'	
Bit 1 Bit 0	--	Bit 1 1 1 0 0	Bit 0 1 - Three-State 0 - N/A 1 - Testmode 0 - Normal Operation

Select Functions

Functional Description	Outputs					
	CPU	PCI, PCI_F	SDRAM	Ref	IOAPIC	USBCLK
Three-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode[4]	TCLK/2[3]	TCLK/4	TCLK/2	TCLK	TCLK	TCLK/2

Notes:

2. AGP clocks are driven on PCICLK5 and PCICLK4 on -2 option. These clocks behave similar to the PCICLK_F output, in that they are free-running and stop only when the PWR_DWN pin is asserted. The frequency of the AGP clocks is as shown in the Function Table.
3. TCLK supplied on the XTALIN pin in Test Mode.
4. Valid only for SEL1=0

Byte 1: CPU Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	47 (-1/-2) 1 (-3)	USBCLK
Bit 6	N/A	(Reserved) drive to '0'
Bit 5	N/A	(Reserved) drive to '0'
Bit 4	N/A	Not used - drive to '0'
Bit 3	40	CPUCLK3 (Active/Inactive)
Bit 2	41	CPUCLK2 (Active/Inactive)
Bit 1	43	CPUCLK1 (Active/Inactive)
Bit 0	44	CPUCLK0 (Active/Inactive)

Byte 2: PCI Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	--	(Reserved) drive to '0'
Bit 6	7	PCICLK_F (Active/Inactive)
Bit 5	15	PCICLK5 (Active/Inactive) (-1 and -3) AGP1 (Active/Inactive) (-2 only)
Bit 4	14	PCICLK4 (Active/Inactive) (-1 and -3) AGP0 (Active/Inactive) (-2 only)
Bit 3	12	PCICLK3 (Active/Inactive)
Bit 2	11	PCICLK2 (Active/Inactive)
Bit 1	10	PCICLK1 (Active/Inactive)
Bit 0	8	PCICLK0 (Active/Inactive)

Byte 3: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	28	SDRAM7 (Active/Inactive)
Bit 6	29	SDRAM6 (Active/Inactive)
Bit 5	31	SDRAM5 (Active/Inactive)
Bit 4	32	SDRAM4 (Active/Inactive)
Bit 3	34	SDRAM3 (Active/Inactive)
Bit 2	35	SDRAM2 (Active/Inactive)
Bit 1	37	SDRAM1 (Active/Inactive)
Bit 0	38	SDRAM0 (Active/Inactive)

Byte 4: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	N/A	Not used - drive to '0'
Bit 6	N/A	Not used - drive to '0'
Bit 5	N/A	Not used - drive to '0'
Bit 4	N/A	Not used - drive to '0'
Bit 3	17	SDRAM11
Bit 2	18	SDRAM10
Bit 1	20	SDRAM9
Bit 0	21	SDRAM8

Byte 5: Peripheral Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	N/A	(Reserved) drive to '0'
Bit 6	N/A	(Reserved) drive to '0'
Bit 5	N/A	(Reserved) drive to '0'
Bit 4	47	IOAPIC (Active/Inactive) (-3 ONLY)
Bit 3	N/A	(Reserved) drive to '0'
Bit 2	N/A	(Reserved) drive to '0'
Bit 1	N/A	(Reserved) drive to '0'
Bit 0	2	REF0 (Active/Inactive)

Byte 6: Reserved, for future use

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5 to +7.0V

Input Voltage ..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[5]

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DDQ3}	Analog and Digital Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375 3.135	2.9 3.465	V
V_{DDQ2}	IOAPIC Supply Voltage	2.375	2.9	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK, USBCLK, IOAPIC PCICLK, AGP, SDRAM REF0	 10 30, 20 20	 20 30 45	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	V_{DDCPU} = V_{DDQ2} = 2.375V	I_{OH} = 16 mA	CPUCLK	2.0		V
			I_{OH} = 18 mA	IOAPIC			
V_{OL}	Low-level Output Voltage	V_{DDCPU} = V_{DDQ2} = 2.375V	I_{OL} = 27 mA	CPUCLK		0.4	V
			I_{OL} = 29 mA	IOAPIC			
V_{OH}	High-level Output Voltage	V_{DDQ3}, AV_{DD}, V_{DDCPU} = 3.135V	I_{OH} = 16 mA	CPUCLK	2.4		V
			I_{OH} = 36 mA	SDRAM			
			I_{OH} = 32 mA	PCICLK			
			I_{OH} = 26 mA	USBCLK			
			I_{OH} = 36 mA	REF0			
V_{OL}	Low-level Output Voltage	V_{DDQ3}, AV_{DD}, V_{DDCPU} = 3.135V	I_{OL} = 27 mA	CPUCLK		0.4V	V
			I_{OL} = 29 mA	SDRAM			
			I_{OL} = 26 mA	PCICLK			
			I_{OL} = 21 mA	USBCLK			
			I_{OL} = 29 mA	REF0			
I_{IH}	Input High Current	V_{IH} = V_{DD}			–10	+10	µA
I_{IL}	Input Low Current	V_{IL} = 0V				10	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD}	Power Supply Current[6]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU clocks = 66.67 MHz				300	mA
I_{DD}	Power Supply Current[6]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Unloaded Outputs				120	mA
I_{DDS}	Power-down Current	Current draw in power-down state				50	µA

Notes:

5. Electrical parameters are guaranteed with these operating conditions.
6. Power supply current will vary with number of outputs which are running. Therefore, power supply current can be calculated with the following formula: TBD

Switching Characteristics[7]

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle[8]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_2	CPUCLK, IOAPIC	CPU and IOAPIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V, V_{DDCPU} = 2.5V Between 0.4V and 2.4V, V_{DDCPU} = 3.3V	1.0		4.0	V/ns
t_2	PCICLK, AGP, REF0	PCI, AGP, REF0 Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t_2	SDRAM	SDRAM Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t_3	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V_{DDCPU} = 2.5V Between 0.4V and 2.4V, V_{DDCPU} = 3.3V	0.4 0.5		1.6 2.0	ns
t_4	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V_{DDCPU} = 2.5V Between 2.4V and 0.4V, V_{DDCPU} = 3.3V	0.4 0.5		1.6 2.0	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V_{DDCPU} = 2.5V Measured at 1.5V, V_{DDCPU} = 3.3V		100	250	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew (-1, -2)	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0	2.0	4.0	ns
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew (-3)	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			0.5	ns
t_7	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			500	ps
t_8	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			250	ps
t_9	PCICLK, AGP	PCICLK-AGP Clock Skew	Measured at 1.5V			250	ps
t_{10}	CPUCLK, SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			250	ps
t_{10}	PCICLK, AGP	Cycle-Cycle Clock Jitter	Measured at 1.5V			500	ps
t_{11}	CPUCLK, PCICLK, AGP, SDRAM	Power-up Time	CPU, PCI, AGP, and SDRAM clock stabilization from power-up			3	ms

Notes:

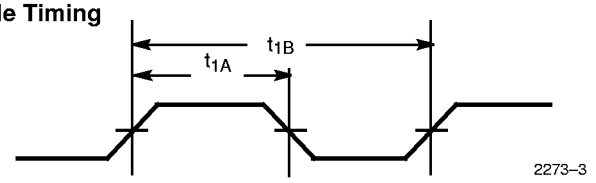
7. All parameters specified with loaded outputs.
8. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DDCPU} = 2.5V, CPUCLK duty cycle is measured at 1.25V.

Timing Requirement for the I²C Bus

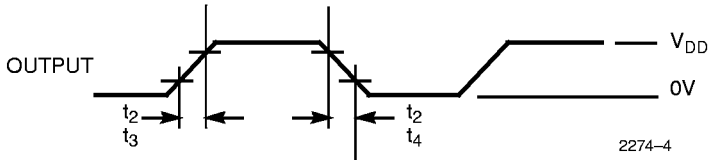
Parameter	Description	Min.	Max.	Unit
t_{12}	SCLK Clock Frequency	0	100	kHz
t_{13}	Time the bus must be free before a new transmission can start	4.7		µs
t_{14}	Hold time start condition. After this period the first clock pulse is generated.	4		µs
t_{15}	The Low period of the clock.	4.7		µs
t_{16}	The High period of the clock.	4		µs
t_{17}	Set-up time for start condition. (Only relevant for a repeated start condition.)	4.7		µs
t_{18}	Hold time DATA for CBUS compatible masters. for I²C devices	 5 0		µs
t_{19}	DATA input set-up time	250		ns
t_{20}	Rise time of both SDATA and SCLK inputs		1	µs
t_{21}	Fall time of both SDATA and SCLK inputs		300	ns
t_{22}	Se-up time for stop condition	4.0		µs

Switching Waveforms

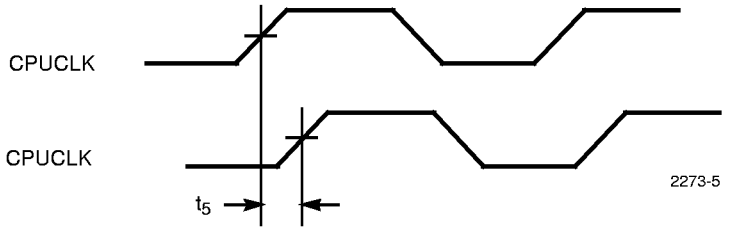
Duty Cycle Timing



All Outputs Rise/Fall Time

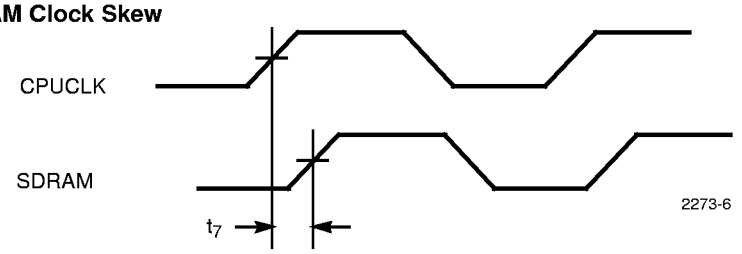


CPU-CPU Clock Skew

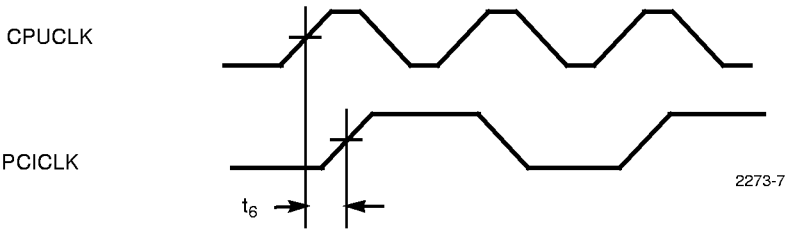


Switching Waveforms (continued)

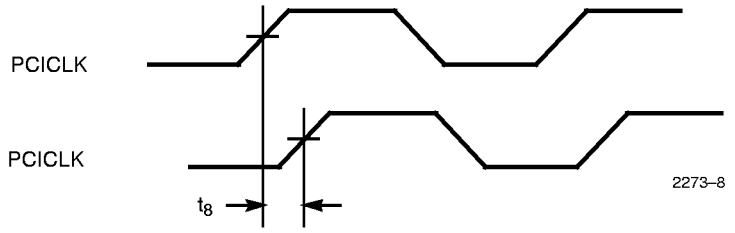
CPU-SDRAM Clock Skew



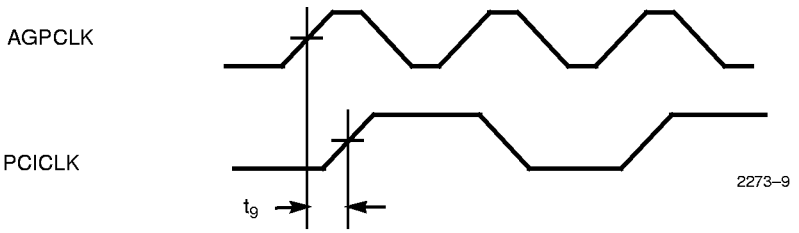
CPU-PCI Clock Skew



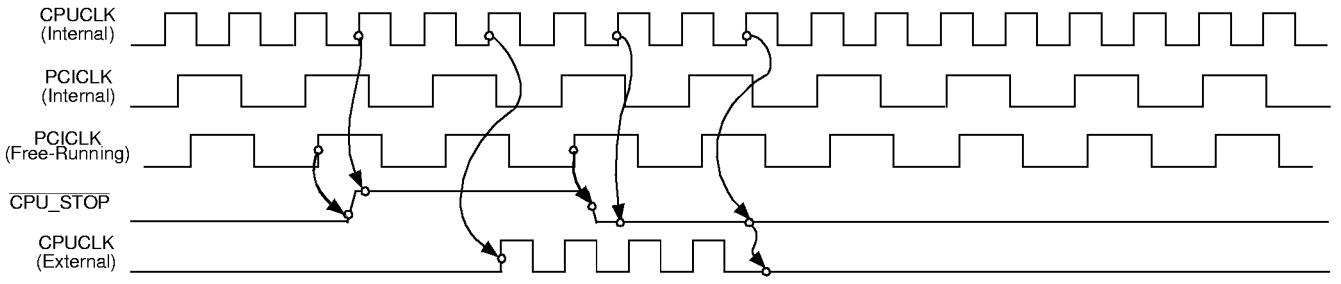
PCI-PCI Clock Skew



AGP-PCI Clock Skew



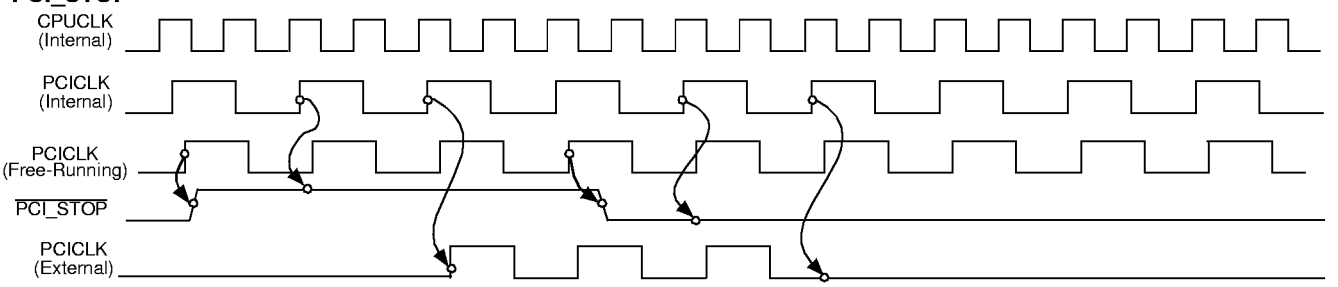
$\overline{\text{CPU\_STOP}}$[9, 10]



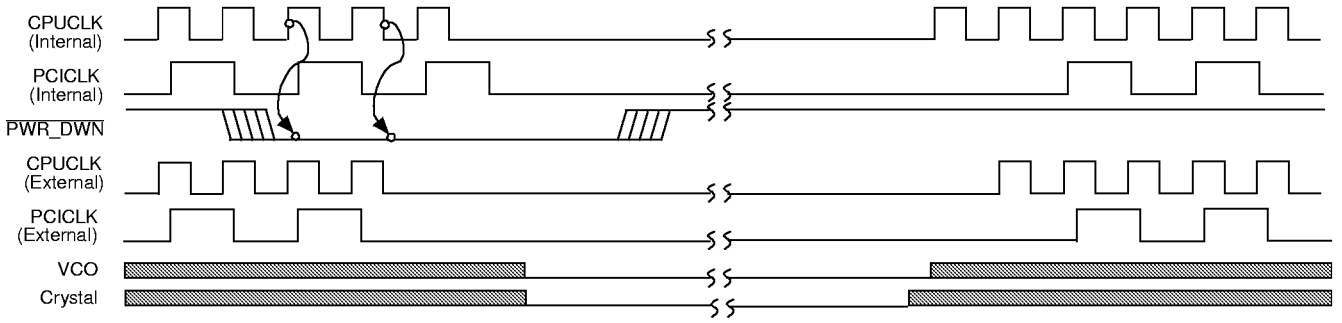
Notes:
9. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
10. CPU_STOP may be applied asynchronously. It is synchronized internally.

Switching Waveforms (continued)

PCI_STOP[11, 12]

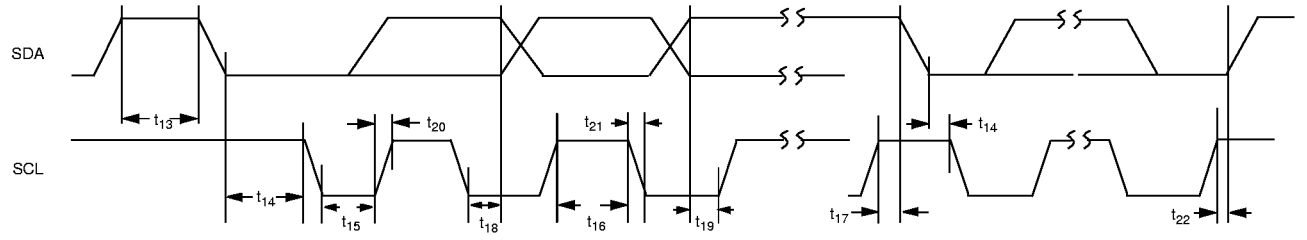


PWR_DOWN



Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Timing Requirements for the I^2C Bus



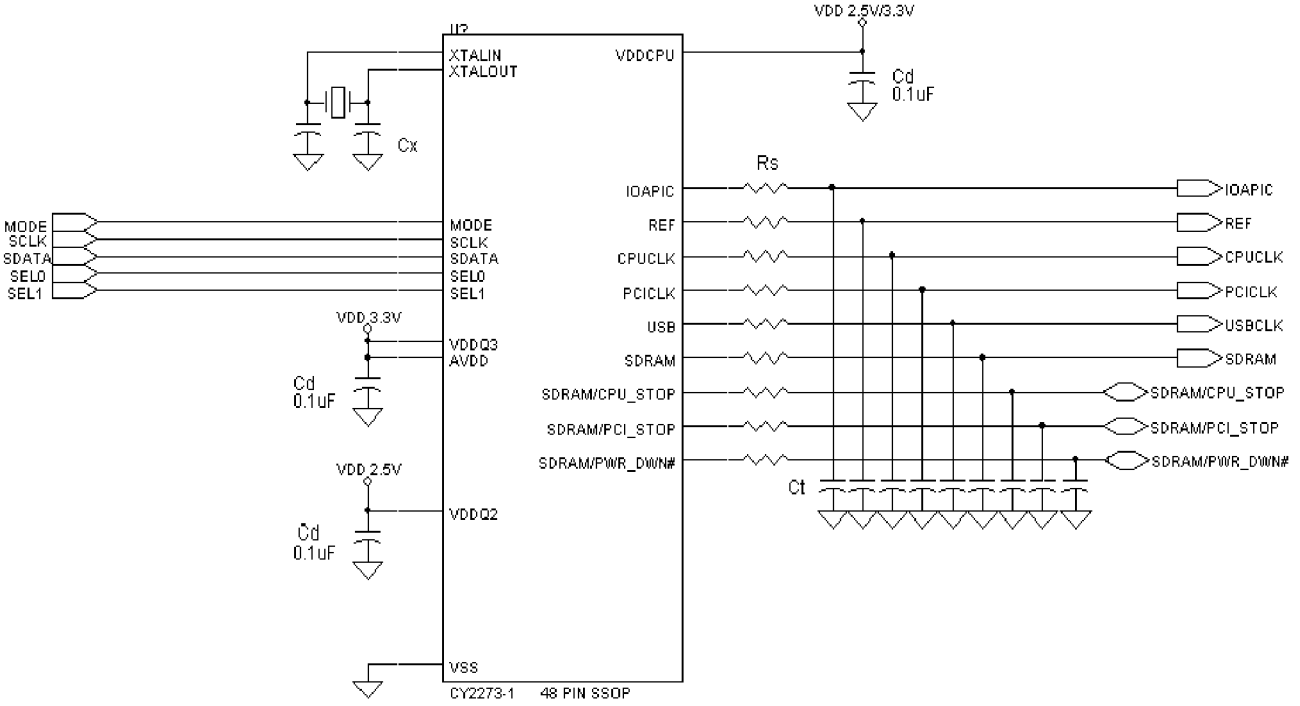
Notes:

11. PCICLK on and PCICLK off latency is 1 rising edge of the external PCICLK.
12. PCI_STOP may be applied asynchronously. It is synchronized internally.

Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit



Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

Rs = SERIES TERMINATING RESISTORS

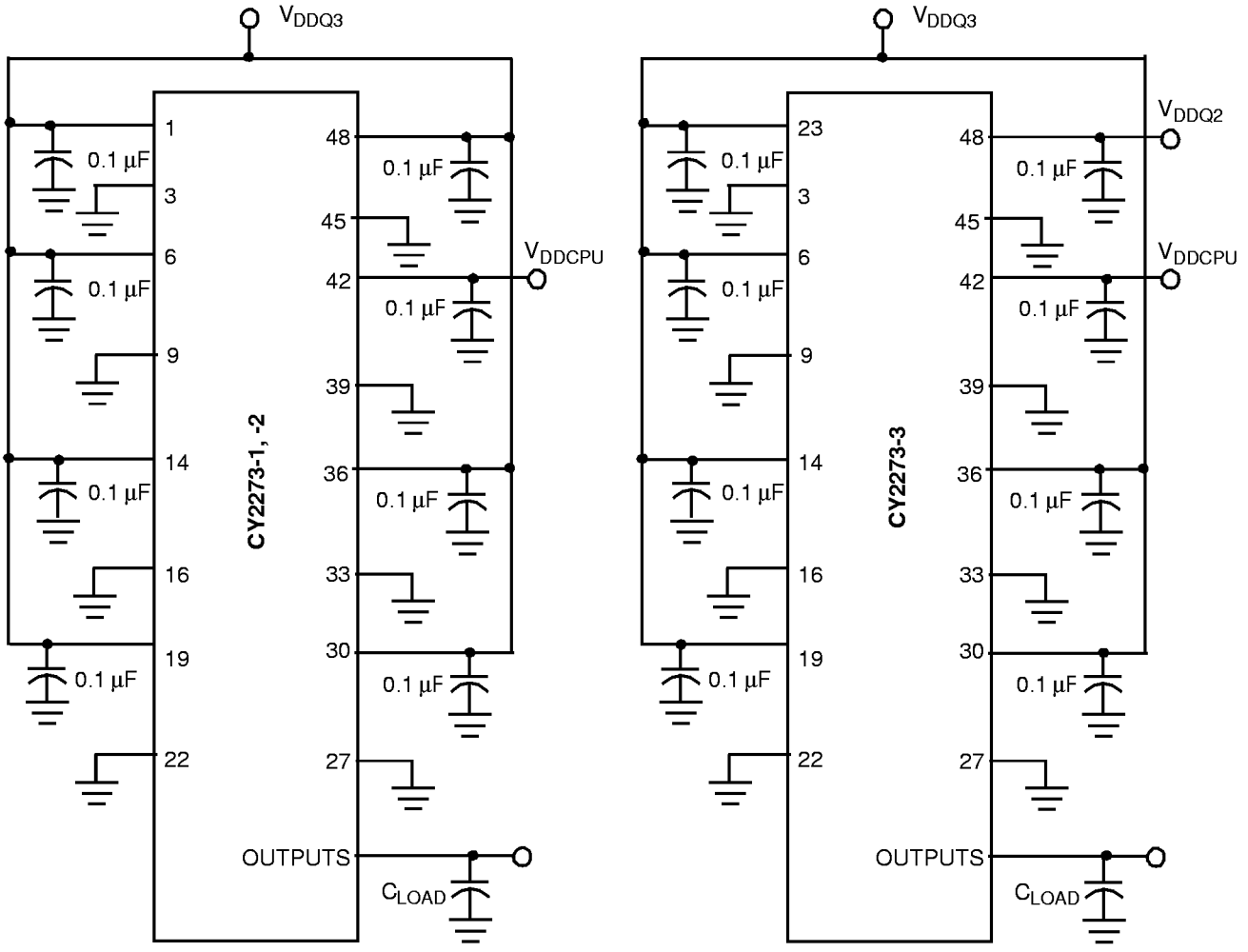
Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (specified in the data sheet), and R_{series} is the series terminating resistor.

  $$R_{series} \geq R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note “Layout and Termination Techniques for Cypress Clock Generators” for more details.
- If a Ferrite Bead is used, a 10 µF– 22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Note: All Capacitors must be placed as close to the pins as is possible

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2273PVC–1	O48	48-Pin SSOP	Commercial
CY2273PVC–2	O48	48-Pin SSOP	Commercial
CY2273PVC–3	O48	48-Pin SSOP	Commercial

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Package Diagram

48-Lead Shrunk Small Outline Package O48