



MOTOROLA

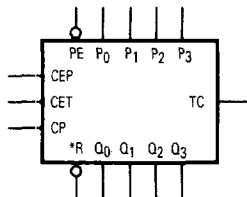
Product Preview

Synchronous Presettable Binary Counter

The MC74AC161/74ACT161 and MC74AC163/74ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74AC161/74ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74AC163/74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- 'ACT161 and 'ACT163 Have TTL Compatible Inputs

LOGIC SYMBOL



- * \overline{MR} for '161
- * \overline{SR} for '163

PIN NAMES

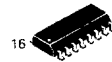
- CEP Count Enable Parallel Input
- CET Count Enable Trickle Input
- CP Clock Pulse Input
- \overline{MR} ('161) Asynchronous Master Reset Input
- \overline{SR} ('163) Synchronous Reset Input
- P_0 - P_3 Parallel Data Inputs
- PE Parallel Enable Input
- Q_0 - Q_3 Flip-Flop Outputs
- TC Terminal Count Output

MC74AC161
MC74ACT161
MC74AC163
MC74ACT163

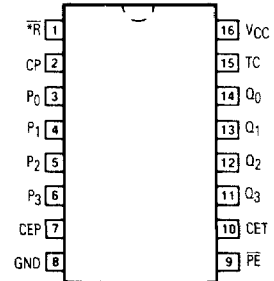
**SYNCHRONOUS
 PRESETTABLE
 BINARY COUNTER**



**N SUFFIX
 CASE 648-08
 PLASTIC**



**D SUFFIX
 CASE 751B-03
 PLASTIC**



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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

The MC74AC161/74ACT161 and MC74AC163/74ACT163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('161), synchronous reset ('163), parallel load, count-up and hold. Five control inputs — Master Reset (\overline{MR} , '161), Synchronous Reset (\overline{SR} , '163), Parallel Enable (\overline{PE}), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on \overline{MR} overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on \overline{SR} overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on \overline{PE} overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded

into the flip-flops on the next rising edge of CP. With \overline{PE} and \overline{MR} ('161) or \overline{SR} ('163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74AC161/74ACT161 and MC74AC163/74ACT163 use D-type edge-triggered flip-flops and changing the \overline{SR} , \overline{PE} , CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

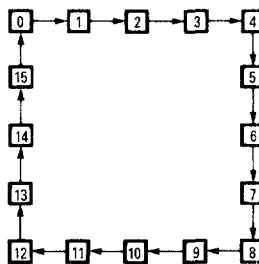
Logic Equations: Count Enable = $CEP \cdot CET \cdot \overline{PE}$
 TC = $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$

MODE SELECT TABLE

* \overline{SR}	\overline{PE}	CET	CEP	Action on the Rising Clock Edge ()
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

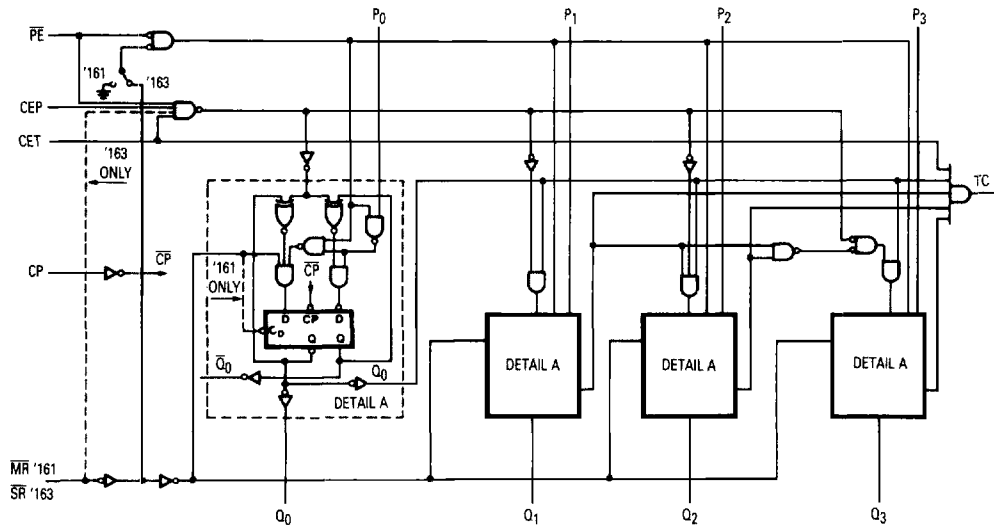
*For '163 only
 H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

STATE DIAGRAM



MC74AC161 • MC74ACT161 • MC74AC163 • MC74ACT163

BLOCK DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I _{CC}	Maximum Quiescent Supply Current	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C
I _{CC(T)}	Maximum Additional I _{CC} /Input ('ACT161/163)	1.5	mA	V _{IN} = V _{CC} - 2.1 V, V _{CC} = 5.5 V, T _A = Worst Case

MC74AC161 • MC74ACT161 • MC74AC163 • MC74ACT163

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC161			74ACT161		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	3.3 5.0		87 118				MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	3.3 5.0		7.5 5.5				ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	3.3 5.0		8.5 6.0				ns	3-6
t _{PLH}	Propagation Delay CP to TC	3.3 5.0		9.5 7.0				ns	3-6
t _{PHL}	Propagation Delay CP to TC	3.3 5.0		11 8.0				ns	3-6
t _{PLH}	Propagation Delay CET to TC	3.3 5.0		7.5 5.5				ns	3-6
t _{PHL}	Propagation Delay CET to TC	3.3 5.0		8.5 6.0				ns	3-6
t _{PLH}	Propagation Delay MR to Q _n	3.3 5.0		8.5 6.0				ns	3-6
t _{PHL}	Propagation Delay MR to TC	3.3 5.0		11 8.0				ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC161		74ACT161		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to CP	3.3 5.0	5.5 4.0				ns	3-9
t _h	Hold Time, HIGH or LOW P _n to CP	3.3 5.0	-7.0 -5.0				ns	3-9
t _s	Setup Time, HIGH or LOW S _R to CP	3.3 3.3	5.5 4.0				ns	3-9
t _h	Hold Time, HIGH or LOW S _R to CP	3.3 5.0	-7.5 -5.5				ns	3-9
t _s	Setup Time, HIGH or LOW P _E to CP	3.3 5.0	5.5 4.0				ns	3-9
t _h	Hold Time, HIGH or LOW P _E to CP	3.3 5.0	-7.5 -5.5				ns	3-9
t _s	Setup Time, HIGH or LOW C _{EP} or C _{ET} to CP	3.3 5.0	3.5 2.5				ns	3-9
t _h	Hold Time, HIGH or LOW C _{EP} or C _{ET} to CP	3.3 5.0	-4.5 -3.0				ns	3-9
t _w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0				ns	3-6
t _w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0				ns	3-6
t _w	M _R Pulse Width, LOW	3.3 5.0	4.5 3.0				ns	3-6
t _{rec}	Recovery Time M _R to CP	3.3 5.0	0 0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

MC74AC161 • MC74ACT161 • MC74AC163 • MC74ACT163

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT161			74ACT161		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	5.0	115	125		100		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	5.0	1.0	6.0	10.5	1.0	11.5	ns	3-6
t _{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11	1.0	12.5	ns	3-6
t _{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	12.5	1.0	13.5	ns	3-6
t _{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	8.5	1.0	10	ns	3-6
t _{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	9.5	1.0	10.5	ns	3-6
t _{PHL}	Propagation Delay MR to Q _n	5.0	1.0	6.0	10	1.0	11	ns	3-6
t _{PHL}	Propagation Delay MR to TC	5.0	1.0	8.0	13.5	1.0	14.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	VCC* (V)	74ACT161		74ACT161		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Pn to CP	5.0	4.0	9.5	11.5	ns	3-9	
th	Hold Time, HIGH or LOW Pn to CP	5.0	-5.0	0	0	ns	3-9	
ts	Setup Time, HIGH or LOW MR to CP	5.0	4.0	8.5	9.5	ns	3-9	
th	Hold Time, HIGH or LOW MR to CP	5.0	-5.5	-0.5	-0.5	ns	3-9	
ts	Setup Time, HIGH or LOW PE to CP	5.0	4.0	8.5	9.5	ns	3-9	
th	Hold Time, HIGH or LOW PE to CP	5.0	-5.5	-0.5	-0.5	ns	3-9	
ts	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	6.5	ns	3-9	
th	Hold Time, HIGH or LOW CEP or CET to CP	5.0	-3.0	0	0	ns	3-9	
tw	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.0	3.5	ns	3-6	
tw	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.0	3.5	ns	3-6	
tw	MR Pulse Width, LOW	5.0	3.0	3.0	7.5	ns	3-6	
trec	Recovery Time MR to CP	5.0	0	0	0.5	ns	3-9	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Conditions
CIN	Input Capacitance	4.5	pF	VCC = 5.0 V
CPD	Power Dissipation Capacitance	45	pF	VCC = 5.0 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC163			74AC163		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	3.3 5.0	70 110	87 118		60 95	MHz	3-3	
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0	1.0 1.0	13.5 9.5	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	12 9.5	1.0 1.0	13 10	ns	3-6
t _{PLH}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	9.5 7.0	15 10.5	1.0 1.0	16.5 11.5	ns	3-6
t _{PHL}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	11 8.0	14 11	1.0 1.0	15.5 11.5	ns	3-6
t _{PLH}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	7.5 5.5	9.5 6.5	1.0 1.0	11 7.5	ns	3-6
t _{PHL}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	8.5 6.0	11 8.5	1.0 1.0	12.5 9.5	ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC163		74AC163		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to CP	3.3 5.0	5.5 4.0	13.5 8.5	16 10.5	ns	3-9	
t _h	Hold Time, HIGH or LOW P _n to CP	3.3 5.0	-7.0 -5.0	-1.0 0	-0.5 0	ns	3-9	
t _s	Setup Time, HIGH or LOW SR to CP	3.3 5.0	5.5 4.0	14 9.5	16.5 11	ns	3-9	
t _h	Hold Time, HIGH or LOW SR to CP	3.3 5.0	-7.5 -5.5	-1.0 -0.5	-0.5 0	ns	3-9	
t _s	Setup Time, HIGH or LOW PE to CP	3.3 5.0	5.5 4.0	11.5 7.5	14 8.5	ns	3-9	
t _h	Hold Time, HIGH or LOW PE to CP	3.3 5.0	-7.5 -5.0	-1.0 -0.5	-0.5 0	ns	3-9	
t _s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5	7.0 5.0	ns	3-9	
t _h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	-4.5 -3.0	0 0	0 0.5	ns	3-9	
t _w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5	4.0 3.0	ns	3-6	
t _w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0	4.5 3.5	ns	3-6	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V



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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT163			74ACT163		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	5.0	120	128		105		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	5.0	1.0	5.5	10	1.0	11	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	5.0	1.0	6.0	11	1.0	12	ns	3-6
t _{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11.5	1.0	13.5	ns	3-6
t _{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	13.5	1.0	15	ns	3-6
t _{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	9.0	1.0	10.5	ns	3-6
t _{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	10	1.0	11	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT163		74ACT163		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _R to CP	5.0	4.0	10	12	ns	3-9	
t _h	Hold Time, HIGH or LOW P _R to CP	5.0	-5.0	0.5	0.5	ns	3-9	
t _s	Setup Time, HIGH or LOW S _R to CP	5.0	4.0	10	11.5	ns	3-9	
t _h	Hold Time, HIGH or LOW S _R to CP	5.0	-5.5	-0.5	-0.5	ns	3-9	
t _s	Setup Time, HIGH or LOW P _E to CP	5.0	4.0	8.5	10.5	ns	3-9	
t _h	Hold Time, HIGH or LOW P _E to CP	5.0	-5.5	-0.5	0	ns	3-9	
t _s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	6.5	ns	3-9	
t _h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	-3.0	0	0.5	ns	3-9	
t _w	Clock Pulse Width HIGH or LOW	5.0	2.0	3.5	3.5	ns	3-6	
t _w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5	3.5	ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Type	Units	Conditions
C _{I/N}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	45	pF	V _{CC} = 5.0 V