FT108SH7U, FT108RF7U, FT108UF7U, FT108SH5U, FT108RF5U, FT108UF5U

Operational Amplifier

General Description

The FT108 is a precision operational amplifier having specifications a factor of ten better than FET amplifiers over a −60°C to +125°C temperature range.
The devices operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with, and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary. The low current error of the FT108 makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 µV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 µF.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Ordering information

Table 1.

Part	Temp., °C	Package	Package drawing
FT108SH5U	-60 to +125	8-lead metal can	TO-5
FT108SH7U			
FT108RH5U		8-lead CDIP	CDIP-8
FT108RH7U			
FT108RF7U		14-lead CDIP	CDIP-14
FT108RF5U			
FT108UF5U		20-lead CLCC	CQFN-20
FT108UF7U			

Note: Military Screening available on request

Pin Function Description

Table 2.

Description	Mnemonic	Pin No			
		TO-5	CDIP-8	CDIP-14	CQFN-20
Compensation (A)	COMP(A)	1	1	2	2
Negative Input	-IN	2	2	4	5
Positive Input	+IN	3	3	5	7
Negative Supply	V_S-	4	4	7	10
Output	OUT	6	6	10	15
Positive Supply	V_S+	7	7	11	17
Compensation (B)	COMP(B)	8	8	12	20

TO-5 : Package is connected to Pin 4 (V−)

Process Flow

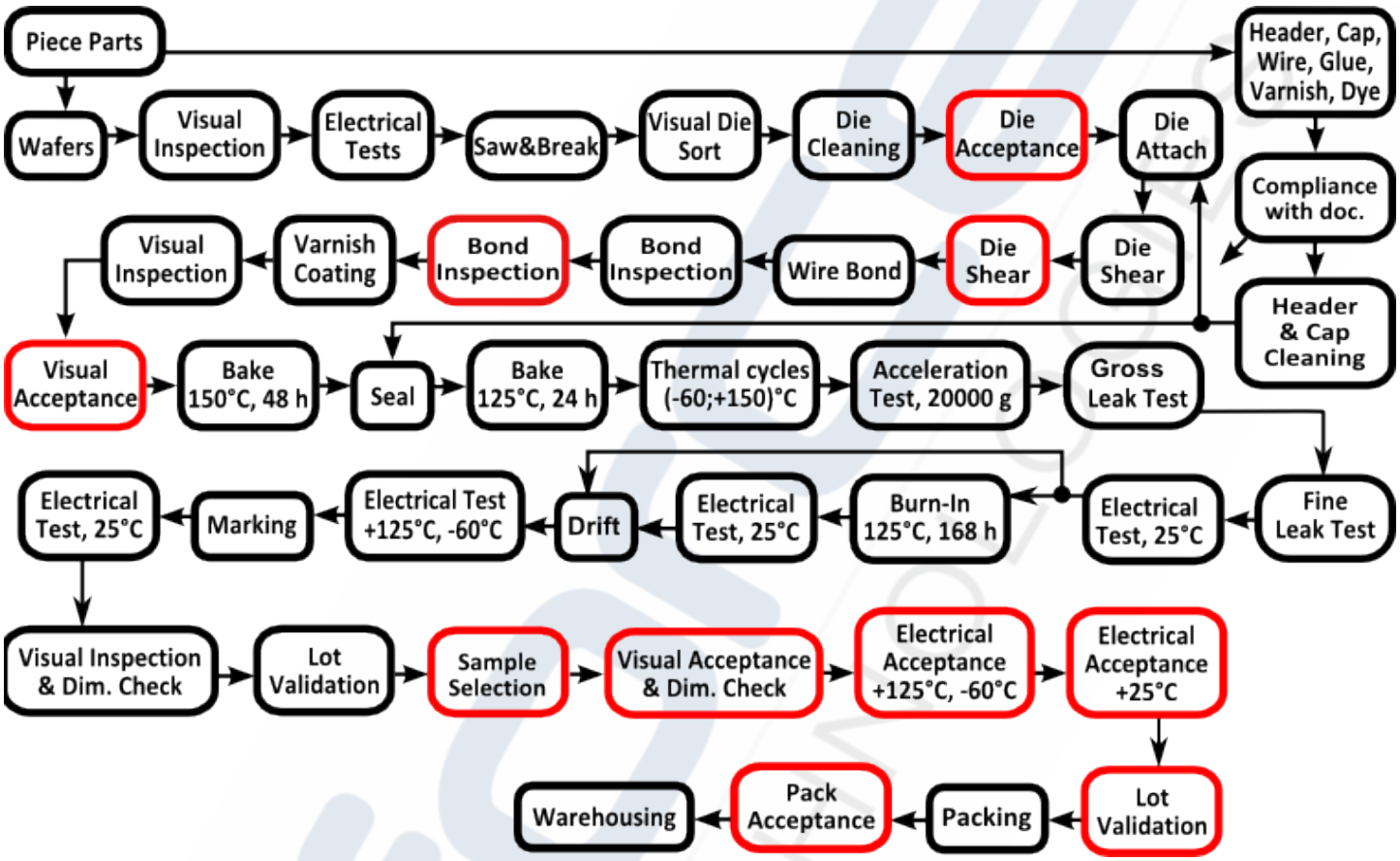


Figure1. Process Flow

Notes:

1. Colour shows the quality assurance procedures
2. Drift measurement is for quality level “7”

Absolute Maximum Ratings (T_{amb} = 25°C)

Table 3.

CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
Supply Voltage	V_{CC}	± 22	V	
Input Voltage	V_{IN}	± 15	V	Note 3
Differential Input Current	I_{DIFF}	± 10	mA	Note 4
Output Short Circuit Duration		Indefinite		
Storage Temperature Range	Tstg	-65/+150	°C	
Lead Temperature	T_{lead}	+300	°C	Soldering, 10 seconds
Power Dissipation	P_D	500	mW	Note 5
Maximum Thermal Resistance, junction to case	$R\ \Theta_{jC}$	TBD	°C/W	
Junction Temperature	T_J	+175	°C	

Notes:

3. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
4. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, if a differential input voltage in excess of 1 V is applied between the inputs, excessive current will flow, unless some limiting resistance is provided.
5. The maximum power dissipation must be derated at elevated temperatures and dictated by T_J, θ_{JA}, and T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J-T_A)/\theta_{JA}$ or the value specified here above, whichever is lower.

Thermal Information

Table 4.

Package	Resistance, °C/W		Dissipation, W	Derating above 75 °C, mW/°C
	θ_{JA}(note 6)	θ_{JC}(note 7)		
TO-5	160	75	0.63	6.3
CDIP-8	115	28	0.87	8.7
CDIP-14				
CQFN-20	75	23	1.33	13.3

Notes:

6. θ_{JA} is measured with component on an evaluation PC board in free air
7. For θ_{JC} "case temp" location is the center of the package underside

Electrical Measurements at Room Temperature

The parameters to be measured at room, high and low temperatures are scheduled in Table 5. Unless otherwise specified, the measurements shall be performed at room T_{amb} = (+22 ± 3)°C temperature

Table 5.

Parameter	Symbol	Conditions	Min Value	Max value	Units
Input Offset Voltage	V_{IO}	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V; V_{CM} = 15 V	- 0.5	0.5	mV
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V; V_{CM} = 15 V	- 0.5	0.5	mV
		$+V_{CC}$ = 20 V, $-V_{CC}$ = -20 V; V_{CM} = 0 V	- 0.5	0.5	mV
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V	- 0.5	0.5	mV
Input Offset Current	I_{IO}	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V; V_{CM} = 15 V ; R_S = 5 MΩ	-0.2	0.2	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V; V_{CM} = 15 V ; R_S = 5 MΩ	-0.2	0.2	nA
		R_S = 5 MΩ	-0.2	0.2	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V	-0.2	0.2	nA
Input Bias Current	$\pm I_{IB}$	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V; V_{CM} = 15 V	- 0.1	2.0	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V; V_{CM} = 15 V	- 0.1	2.0	nA
		$+V_{CC}$ = 20 V, $-V_{CC}$ = -20 V; V_{CM} = 0 V	- 0.1	2.0	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V	- 0.1	2.0	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC}$ = 10 V ; $-V_{CC}$ = -20 V ; R_S = 50 Ω	-16	16	µV/V
	-PSRR	$+V_{CC}$ = 20 V ; $-V_{CC}$ = -10 V ; R_S = 50 Ω	-16	16	µV/V
Input Voltage Common Mode Rejection	CMR	V_{CM} = ± 15 V	96		dB
Output Short-Circuit Current (for positive output)	$I_{OS(+)}$	$\pm V_{CC}$ = ±15 V; t ≤ 25 ms	-20.0		mA
Output Short-Circuit Current (for negative output)	$I_{OS(-)}$	$\pm V_{CC}$ = ±15 V; t ≤ 25 ms		20.0	mA
Supply Current	I_{CC}	$\pm V_{CC}$ = ±15 V		0.6	mA
Output Voltage Swing (maximum)	$+V_{OP}$	R_L = 10 kΩ	-16.0		V
	$-V_{OP}$	R_L = 10 kΩ		16.0	V

Open Loop Voltage Gain (single ended)	AVS(+)	$\pm V_{CC}$ = ±20 V ; R_L = 10 kΩ ; V_{OUT} = +15V	80		V/mV
	AVS(-)	$\pm V_{CC}$ = ±20 V ; R_L = 10 kΩ ; V_{OUT} = -15 V	80		V/mV
Open Loop Voltage Gain (single ended)	AVS	$\pm V_{CC}$ = ±5 V ; R_L = 10 kΩ ; V_{OUT} = ±2 V	20		V/mV
Transient Response Rise Time	$TR_{(tr)}$	R_L = 10 kΩ ; C_L = 100 pF ; f < 1 kHz ; V_{IN} = +50 mV		1000	ns
Transient Response Overshoot	$TR_{(OS)}$	R_L = 10 kΩ ; C_L = 100 pF ; f < 1 kHz ; V_{IN} = +50 mV		1000	ns
Slew Rate	SR(+)	V_{IN} = +5 V to -5 V ; A_V = 1	0.05		V/µs
	SR(-)	V_{IN} = +5 V to -5 V ; A_V = 1	0.05		V/µs
Noise (referred to input) broadband	$NI_{(BB)}$	Bandwidth = 10 Hz to 5 kHz ; R_S = 0 Ω		15	µV rms
Noise (referred to input) popcorn	$NI_{(PC)}$	Bandwidth = 10 Hz to 5 kHz ; R_S = 100 kΩ		40	µV pk

Electrical Measurements at High and Low Temperature

The parameters to be measured at high and low temperatures are scheduled in Table 5a and Table 5b respectively. The measurements shall be performed at

$T_{amb} = +125\,^{+0}_{-3}$ °C and $T_{amb} = -60\,^{+3}_{-0}$ °C respectively.

Electrical Measurement at High Temperature – Tamb = +125°C

Table 5a.

Parameter	Symbol	Conditions	Min Value	Max value	Units
Input Offset Voltage	V_{IO}	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V; V_{CM} = 15 V	- 1.0	1.0	mV
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V; V_{CM} = 15 V	- 1.0	1.0	mV
		$+V_{CC}$ = 20 V, $-V_{CC}$ = -20 V; V_{CM} = 0 V	- 1.0	1.0	mV
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V	- 1.0	1.0	mV
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}/\Delta T$		-5.0	5.0	µV/°C
Input Offset Current	I_{IO}	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V; V_{CM} = 15 V ; R_S = 5 MΩ	-0.4	0.4	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V; V_{CM} = 15 V ;	-0.4	0.4	nA

		R_S = 5 MΩ			
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V	-0.4	0.4	nA
Input Offset Current Temperature Sensitivity	$\Delta I_{IO}/\Delta T$		-2.5	2.5	pA/°C
Input Bias Current	$\pm I_{IB}$	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V; V_{CM} = 15 V	- 1.0	2.0	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V; V_{CM} = 15 V	- 1.0	2.0	nA
		$+V_{CC}$ = 20 V, $-V_{CC}$ = -20 V; V_{CM} = 0 V	- 1.0	2.0	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V	- 1.0	2.0	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC}$ = 10 V ; $-V_{CC}$ = -20 V ; R_S = 50 Ω	-16	16	µV/V
	-PSRR	$+V_{CC}$ = 20 V ; $-V_{CC}$ = -10 V ; R_S = 50 Ω	-16	16	µV/V
Input Voltage Common Mode Rejection	CMR	V_{CM} = ± 15 V	96		dB
Output Short-Circuit Current (for positive output)	$I_{OS(+)}$	$\pm V_{CC}$ = ±15 V; t ≤ 25 ms	-20.0		mA
Output Short-Circuit Current (for negative output)	$I_{OS(-)}$	$\pm V_{CC}$ = ±15 V; t ≤ 25 ms		20.0	mA
Supply Current	I_{CC}	$\pm V_{CC}$ = ±15 V		0.6	mA
Output Voltage Swing (maximum)	$+V_{OP}$	R_L = 10 kΩ	-16.0		V
	$-V_{OP}$	R_L = 10 kΩ		16.0	V
Open Loop Voltage Gain (single ended)	AVS(+)	$\pm V_{CC}$ = ±20 V ; R_L = 10 kΩ ; V_{OUT} = +15V	40		V/mV
	AVS(-)	$\pm V_{CC}$ = ±20 V ; R_L = 10 kΩ ; V_{OUT} = -15 V	40		V/mV
Open Loop Voltage Gain (single ended)	AVS	$\pm V_{CC}$ = ±5 V ; R_L = 10 kΩ ; V_{OUT} = ±2 V	20		V/mV
Transient Response Rise Time	$TR_{(tr)}$	R_L = 10 kΩ ; C_L = 100 pF ; f < 1 kHz ; V_{IN} = +50 mV		1000	ns
Transient Response Overshoot	$TR_{(os)}$	R_L = 10 kΩ ; C_L = 100 pF ; f < 1 kHz ; V_{IN} = +50 mV		1000	ns
Slew Rate	SR(+)	V_{IN} = +5 V to -5 V ; A_V = 1	0.05		V/µs
	SR(-)	V_{IN} = +5 V to -5 V ; A_V = 1	0.05		V/µs

Electrical Measurement at Low Temperature – Tamb = -60°C

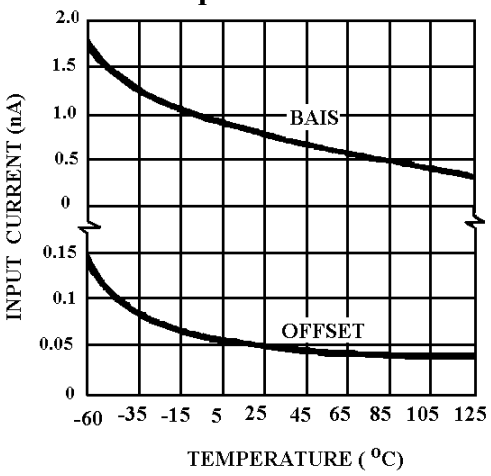
Table 5b.

Parameter	Symbol	Conditions	Min Value	Max value	Units
Input Offset Voltage	V_{IO}	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V; V_{CM} = 15 V	- 1.0	1.0	mV
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V; V_{CM} = 15 V	- 1.0	1.0	mV
		$+V_{CC}$ = 20 V, $-V_{CC}$ = -20 V; V_{CM} = 0 V	- 1.0	1.0	mV
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V	- 1.0	1.0	mV
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}/\Delta T$		-5.0	5.0	µV/°C
Input Offset Current	I_{IO}	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V; V_{CM} = 15 V ; R_S = 5 MΩ	-0.4	0.4	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V; V_{CM} = 15 V ; R_S = 5 MΩ	-0.4	0.4	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V	-0.4	0.4	nA
Input Offset Current Temperature Sensitivity	$\Delta I_{IO}/\Delta T$		-2.5	2.5	pA/°C
Input Bias Current	$\pm I_{IB}$	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V; V_{CM} = 15 V	- 0.1	3.0	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V; V_{CM} = 15 V	- 0.1	3.0	nA
		$+V_{CC}$ = 20 V, $-V_{CC}$ = -20 V; V_{CM} = 0 V	- 0.1	3.0	nA
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V	- 0.1	3.0	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC}$ = 10 V ; $-V_{CC}$ = -20 V ; R_S = 50 Ω	-16	16	µV/V
	-PSRR	$+V_{CC}$ = 20 V ; $-V_{CC}$ = -10 V ; R_S = 50 Ω	-16	16	µV/V
Input Voltage Common Mode Rejection	CMR	V_{CM} = ± 15 V	96		dB
Output Short-Circuit Current (for positive output)	$I_{OS}(+)$	$\pm V_{CC}$ = ±15 V; t ≤ 25 ms	-20.0		mA
Output Short-Circuit Current (for negative output)	$I_{OS}(-)$	$\pm V_{CC}$ = ±15 V; t ≤ 25 ms		20.0	mA
Supply Current	I_{CC}	$\pm V_{CC}$ = ±15 V		0.8	mA

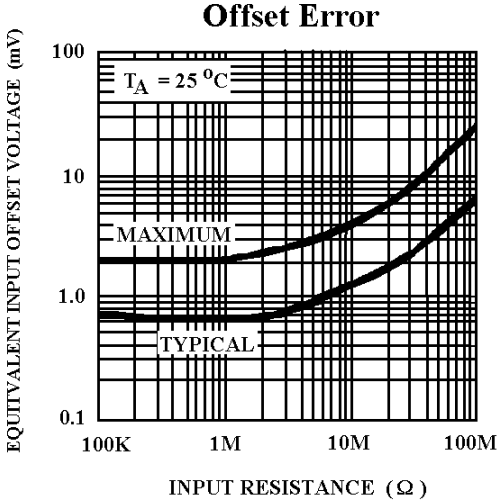
Output Voltage Swing (maximum)	$+V_{OP}$	R_L = 10 kΩ	-16.0		V
	$-V_{OP}$	R_L = 10 kΩ		16.0	V
Open Loop Voltage Gain (single ended)	AVS(+)	$\pm V_{CC}$ = ±20 V ; R_L = 10 kΩ ; V_{OUT} = +15V	40		V/mV
	AVS(-)	$\pm V_{CC}$ = ±20 V ; R_L = 10 kΩ ; V_{OUT} = -15 V	40		V/mV
Open Loop Voltage Gain (single ended)	AVS	$\pm V_{CC}$ = ±5 V ; R_L = 10 kΩ ; V_{OUT} = ±2 V	20		V/mV
Transient Response Rise Time	TR(tr)	R_L = 10 kΩ ; C_L = 100 pF ; f < 1 kHz ; V_{IN} = +50 mV		1000	ns
Transient Response Overshoot	TR(OS)	R_L = 10 kΩ ; C_L = 100 pF ; f < 1 kHz ; V_{IN} = +50 mV		1000	ns
Slew Rate	SR(+)	VI_N = +5 V to -5 V ; A_V = 1	0.05		V/µs
	SR(-)	V_{IN} = +5 V to -5 V ; A_V = 1	0.05		V/µs

Typical Performance Characteristics

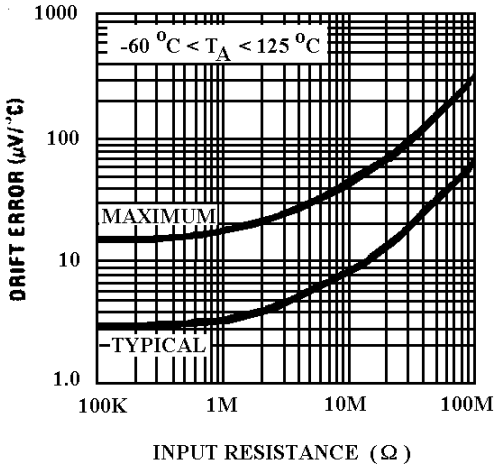
Input Current



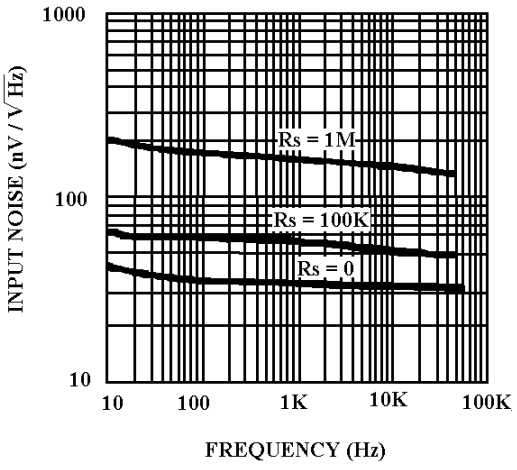
Offset Error



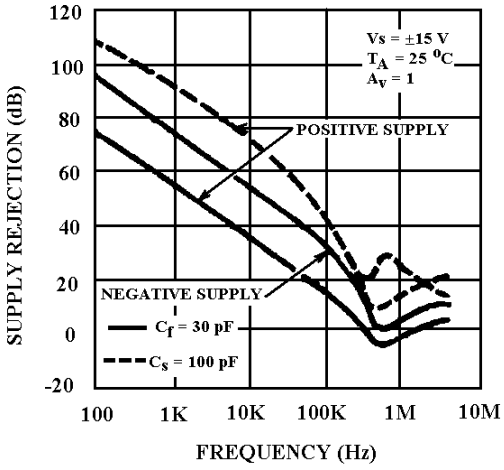
Driff Error



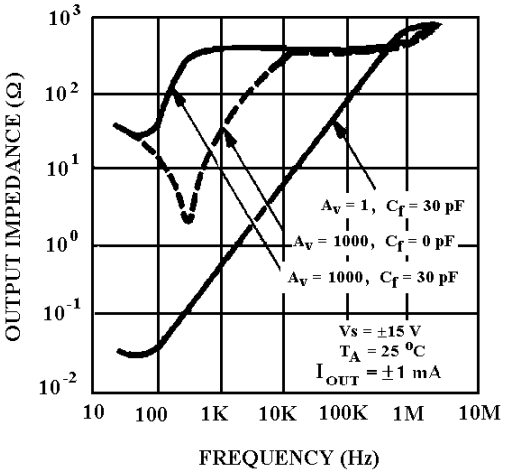
Input Noise Voltage



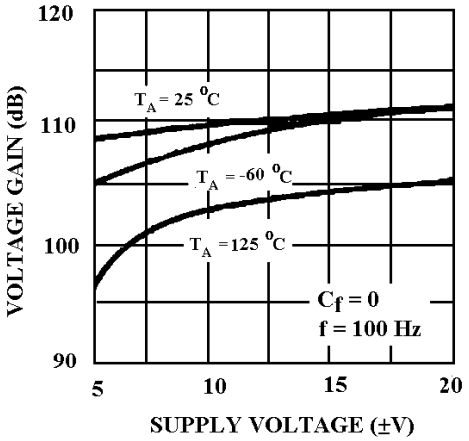
Power Supply Rejection



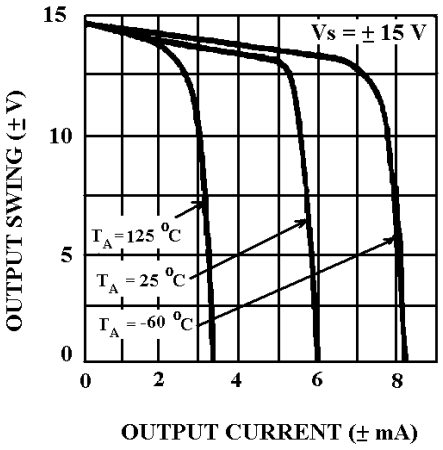
Closed Loop Output Impedance



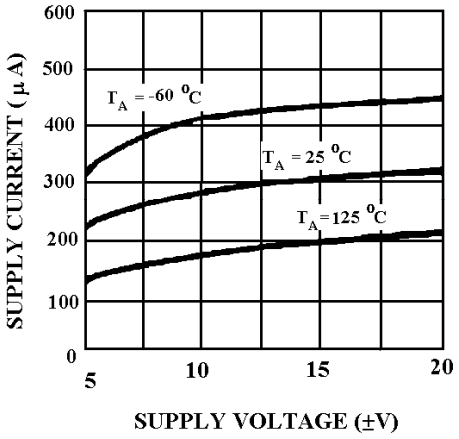
Voltage Gain



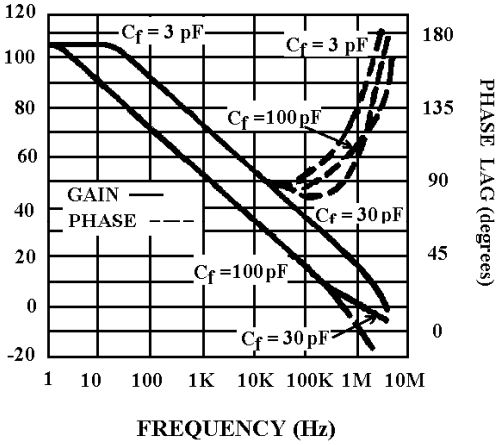
Output Swing



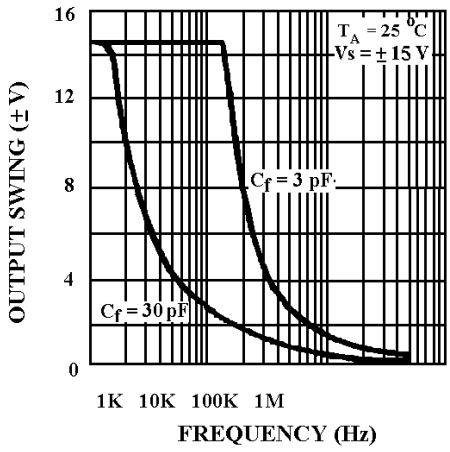
Supply Current



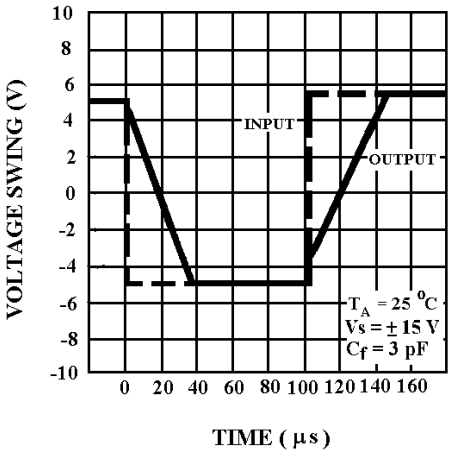
Open Loop Frequency Response



Large Signal Frequency Response

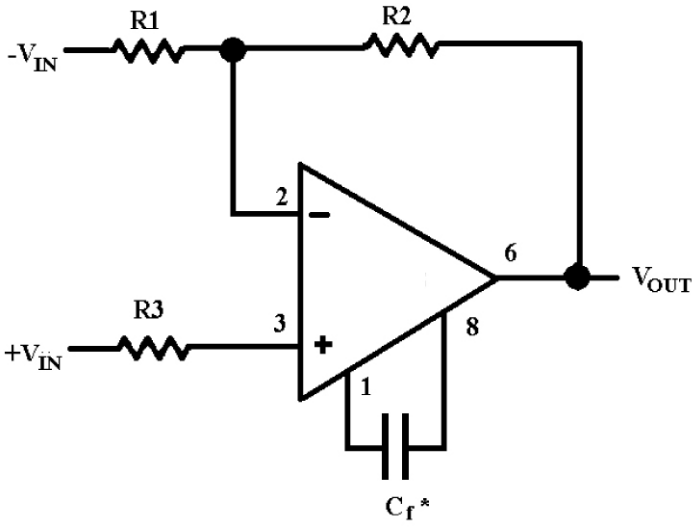


Voltage Follower Pulse Response



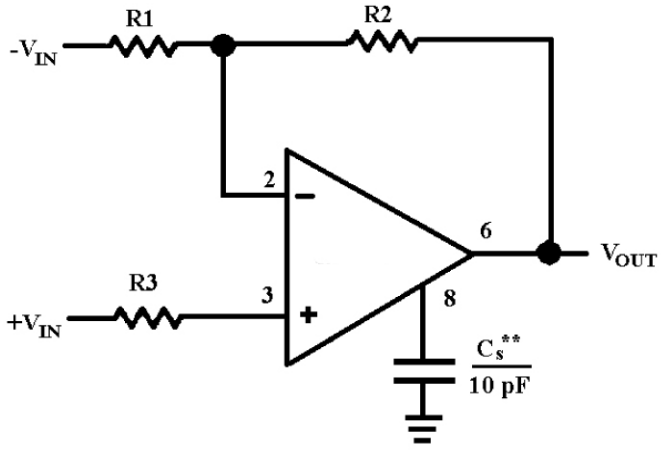
Typical Applications

Standard Compensation Circuit



**Bandwidth and slew rate are proportional to $1/C_f$.

Alternate Frequency Compensation

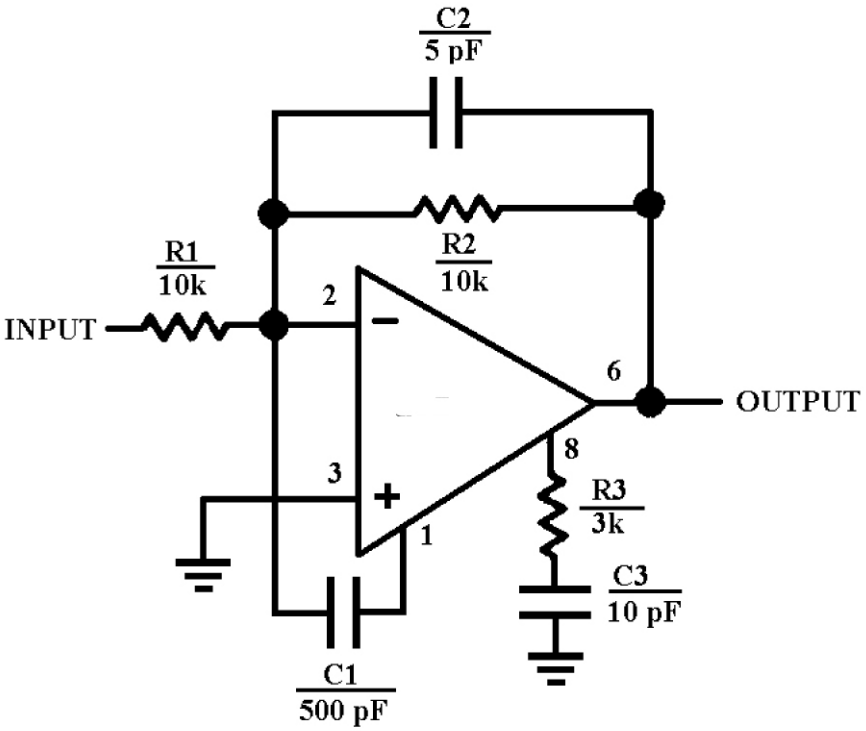


**Bandwidth and slew rate are proportional to $1/C_S$.

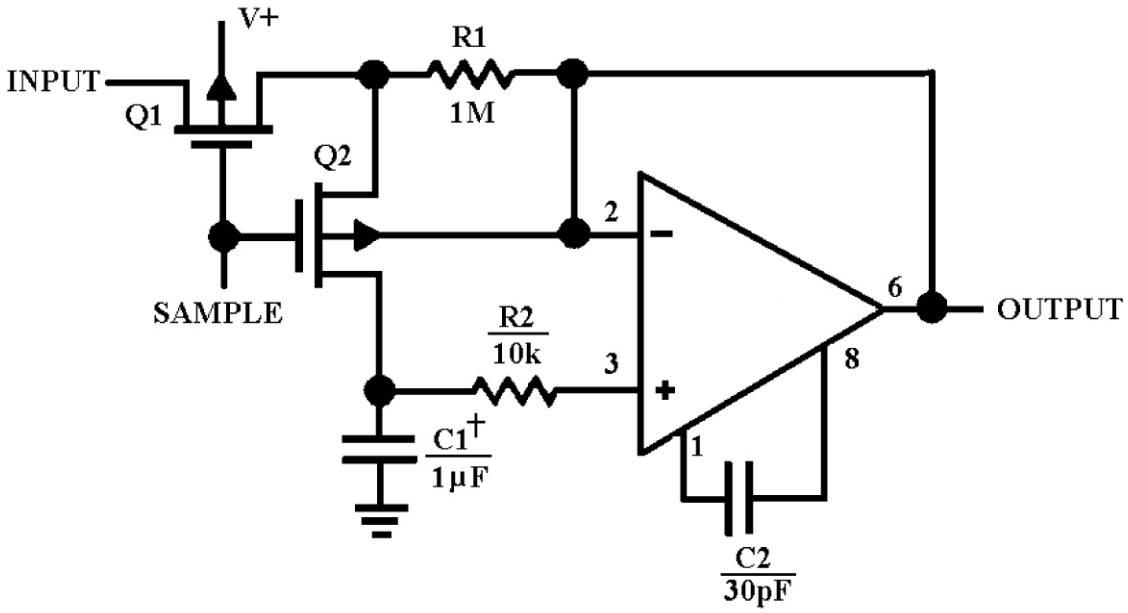
$$C_f = \frac{R1 * C_0}{R1+R2} \quad ; \quad C_0 = 30pF$$

Note: Improves rejection of power supply noise by a factor of ten.

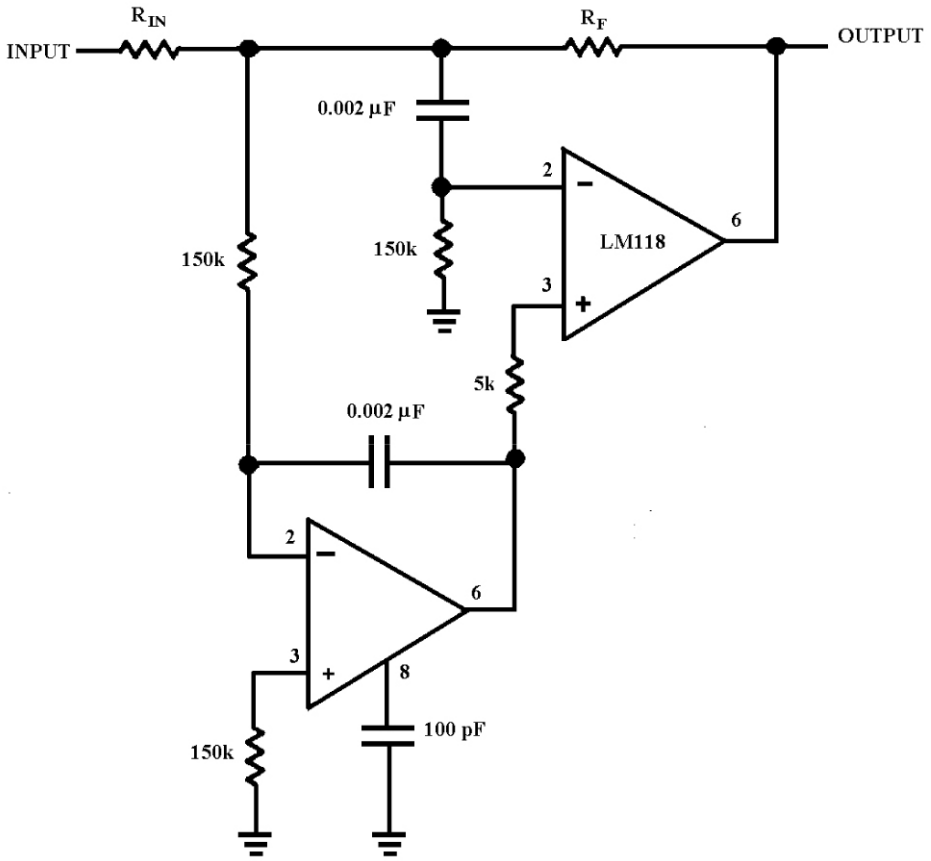
Feedforward Compensation



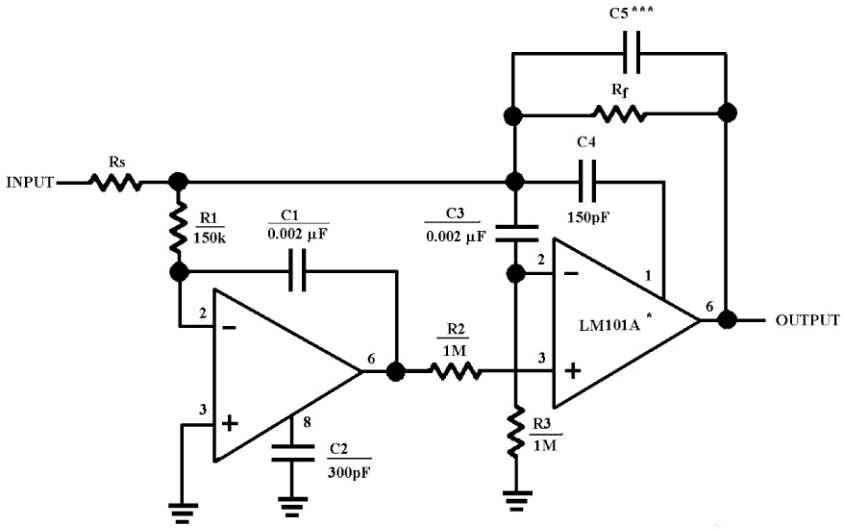
Sample and Hold



High Speed Amplifier with Low Drift and Low Input Current



Fast + Summing Amplifier

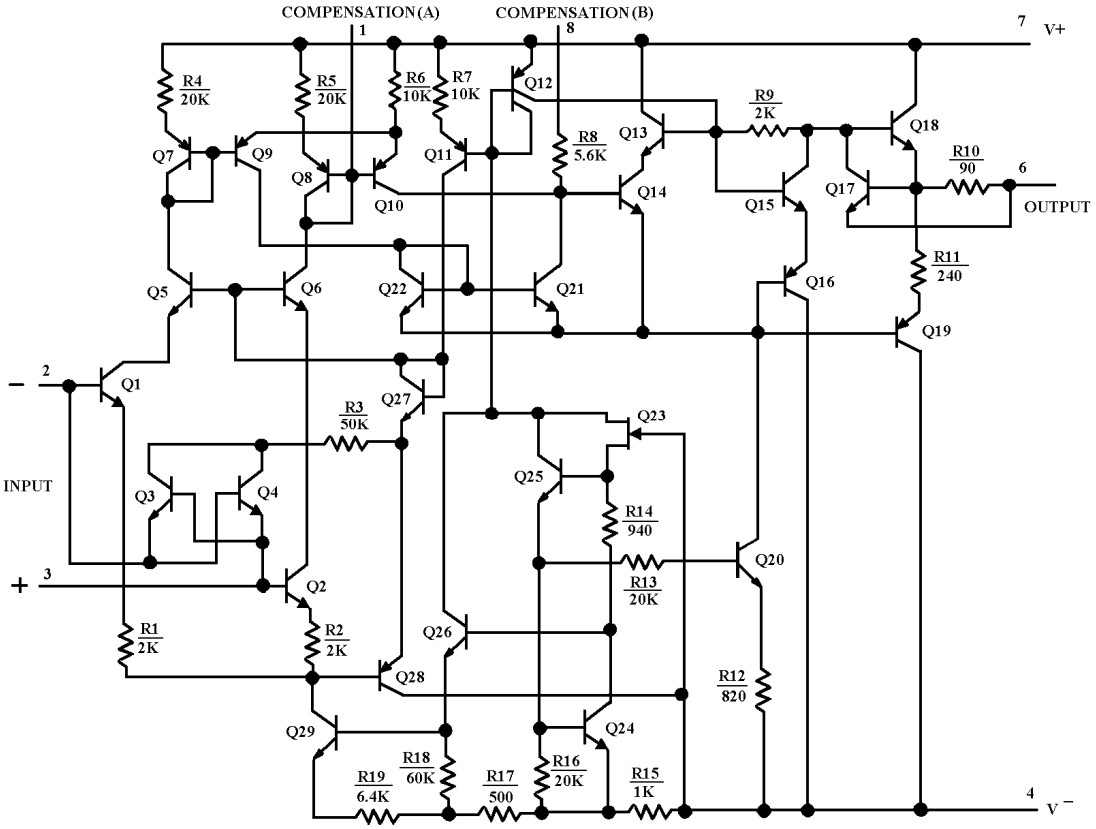


*In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

**Power Bandwidth: 250 KHz .Small Signal Bandwidth: 3.5 MHz. Slew Rate: 10V/mS.

*** $C5 = \frac{6*10^{-8}}{Rf}$

Schematic Diagram

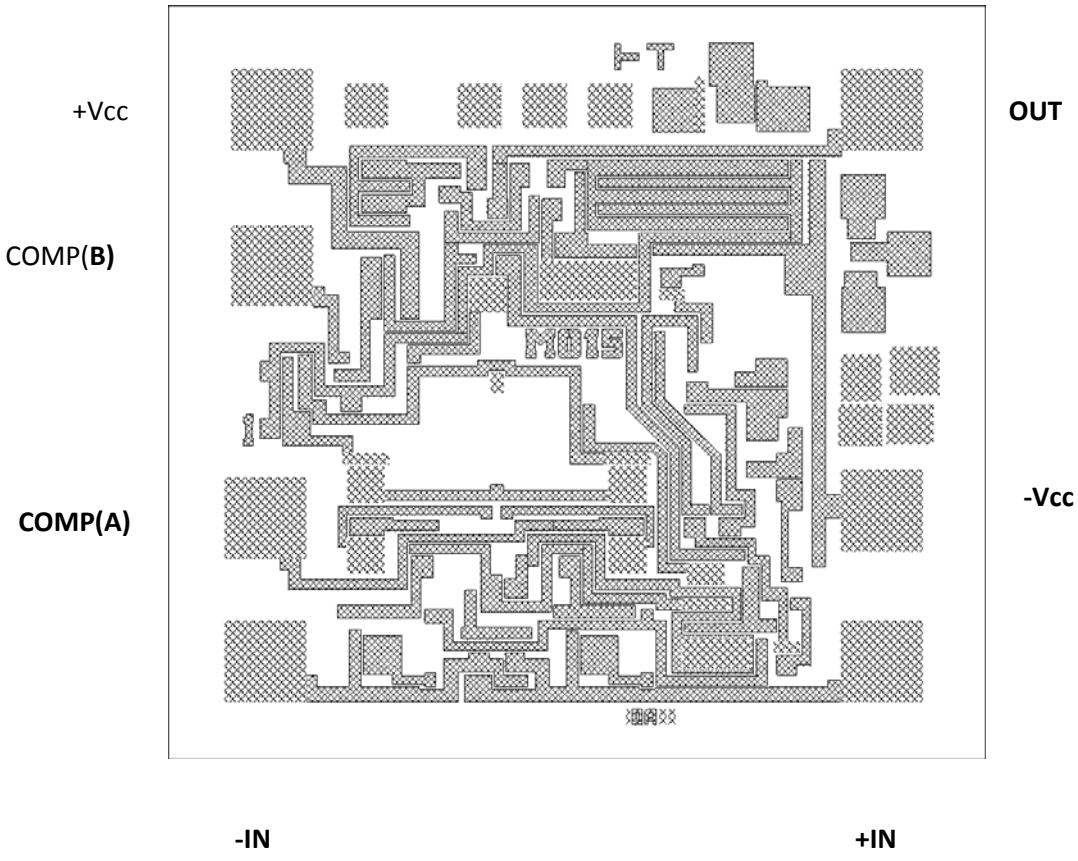


Die Characteristics

Die dimensions:
1.3x1.2 ± 0.1 mm,
51x47 ± 4 mils.
Wafer thickness 0.46± 0.02 mm,
18 ± 1 mils.
Metallisation
type: Al, 1% Si,thickness: 1.4 ± 0.1 µm
Glassivation: phosphosilicate glass (PSG),
thickness 1.2 ± 0.2 µm.

Worst case current density:
$8 \cdot 10^4$ A/cm^2.
Substrate potential(Powered Up):
Unbiased.
Transistor count:
29.
Process:
Bipolar epitaxial + FET.

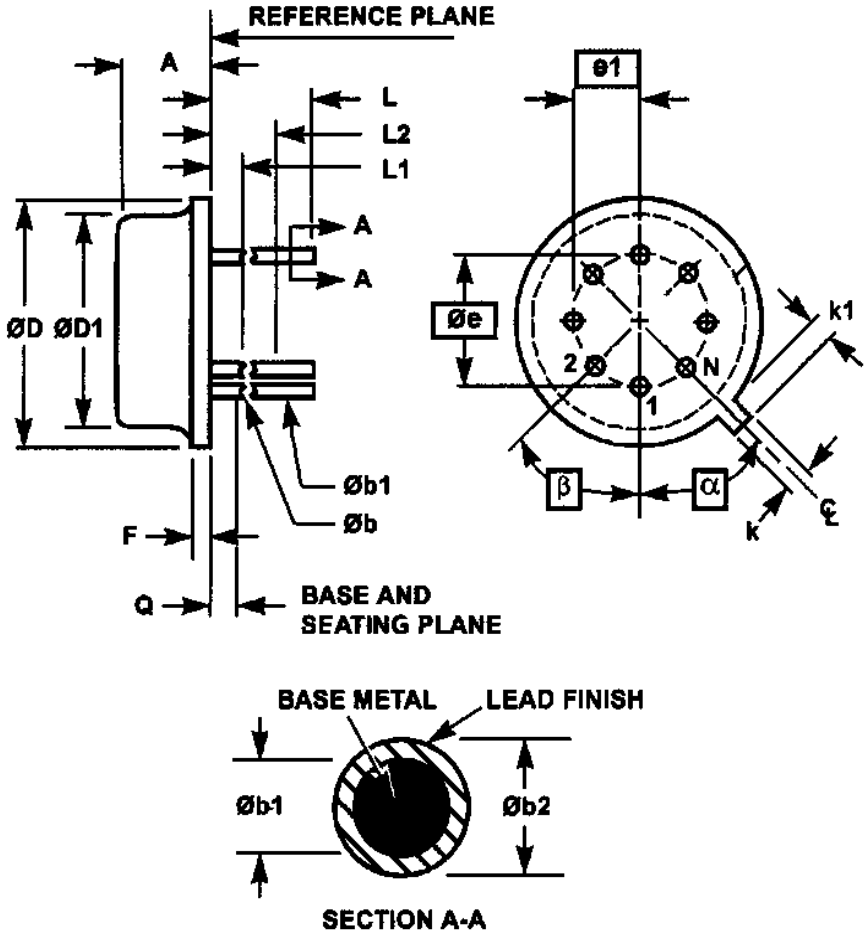
Metallisation Mask Layout



Physical Dimensions

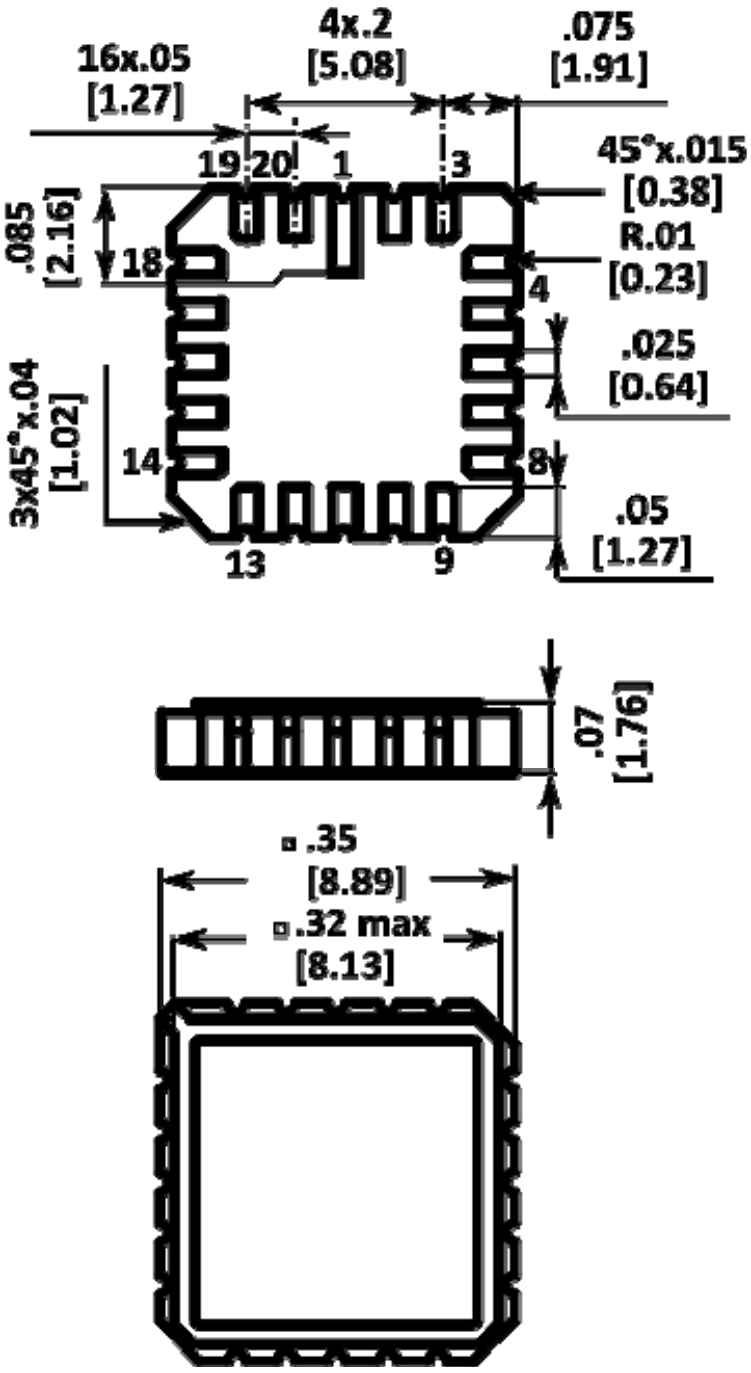
All dimensions are in inches and [millimeters]. In case of conflict between English and metric dimension, the inch dimensions control.

Metal Can Package TO-5

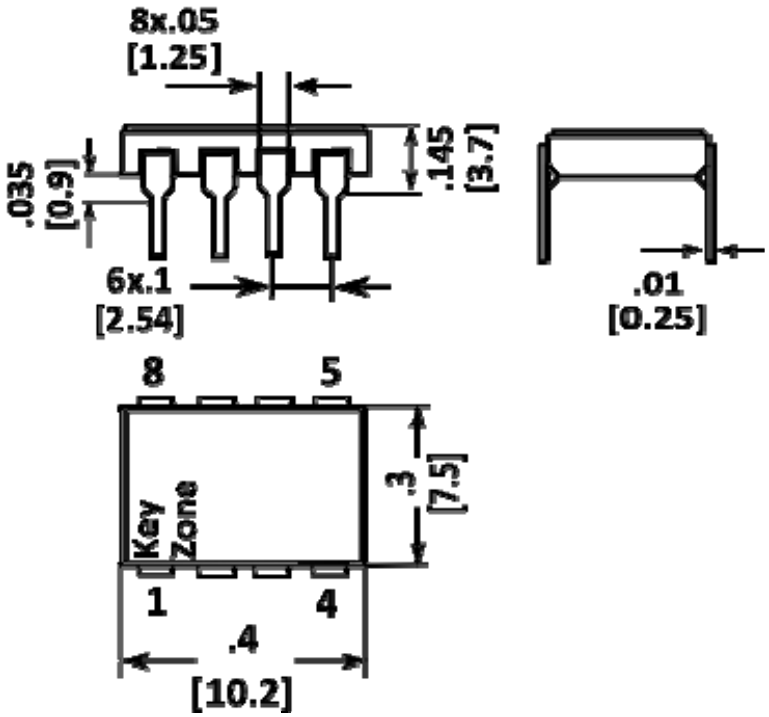


Symbol	Millimeters		Inches		Note
	MIN	MAX	MIN	MAX	
A	6.00	6.22	0.236	0.244	-
Øb	0.41	0.48	0.016	0.019	13
Øb1	0.41	0.53	0.016	0.021	13
Øb2	0.41	0.61	0.016	0.024	-
ØD	9.09	9.19	0.335	0.375	-
ØD1	8.23	8.43	0.305	0.335	-
Øe	0.200		5.08		-
e1	0.100		2.54		-
F	0.33	0.43	0.013	0.017	-
k	0.69	0.86	0.027	0.034	-
k1	0.69	1.14	0.027	0.045	14
L	13.0	14.0	0.512	0.552	13
L1	-	1.27	-	0.05	13
L2	6.35	6.85	0.250	0.270	13
Q	0.5	-	0.02	-	-
α	45°		45°		15
β	45°		45°		15
N	8		8		16

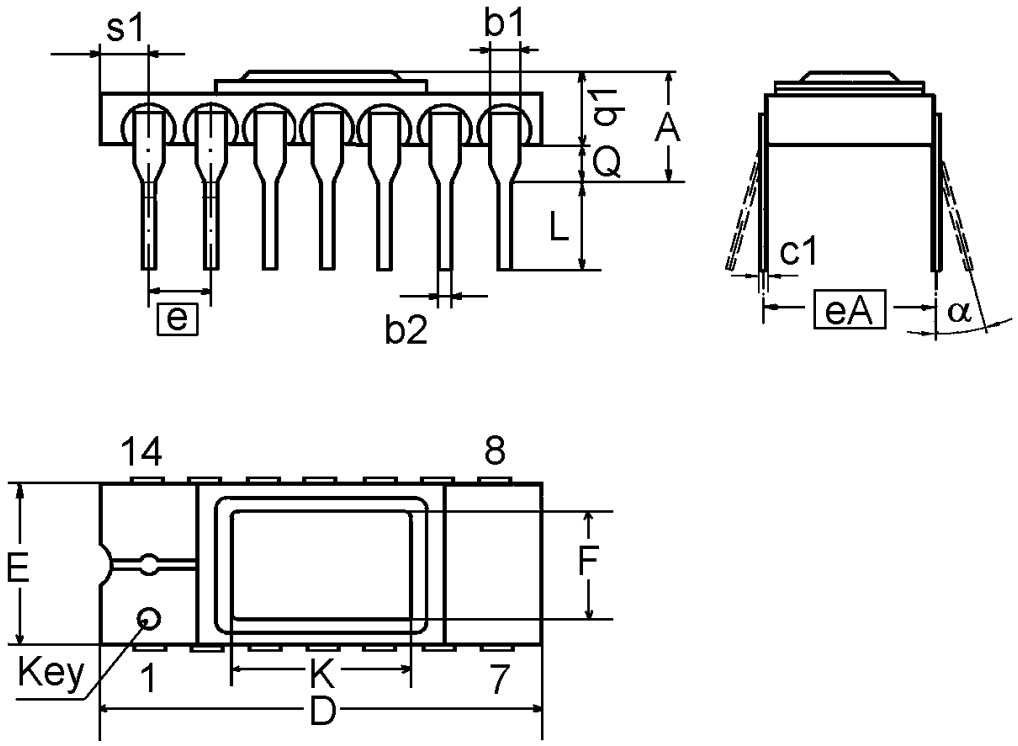
Ceramic leadless package CLCC



Ceramic dual-in-line package(8pin)



Ceramic dual-in-line package (14pin)



Symbol	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	-	0,20	-	5
b1	0,04	0,06	1.03	1.53
b2	0,016	0,027	0.41	0.69
c1	0,009	0,015	0.22	0.38
D	0,739	0,773	18.77	19.63
E	0,279	0,296	7.08	7.53
e	0,098		2.5	
eA	0,295		7.5	
F	0,178	0,192	4.52	4.88
K	0,295	0,304	7.5	7.72
L	-	0,153	-	3.88
Q	0,126	0,173	3.2	4.4
q1	0,024	0,071	0.6	1.8
s1	-	0,089	-	2.25
α	0	15 °	0	15 °

Revision History

Rev	Date	Description
A	06/02/14	Original

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