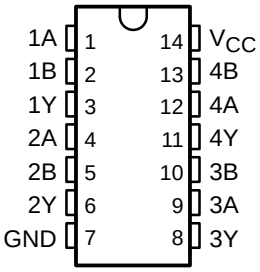
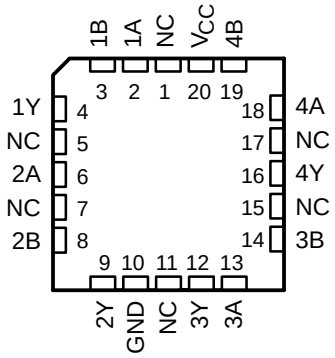
- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 8 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

SN54HC00 . . . J OR W PACKAGE
SN74HC00 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The ’HC00 devices contain four independent 2-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74HC00N	SN74HC00N
	SOIC – D	Tube	SN74HC00D	HC00
		Tape and reel	SN74HC00DR	
	SOP – NS	Tape and reel	SN74HC00NSR	HC00
	SSOP – DB	Tape and reel	SN74HC00DBR	HC00
	TSSOP – PW	Tube	SN74HC00PW	HC00
		Tape and reel	SN74HC00PWR	
–55°C to 125°C	CDIP – J	Tube	SNJ54HC00J	SNJ54HC00J
	CFP – W	Tube	SNJ54HC00W	SNJ54HC00W
	LCCC – FK	Tube	SNJ54HC00FK	SNJ54HC00FK

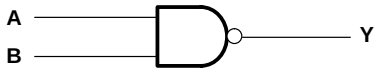
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HC00			SN74HC00			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC00		SN74HC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±100		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

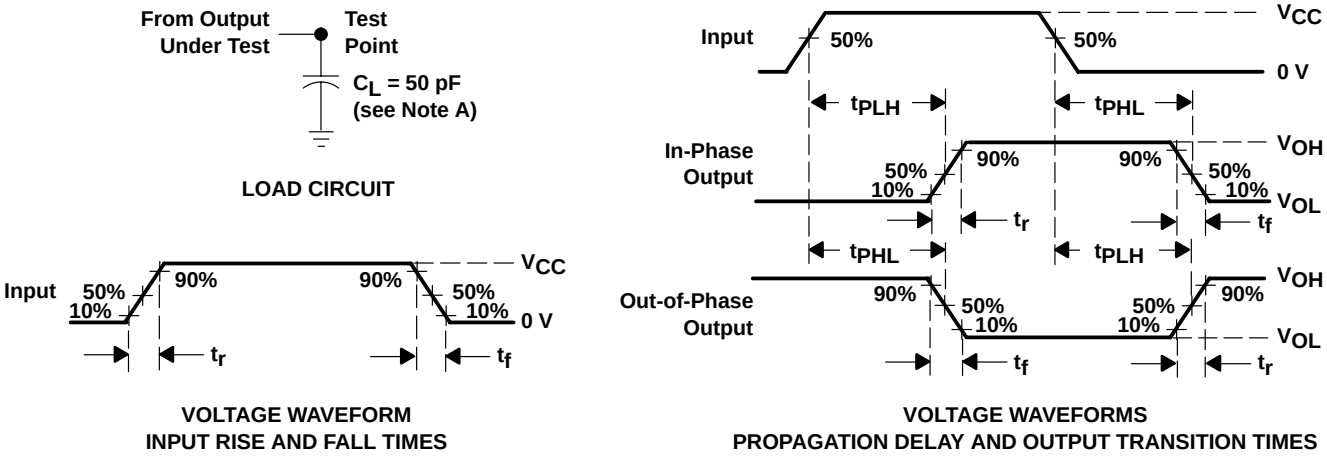
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC00		SN74HC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



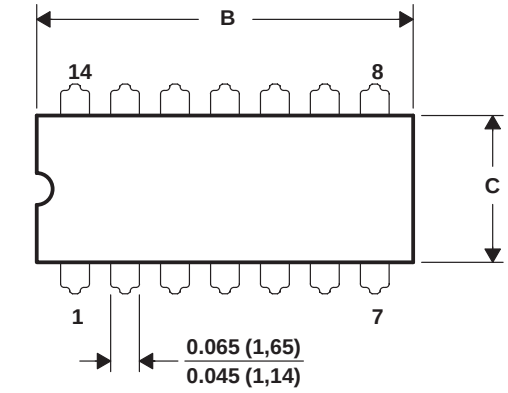
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

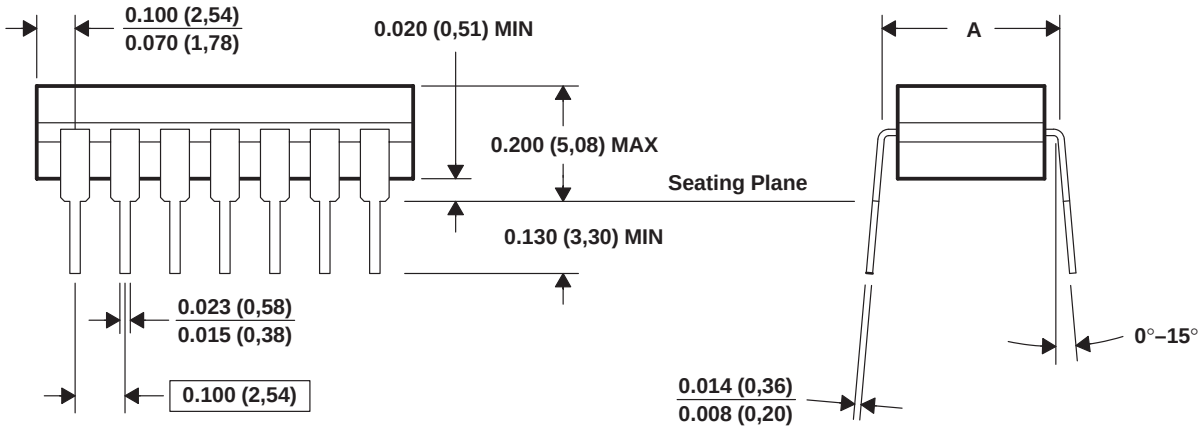
MCER002C – JANUARY 1995 – REVISED JUNE 1999

J (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

14 LEADS SHOWN



DIM \ PINS **	14	16	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)

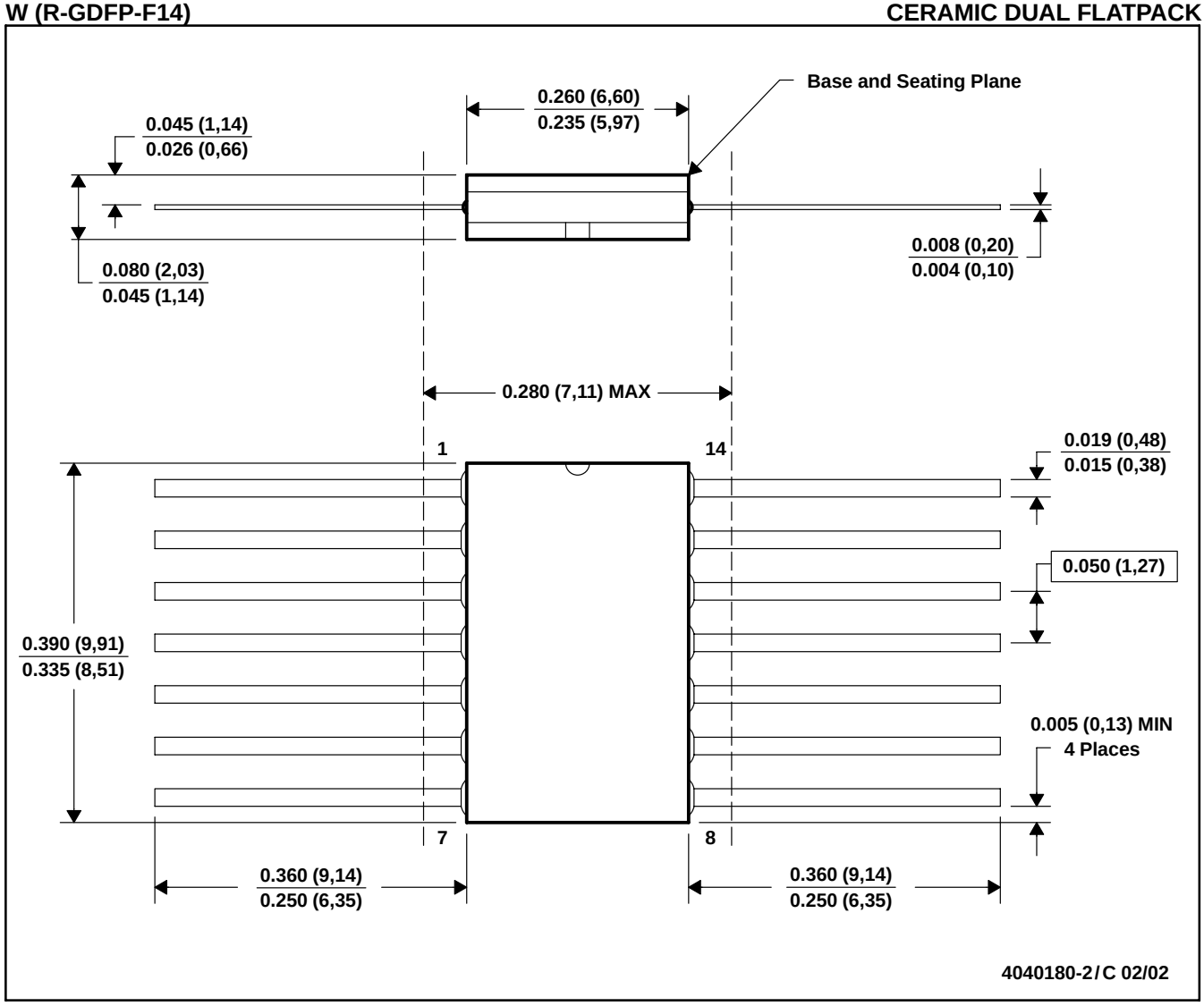


4040083/E 03/99

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, and GDIP1-T20

MCFP002A – JANUARY 1995 – REVISED FEBRUARY 2002

W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**

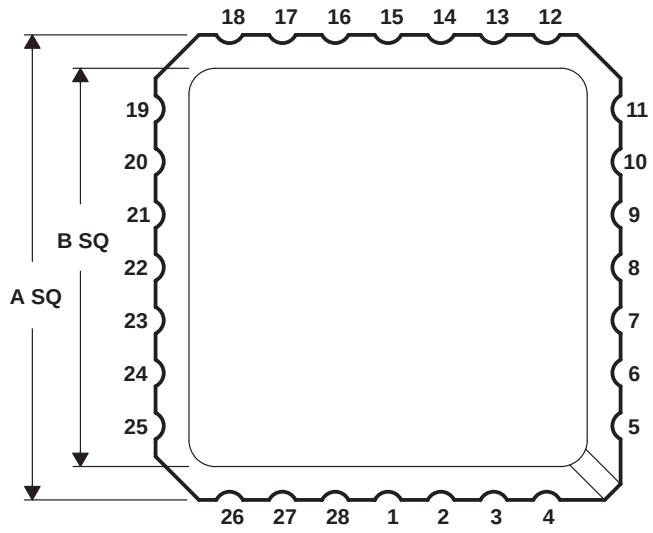


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

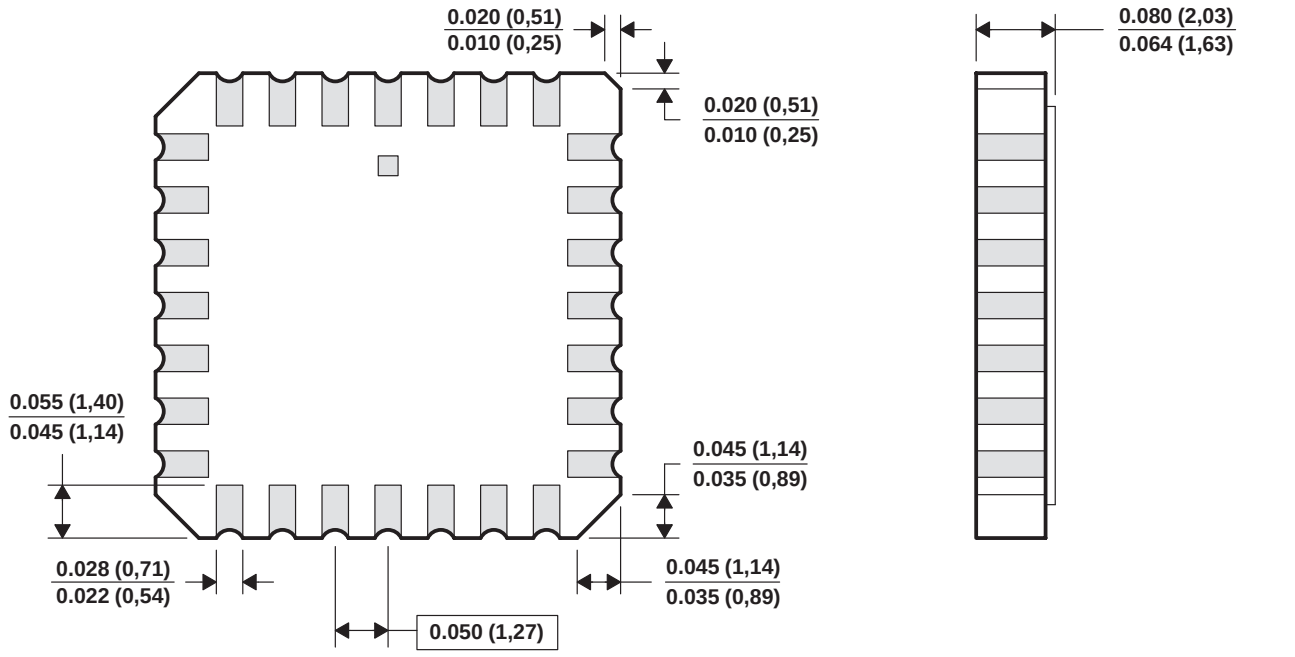
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



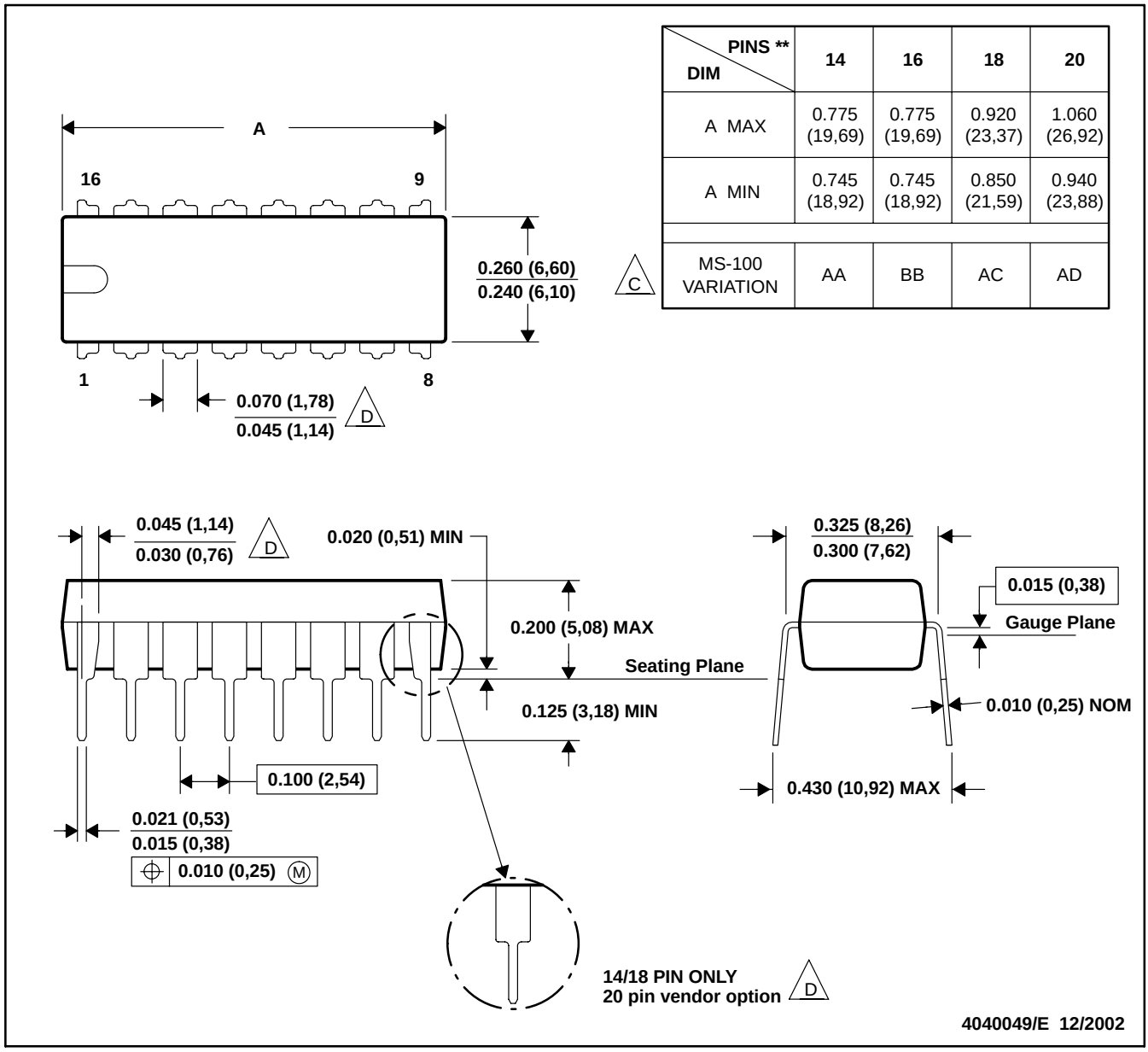
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

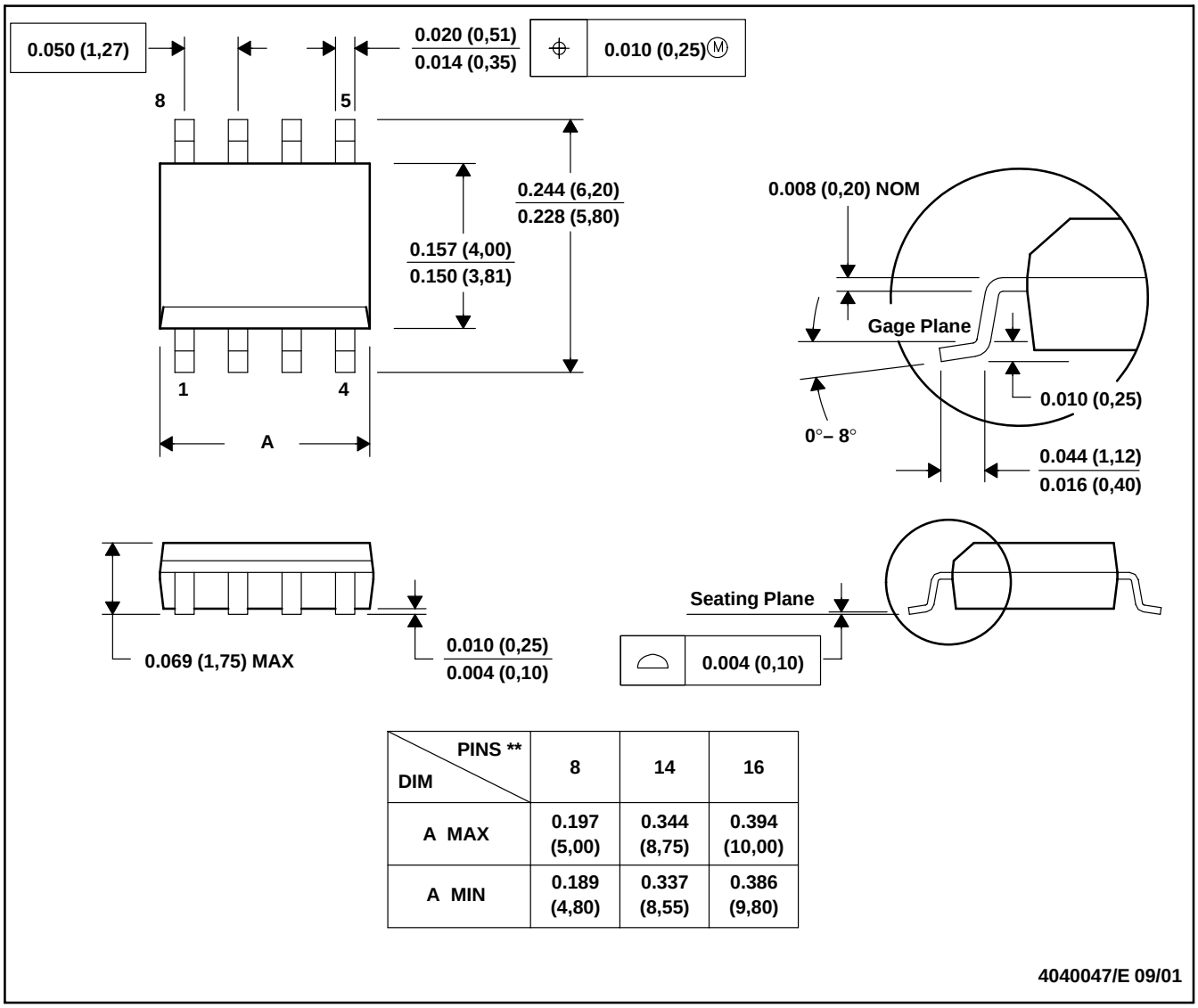
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



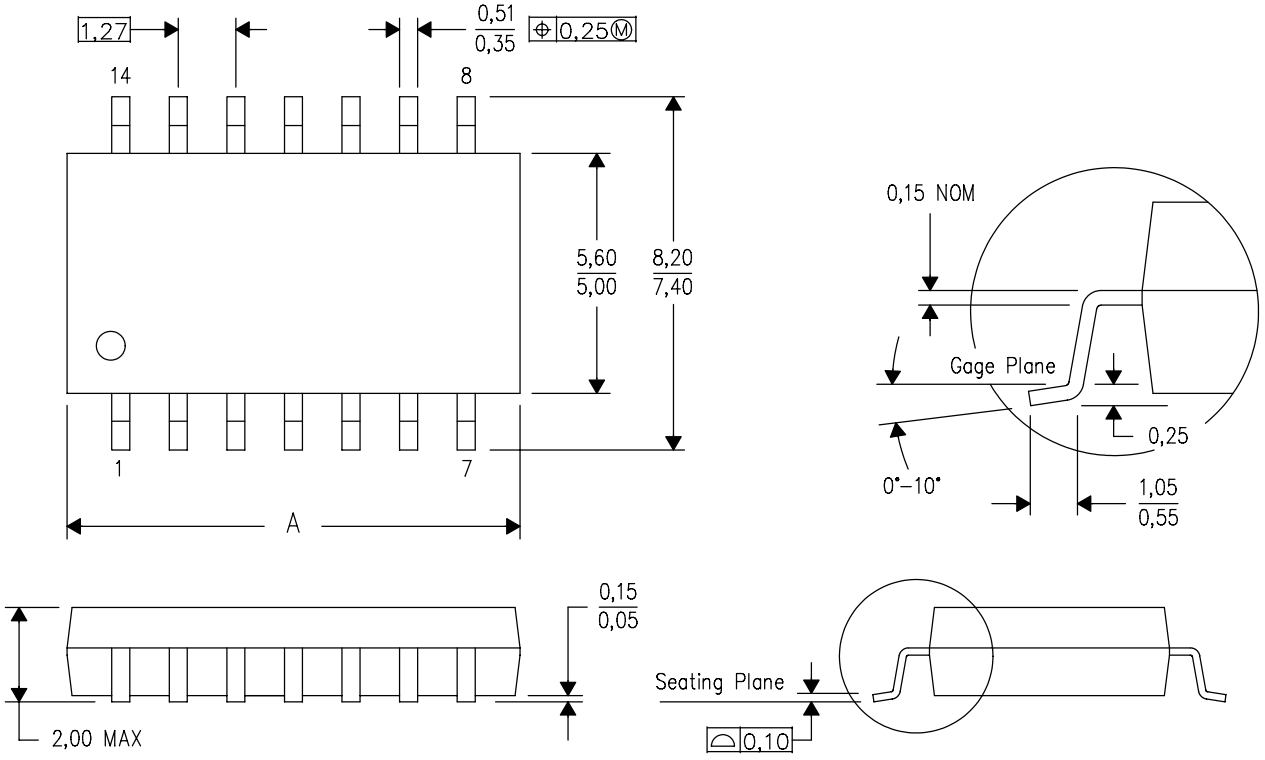
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

NS (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

14–PIN SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

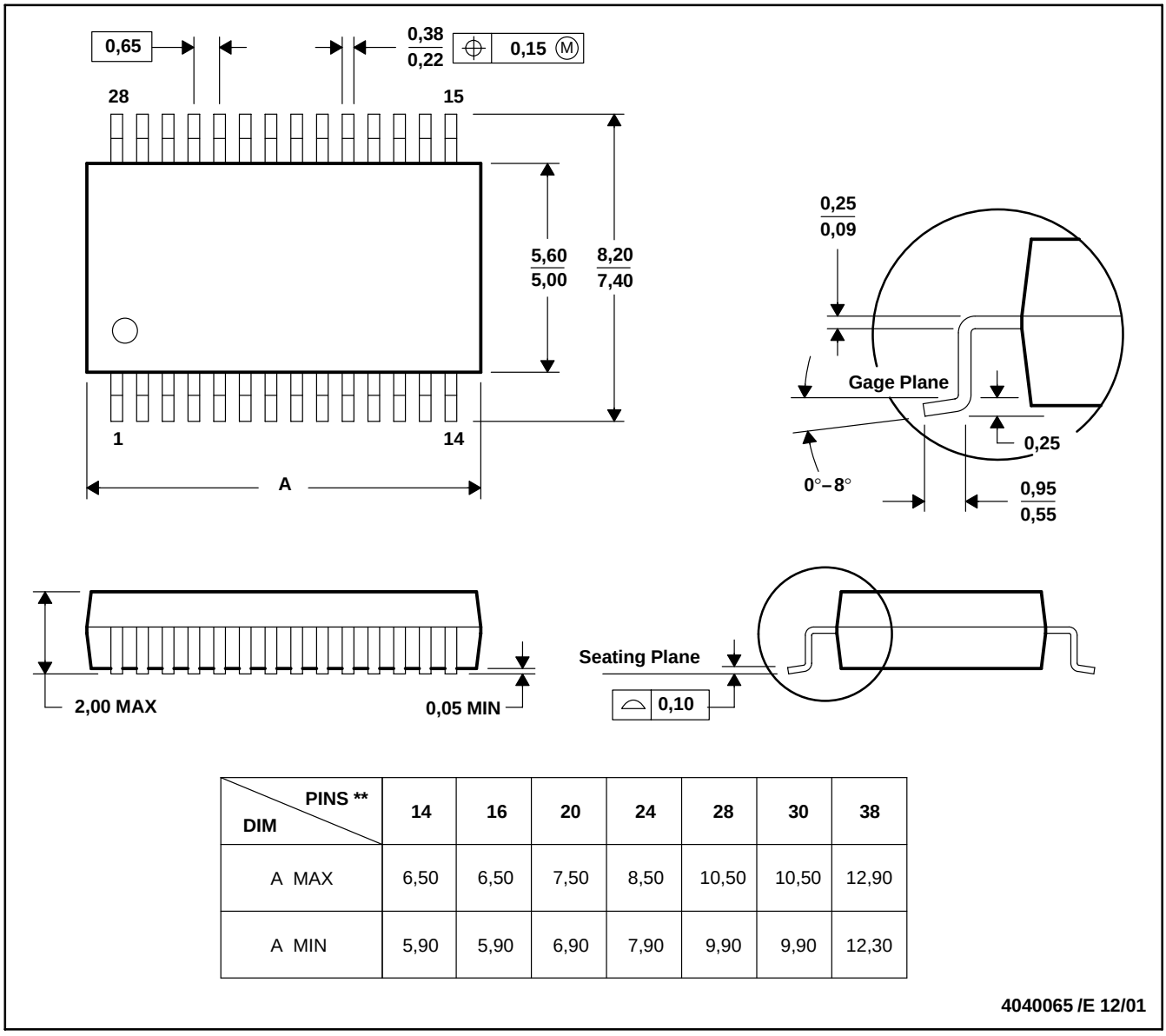
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



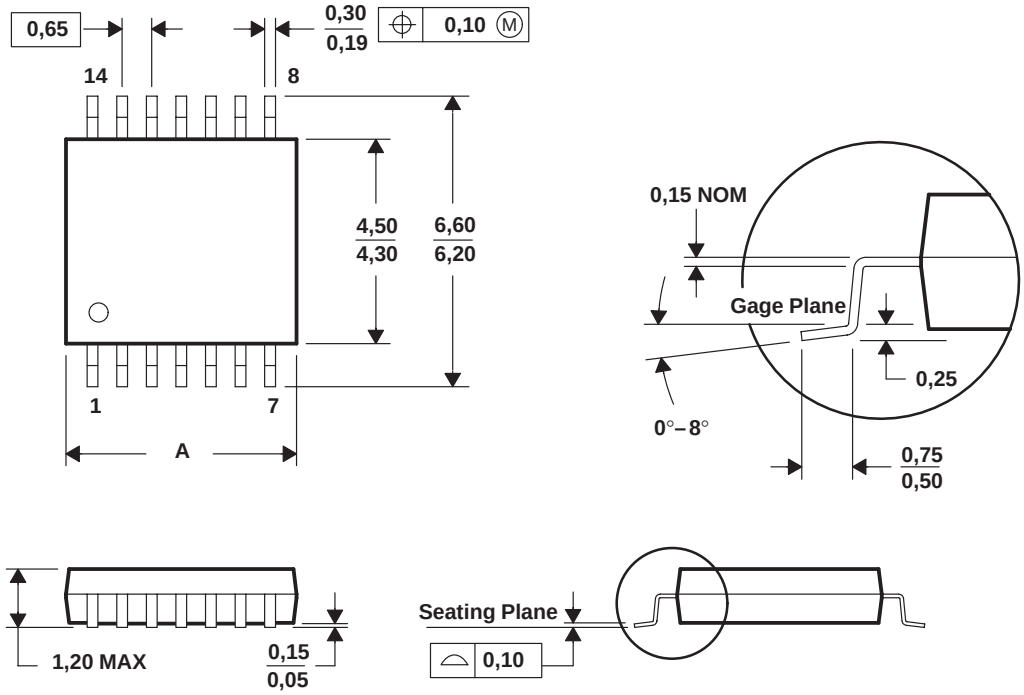
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

SN74HC00, Quad 2-Input Positive-NAND Gates
DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54HC00	SN74HC00
Voltage Nodes (V)	6, 5, 2	6, 5, 2
Vcc range (V)	2.0 to 6.0	2.0 to 6.0
Input Level	CMOS	CMOS
Output Level	CMOS	CMOS
Output Drive (mA)		-4/4
No. of Gates	4	4
Static Current		0.02
tpd max (ns)		20

FEATURES

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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20-uA Max I_{CC}
- Typical t_{pd} = 8 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 uA Max

DESCRIPTION

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The 'HC00 devices contain four independent 2-input NAND gates. They perform the Boolean function Y = (A • B)\ or Y = A\ + B\ in positive logic.

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74hc00.pdf (279 KB,Rev.D) (Updated: 12/03/2002)

APPLICATION NOTES

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View Application Notes for Digital Logic

- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- SN54/74HCT CMOS Logic Family Applications and Restrictions (SCLA011 - Updated: 05/01/1996)
- Selecting the Right Texas Instruments Signal Switch (SZZA030 - Updated: 09/07/2001)

Product Folder: SN74HC00, Quad 2-Input Positive-NAND Gates

- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)
- Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)
- Signal Switch Data Book (SCDD003, 10259 KB - Updated: 03/19/2001)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74HC00D	SOIC (D)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HC00DR	SOIC (D)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HC00N	PDIP (N)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HC00NSR	SOP (NS)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HC00PWR	TSSOP (PW)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION
Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
SN74HC00ADBLE	OBSOLETE	SSOP (DB) | 14	-40 TO 85	View Contents	1KU |	
SN74HC00D	ACTIVE	SOIC (D) | 14	-40 TO 85	View Contents	1KU | 0.11	50

TI INVENTORY STATUS
As Of 09:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME
0*		Call**
0*	1953 | 30 Apr	4 WKS
	>10k | 12 May	

REPORTED DISTRIBUTOR INVENTORY
As Of 09:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
None Reported View Distributors		
Avnet | Americas	>1k	BUY NOW
Arrow | Americas	>1k	BUY NOW
EBV Electronik | Europe	>1k	BUY NOW
DigiKey | Americas	>1k	BUY NOW
Newark Electronics | Americas	>1k	BUY NOW

SN74HC00DR	ACTIVE	SOIC (D)	14	-40 TO 85	View Contents	1KU | 0.11	2500	0*	>10k | 28 Apr	2 WKS	Avnet | Americas >1k BUY NOW
											Arrow | Americas >1k BUY NOW
											EBV Electronik | Europe >1k BUY NOW
											Abacus Polar | Europe >1k BUY NOW
											DigiKey | Americas >1k BUY NOW
											Avnet-SILICA | Europe >1k BUY NOW
SN74HC00N	ACTIVE	PDIP (N)	14	-40 TO 85	View Contents	1KU | 0.11	25	0*	3 | 21 Apr	7 WKS	Avnet-SILICA | Europe >1k BUY NOW
									1100 | 28 Apr		Avnet | Americas >1k BUY NOW
									500 | 29 Apr		Arrow | Americas >1k BUY NOW
									1000 | 22 May		EBV Electronik | Europe >1k BUY NOW
									8100 | 27 May		DigiKey | Americas >1k BUY NOW
											Newark Electronics | Americas >1k BUY NOW
SN74HC00N3	OBSOLETE	PDIP (N)	14	-40 TO 85	View Contents	1KU |		0*		Call**	None Reported View Distributors
SN74HC00NS	ACTIVE	SOP (NS)	14		View Contents	1KU |		0*		Call**	None Reported View Distributors
SN74HC00NSLE	OBSOLETE	SOP (NS)	14	-40 TO 85	View Contents	1KU |		0*		Call**	None Reported View Distributors
SN74HC00NSR	ACTIVE	SOP (NS)	14	-40 TO 85	View Contents	1KU | 0.55	2000	0*	>10k | 28 Apr	2 WKS	DigiKey | Americas >1k BUY NOW
SN74HC00PW	ACTIVE	TSSOP (PW)	14	-40 TO 85	View Contents	1KU | 0.18	90	0*	450 | 16 Apr	4 WKS	Arrow | Americas 356 BUY NOW
									>10k | 08 May		
SN74HC00PWLE	OBSOLETE	TSSOP (PW)	14	-40 TO 85	View Contents	1KU |		0*		Call**	None Reported View Distributors
SN74HC00PWR	ACTIVE	TSSOP (PW)	14	-40 TO 85	View Contents	1KU | 0.11	2000	0*	2400 | 25 Apr	2 WKS	Arrow | Americas >1k BUY NOW
									>10k | 28 Apr		Avnet | Americas >1k BUY NOW
											DigiKey | Americas 316 BUY NOW

Table Data Updated on: 4/17/2003

Product Folder: SN74HC00, Quad 2-Input Positive-NAND Gates