

#### Features

- High-speed access times  
Com'l: 7, 8, 10, 12 and 15ns  
Ind'l: 8, 10, 12 and 15ns  
(use 15ns for slower designs)
- Low power operation (typical)
  - PDM41256SA  
Active: 475 mW  
Standby: 100 mW
  - PDM41256LA  
Active: 425mW  
Standby: 25 mW
- Single +5V ( $\pm 10\%$ ) power supply
- TTL-compatible inputs and outputs
- Packages
  - Plastic SOJ (300 mil) - SO
  - Plastic TSOP (I) - T

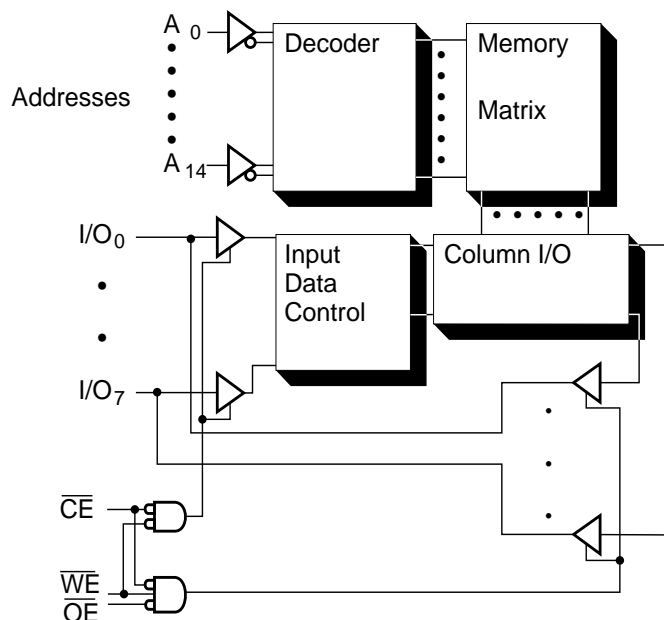
#### Description

The PDM41256 is a high-performance CMOS static RAM organized as 32,768 x 8 bits. Writing to this device is accomplished when the write enable ( $\overline{WE}$ ) and the chip enable ( $\overline{CE}$ ) inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  and  $\overline{OE}$  are both LOW.

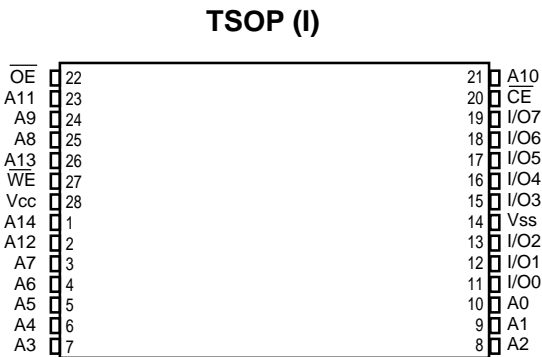
The PDM41256 operates from a single +5V power supply and all the inputs and outputs are fully TTL-compatible. The PDM41256 comes in two versions: the standard power version PDM41256SA and the low power version PDM41256LA. Both versions are functionally the same and differ only in their power consumption.

The PDM41256 is available in a 28-pin plastic TSOP (I) and a 28-pin 300-mil plastic SOJ.

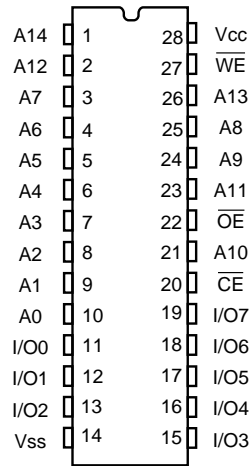
#### Functional Block Diagram



Pin Configurations



SOJ



Pin Description

Name	Description
A14-A0	Address Inputs
I/O7-I/O0	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{CE}$	Chip Enable Input
V <sub>CC</sub>	Power (+5V)
V <sub>SS</sub>	Ground

Truth Table

OE	WE	CE	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D <sub>OUT</sub>	Read
X	L	L	D <sub>IN</sub>	Write
H	H	L	Hi-Z	Output Disable

NOTE: 1. H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = DON'T CARE

Absolute Maximum Ratings <sup>(1)</sup>

Symbol	Rating	Com'l.	Ind.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to V <sub>SS</sub>	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA
T <sub>j</sub>	Maximum Junction Temperature <sup>(2)</sup>	125	145	°C

- NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form:  $T_j = T_a + P * \theta_{ja}$  where T<sub>a</sub> is the ambient temperature, P is average operating power and  $\theta_{ja}$  the thermal resistance of the package. For this product, use the following  $\theta_{ja}$  values:

SOJ: 78 °C/W  
 TSOP: 112 °C/W

### Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C
Industrial	Ambient Temperature	-40	25	85	°C

### DC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		PDM41256SA		PDM41256LA		Unit
				Min.	Max.	Min.	Max.	
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	Com'l/ Ind.	-5	5	-1	1	µA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = MAX., CE = V <sub>IH</sub> , V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>	Com'l/ Ind.	-5	5	-1	1	µA
V <sub>IL</sub>	Input Low Voltage			-0.5 <sup>(1)</sup>	0.8	-0.5 <sup>(1)</sup>	0.8	V
V <sub>IH</sub>	Input High Voltage			2.2	6.0	2.2	6.0	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8 mA, V <sub>CC</sub> = Min. I <sub>OL</sub> = 10 mA, V <sub>CC</sub> = Min.		—	0.4 0.5	—	0.4 0.5	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4 mA, V <sub>CC</sub> = Min.		2.4	—	2.4	—	V

NOTE: 1. V<sub>IL</sub>(min) = -3.0V for pulse width less than 20 ns.

### Power Supply Characteristics

Symbol	Parameter	Power	-7		-8		-10		-12		-15		Units
			Com'l.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.		
I <sub>CC</sub>	Operating Current CE = V <sub>IL</sub>  f = f <sub>MAX</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = Max I <sub>OUT</sub> = 0 mA	SA	210	200	210	190	200	170	180	150	160	mA	
		LA	190	180	190	170	180	150	160	130	140	mA	
I <sub>SB</sub>	Standby Current CE = V <sub>IH</sub>  f = f <sub>MAX</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = Max	SA	90	80	80	70	70	60	60	50	50	mA	
		LA	90	80	80	70	70	60	60	50	50	mA	
I <sub>SB1</sub>	Full Standby Current CE ≥ V <sub>CC</sub> - 0.2V  f = 0 V <sub>CC</sub> = Max V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or ≤ 0.2V	SA	20	20	20	20	20	20	20	20	20	mA	
		LA	5	5	5	5	5	5	5	5	5	mA	

SHADED AREA = PRELIMINARY DATA

NOTE: All values are maximum guaranteed values.

**Capacitance<sup>(1)</sup>** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

Symbol	Parameter	Max.	Unit
$C_{IN}$	Input Capacitance	8	pF
$C_{OUT}$	Output Capacitance	8	pF

NOTE: 1. This parameter is determined by device characterization but is not production tested.

**AC Test Conditions**

Input pulse levels	$V_{SS}$ to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

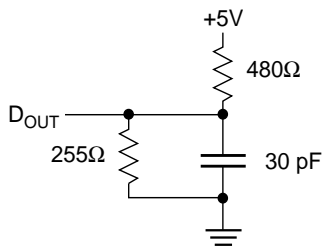


Figure 1. Output Load Equivalent

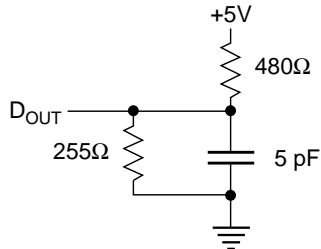


Figure 2. Output Load Equivalent  
(for  $t_{LZCE}$ ,  $t_{HZCE}$ ,  $t_{LZWE}$ ,  $t_{HZWE}$ ,  $t_{LZOE}$ ,  $t_{HZOE}$ )

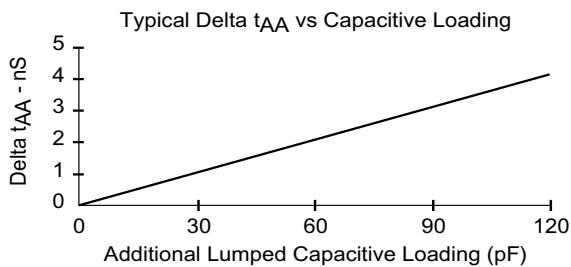
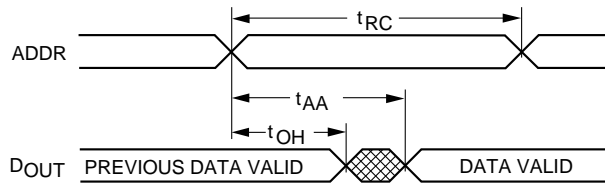
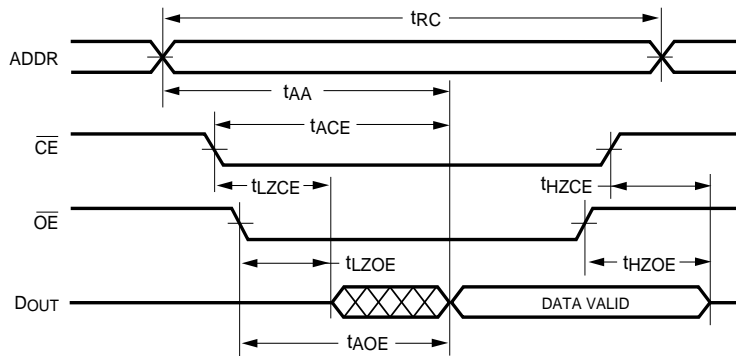


Figure 3.

Read Cycle No. 1<sup>(1)</sup>



Read Cycle No. 2<sup>(2)</sup>

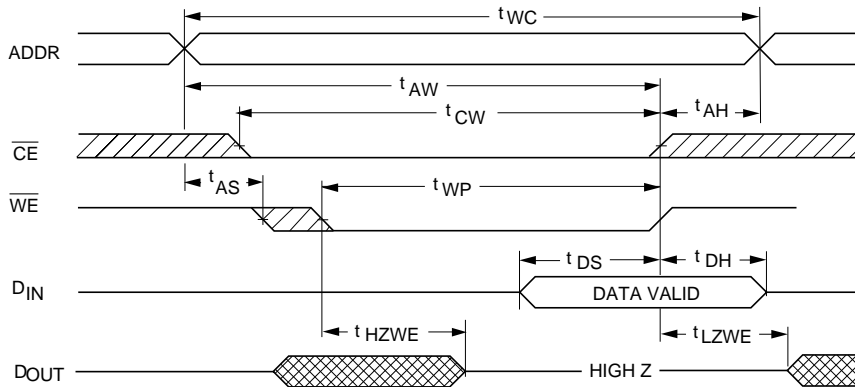


AC Electrical Characteristics

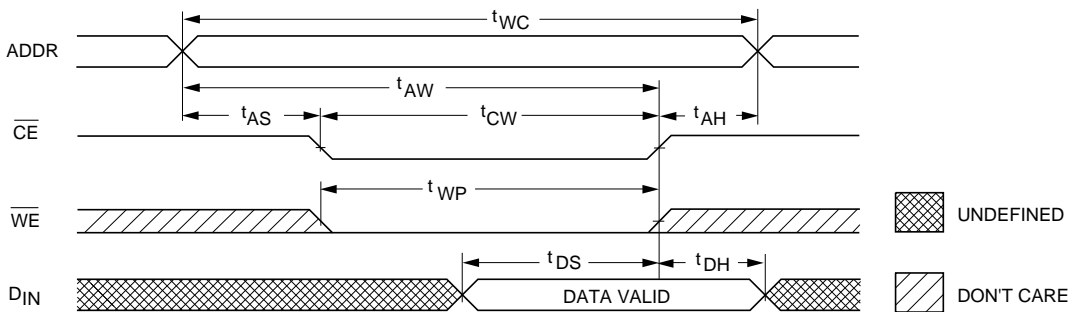
Description		-7 <sup>(6)</sup>		-8 <sup>(6)</sup>		-10 <sup>(6)</sup>		-12		-15		
READ Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
READ cycle time	t <sub>RC</sub>	7		8		10		12		15		ns
Address access time	t <sub>AA</sub>		7		8		10		12		15	ns
Chip enable access time	t <sub>ACE</sub>		7		8		10		12		15	ns
Output hold from address change	t <sub>OH</sub>	3		3		3		3		3		ns
Chip enable to output in low Z <sup>(3, 4, 5)</sup>	t <sub>LZCE</sub>	5		5		5		5		5		ns
Chip disable to output in high Z <sup>(3, 4, 5)</sup>	t <sub>HZCE</sub>		5		6		6		6		6	ns
Chip enable to power up time <sup>(4)</sup>	t <sub>PU</sub>	0		0		0		0		0		ns
Chip disable to power down time <sup>(4)</sup>	t <sub>PD</sub>		7		8		10		12		15	ns
Output enable access time	t <sub>AOE</sub>		5		5		5		6		8	ns
Output enable to output in low Z <sup>(4, 5)</sup>	t <sub>LZOE</sub>	0		0		0		0		0		ns
Output disable to output in high Z <sup>(4, 5)</sup>	t <sub>HZOE</sub>		5		6		6		6		6	ns

SHADED AREA = PRELIMINARY DATA.  
 Notes referenced are after Data Retention Table.

**Write Cycle No. 1 (Write Enable Controlled)**



**Write Cycle No. 2 (Chip Enable Controlled)**

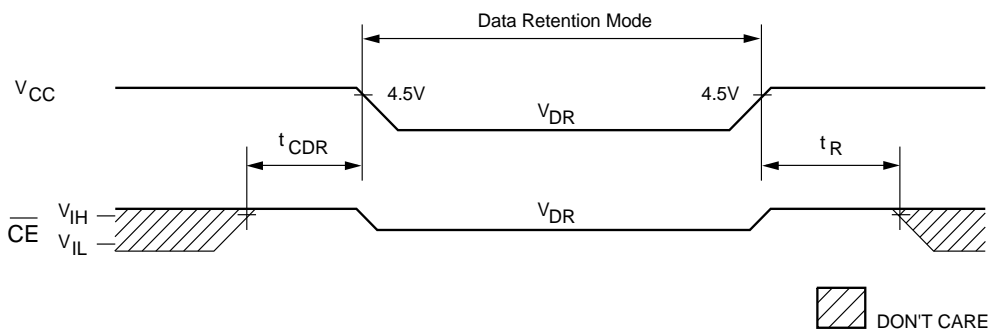


**AC Electrical Characteristics**

Description		-7 <sup>(6)</sup>		-8 <sup>(6)</sup>		-10 <sup>(6)</sup>		-12		-15		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE Cycle</b>	<b>Sym</b>											
WRITE cycle time	t <sub>WC</sub>	7		8		10		12		15		ns
Chip enable to end of write	t <sub>CW</sub>	7		8		10		10		12		ns
Address valid to end of write	t <sub>AW</sub>	7		8		10		10		12		ns
Address setup time	t <sub>AS</sub>	0		0		0		0		0		ns
Address hold from end of write	t <sub>AH</sub>	0		0		0		0		0		ns
Write pulse width	t <sub>WP</sub>	7		8		8		8		11		ns
Data setup time	t <sub>DS</sub>	6		7		7		7		7		ns
Data hold time	t <sub>DH</sub>	0		0		0		0		0		ns
Write disable to output in low Z <sup>(4, 5)</sup>	t <sub>LZWE</sub>	0		0		0		0		0		ns
Write enable to output in high Z <sup>(4, 5)</sup>	t <sub>HZWE</sub>		3		3		3		3		3	ns

SHADED AREA = PRELIMINARY DATA

### Low V<sub>CC</sub> Data Retention Waveform



### Data Retention Electrical Characteristics (LA Version Only)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Retention Data		2	—	—	V
I <sub>CCDR</sub>	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$				
		V <sub>CC</sub> = 2V	—	95	500	μA
		V <sub>CC</sub> = 3V	—	350	750	μA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time		0	—	—	ns
t <sub>R</sub> <sup>(4)</sup>	Operation Recovery Time		t <sub>RC</sub>	—	—	ns

NOTES: (For three previous Electrical Characteristics tables)

1. The device is continuously selected. Chip Enable is held in its active state.
2. The address is valid prior to or coincident with the latest occurring Chip Enable.
3. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>.
4. This parameter is sampled.
5. The parameter is tested with CL = 5 pF as shown in Figure 2. Transition is measured ±200 mV from steady state voltage
6. V<sub>CC</sub> = 5V ± 5%.

**Ordering Information**

