

# Recent Additions

## CD54AC163/3A

## CD54ACT163/3A

### Synchronous Presettable Binary Counters

Synchronous Reset

The RCA CD54AC163 and CD54ACT163 are synchronous presettable binary counters that utilize the new RCA ADVANCED CMOS LOGIC technology. The CD54AC/ACT163 devices are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

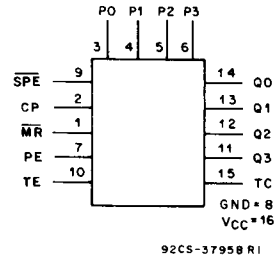
A LOW level on the Synchronous Parallel Enable input,  $\overline{SPE}$ , disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for  $\overline{SPE}$  are met).

The counters are reset with a LOW level on the Master Reset input,  $\overline{MR}$ . The requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. Reset action occurs regardless of the level of the  $\overline{SPE}$ , PE, and TE inputs.

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be HIGH to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count, the terminal count (TC) output goes HIGH for one clock period. This TC pulse is used to enable the next cascaded stage.

The CD54AC163 and CD54ACT163 are supplied in 16-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM

### Package Specifications

(See Section 11, Fig. 11)

### Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

| CHARACTERISTICS                | TEST CONDITIONS |                 | $V_{CC}$<br>(V) | AMBIENT TEMPERATURE ( $T_A$ ) - °C |      |             |      | UNITS |         |
|--------------------------------|-----------------|-----------------|-----------------|------------------------------------|------|-------------|------|-------|---------|
|                                |                 |                 |                 | +25                                |      | -55 to +125 |      |       |         |
|                                |                 |                 |                 | MIN.                               | MAX. | MIN.        | MAX. |       |         |
| Quiescent Supply Current (MSI) | $I_{CC}$        | $V_{CC}$ or GND | 0               | 5.5                                | —    | 8•          | —    | 160•  | $\mu A$ |

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

### ACT INPUT LOADING TABLE

| INPUT                | UNIT LOAD* |
|----------------------|------------|
| $P_n$                | 0.13       |
| CP                   | 1          |
| $\overline{MR}$ , TE | 0.83       |
| $\overline{SPE}$     | 0.67       |
| PE                   | 0.5        |

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

### Burn-In Test-Circuit Connections

Identical to CD54HC/HCT163/3A, page 5-70.

# Recent Additions

## CD54AC163/3A

## CD54ACT163/3A

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$  (Worst Case)

| CHARACTERISTICS                               | SYMBOL                               | V <sub>CC</sub><br>(V) | -55 to +125°C |       | UNITS |
|---|--------------------------------------|------------------------|---------------|-------|-------|
|   |                                      |                        | MIN.          | MAX.  |       |
| Propagation Delays:<br>CP to Qn<br>(SPE HIGH) | t <sub>PLH</sub><br>t <sub>PHL</sub> | 1.5                    | —             | 207   | ns    |
|   |                                      | 3.3*                   | 4.3           | 23.1  |       |
|   |                                      | 5†                     | 2.8           | 16.5  |       |
| CP to Qn<br>(SPE LOW)                         | t <sub>PLH</sub><br>t <sub>PHL</sub> | 1.5                    | —             | 207   | ns    |
|   |                                      | 3.3                    | 4.3           | 23.1  |       |
|   |                                      | 5                      | 2.8           | 16.5* |       |
| CP to TC                                      | t <sub>PLH</sub><br>t <sub>PHL</sub> | 1.5                    | —             | 209   | ns    |
|   |                                      | 3.3                    | 4.4           | 23.4  |       |
|   |                                      | 5                      | 2.9           | 16.7* |       |
| TE to TC                                      | t <sub>PLH</sub><br>t <sub>PHL</sub> | 1.5                    | —             | 129   | ns    |
|   |                                      | 3.3                    | 2.6           | 14.4  |       |
|   |                                      | 5                      | 1.8           | 10.3* |       |
| Power Dissipation Capacitance                 | C <sub>PD</sub> §                    | —                      |               |       | pF    |
| Input Capacitance                             | C <sub>I</sub>                       | —                      | —             | 10    | pF    |

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$  (Worst Case)

| CHARACTERISTICS                               | SYMBOL                               | V <sub>CC</sub><br>(V) | -55 to +125°C |       | UNITS |
|---|--------------------------------------|------------------------|---------------|-------|-------|
|   |                                      |                        | MIN.          | MAX.  |       |
| Propagation Delays:<br>CP to Qn<br>(SPE HIGH) | t <sub>PLH</sub><br>t <sub>PHL</sub> | 5†                     | 2.8           | 16.5  | ns    |
|   |                                      | 5                      | 2.8           | 16.5* | ns    |
|   |                                      |                        | 2.9           | 16.7* | ns    |
|   |                                      |                        | 1.8           | 10.8* | ns    |
| TE to TC                                      | 5                                    | 1.8                    | 10.8*         | ns    |       |
| Power Dissipation Capacitance                 | C <sub>PD</sub> §                    | —                      |               |       | pF    |
| Input Capacitance                             | C <sub>I</sub>                       | —                      | —             | 10    | pF    |

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption per device.

For AC,  $P_D = C_{PD}V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$

For ACT,  $P_D = C_{PD}V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) | V_{CC} \Delta I_{CC}$  where

$f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage

(Limits with black dots (\*) are tested 100%.)