Rochester Electronics

# Datasheet

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FAIRCHILD SEMICONDUCTOR®

March 2007

# 74AC109, 74ACT109
# Dual $J\overline{K}$ Positive Edge-Triggered Flip-Flop

## Features

- $I_{CC}$ reduced by 50%
- Outputs source/sink 24mA
- ACT109 has TTL-compatible inputs

## General Description

The AC/ACT109 consists of two high-speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D-Type flip-flop (refer to AC/ACT74 data sheet) by connecting the J and $\overline{K}$ inputs together.

Asynchronous Inputs:

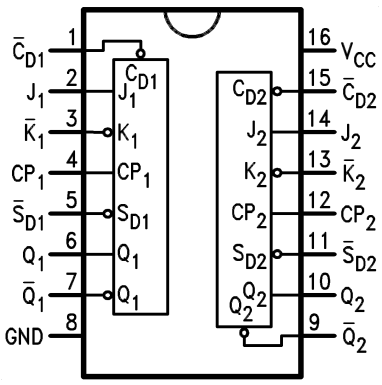
- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

## Ordering Information

| Order Number | Package Number | Package Description |
|---|---|---|
| 74AC109SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74AC109SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC109MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT109SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74AC109MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT109PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $J_1$, $J_2$, $\overline{K}_1$, $\overline{K}_2$ | Data Inputs |
| $CP_1$, $CP_2$ | Clock Pulse Inputs |
| $\overline{C}_{D1}$, $\overline{C}_{D2}$ | Direct Clear Inputs |
| $\overline{S}_{D1}$, $\overline{S}_{D2}$ | Direct Set Inputs |
| $Q_1$, $Q_2$, $\overline{Q}_1$, $\overline{Q}_2$ | Outputs |

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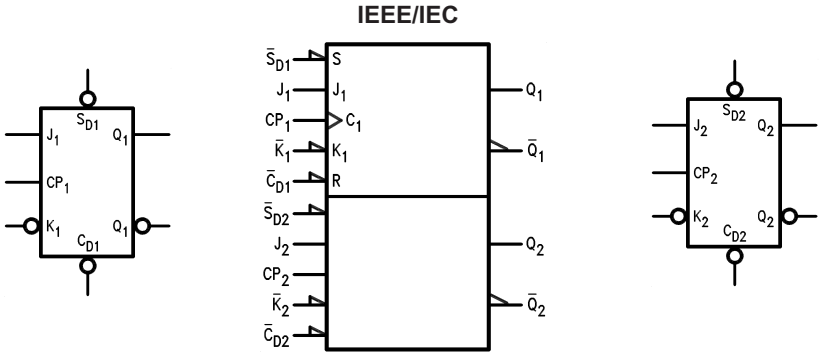
## Logic Symbols




## Truth Table

Each half.

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{S}_D$ | $\overline{C}_D$ | CP | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H | H |
| H | H | ↗ | L | L | L | H |
| H | H | ↗ | H | L | Toggle | |
| H | H | ↗ | L | H | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↗ | H | H | H | L |
| H | H | L | X | X | $Q_0$ | $\overline{Q}_0$ |

H = HIGH Voltage Level

L = LOW Voltage Level

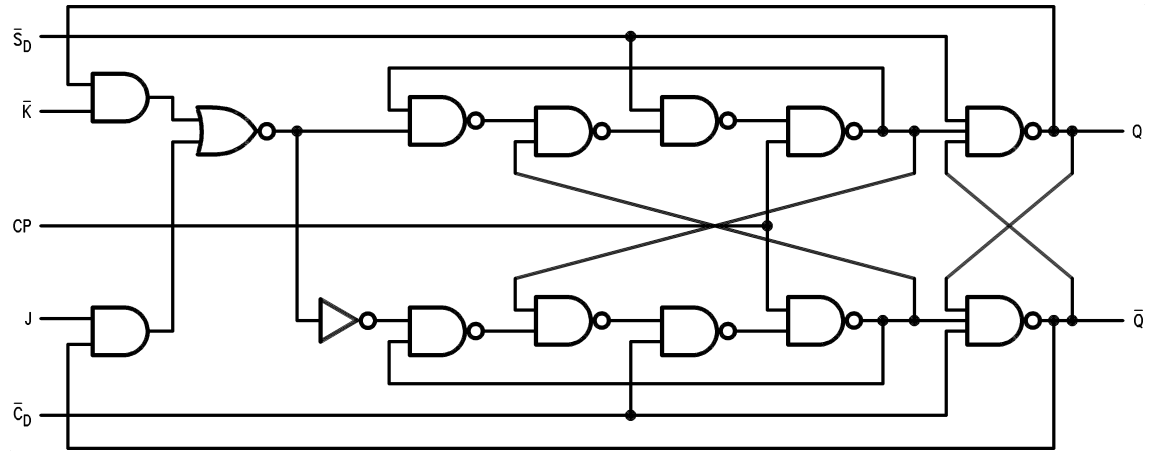
↗ = LOW-to-HIGH Transition

X = Immaterial

$Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before LOW-to-HIGH Transition of Clock

## Logic Diagram

One half shown.




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.5V to +7.0V |
| $I_{IK}$ | DC Input Diode Current | |
| | $V_I = –0.5V$ | –20mA |
| | $V_I = V_{CC} + 0.5V$ | +20mA |
| $V_I$ | DC Input Voltage | –0.5V to $V_{CC}$ + 0.5V |
| $I_{OK}$ | DC Output Diode Current | |
| | $V_O = –0.5V$ | –20mA |
| | $V_O = V_{CC} + 0.5V$ | +20mA |
| $V_O$ | DC Output Voltage | –0.5V to $V_{CC}$ + 0.5V |
| $I_O$ | DC Output Source or Sink Current | ±50mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current per Output Pin | ±50mA |
| $T_{STG}$ | Storage Temperature | –65°C to +150°C |
| $T_J$ | Junction Temperature | 140°C |

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|---|---|---|
| $V_{CC}$ | Supply Voltage | |
| | AC | 2.0V to 6.0V |
| | ACT | 4.5V to 5.5V |
| $V_I$ | Input Voltage | 0V to $V_{CC}$ |
| $V_O$ | Output Voltage | 0V to $V_{CC}$ |
| $T_A$ | Operating Temperature | –40°C to +85°C |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, AC Devices: | 125mV/ns |
| | $V_{IN}$ from 30% to 70% of $V_{CC}$, $V_{CC}$ @ 3.3V, 4.5V, 5.5V | |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, ACT Devices: | 125mV/ns |
| | $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V | |

## DC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = +25°C | $T_A$ = –40°C to +85°C | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ. | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 3.0 | $V_{OUT}$ = 0.1V or $V_{CC}$ – 0.1V | 1.5 | 2.1 | 2.1 | V |
| | | 4.5 | | 2.25 | 3.15 | 3.15 | |
| | | 5.5 | | 2.75 | 3.85 | 3.85 | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 3.0 | $V_{OUT}$ = 0.1V or $V_{CC}$ – 0.1V | 1.5 | 0.9 | 0.9 | V |
| | | 4.5 | | 2.25 | 1.35 | 1.35 | |
| | | 5.5 | | 2.75 | 1.65 | 1.65 | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 3.0 | $I_{OUT}$ = –50µA | 2.99 | 2.9 | 2.9 | V |
| | | 4.5 | | 4.49 | 4.4 | 4.4 | |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | |
| | | 3.0 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$: $I_{OH}$ = –12mA | | 2.56 | 2.46 | |
| | | 4.5 | $I_{OH}$ = –24mA | | 3.86 | 3.76 | |
| | | 5.5 | $I_{OH}$ = –24mA(1) | | 4.86 | 4.76 | |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 3.0 | $I_{OUT}$ = 50µA | 0.002 | 0.1 | 0.1 | V |
| | | 4.5 | | 0.001 | 0.1 | 0.1 | |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | |
| | | 3.0 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$: $I_{OL}$ = 12mA | | 0.36 | 0.44 | |
| | | 4.5 | $I_{OL}$ = 24mA | | 0.36 | 0.44 | |
| | | 5.5 | $I_{OL}$ = 24mA(1) | | 0.36 | 0.44 | |
| $I_{IN}$(3) | Maximum Input Leakage Current | 5.5 | $V_I$ = $V_{CC}$, GND | | ±0.1 | ±1.0 | µA |
| $I_{OLD}$ | Minimum Dynamic Output Current(2) | 5.5 | $V_{OLD}$ = 1.65V Max. | | | 75 | mA |
| $I_{OHD}$ | | | $V_{OHD}$ = 3.85V Min. | | | –75 | mA |
| $I_{CC}$(3) | Maximum Quiescent Supply Current | 5.5 | $V_{IN}$ = $V_{CC}$ or GND | | 2.0 | 20.0 | µA |

**Notes:**

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. $I_{IN}$ and $I_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{CC}$.

## DC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = +25°C | $T_A$ = –40°C to +85°C | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ. | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 4.5 | $V_{OUT}$ = 0.1V or $V_{CC}$ – 0.1V | 1.5 | 2.0 | 2.0 | V |
| | | 5.5 | | 1.5 | 2.0 | 2.0 | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 4.5 | $V_{OUT}$ = 0.1V or $V_{CC}$ – 0.1V | 1.5 | 0.8 | 0.8 | V |
| | | 5.5 | | 1.5 | 0.8 | 0.8 | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 4.5 | $I_{OUT}$ = –50µA | 4.49 | 4.4 | 4.4 | V |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | |
| | | 4.5 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$: $I_{OH}$ = –24mA | | 3.86 | 3.76 | |
| | | 5.5 | $I_{OH}$ = –24mA[4] | | 4.86 | 4.76 | |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 4.5 | $I_{OUT}$ = 50µA | 0.001 | 0.1 | 0.1 | V |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | |
| | | 4.5 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$: $I_{OL}$ = 24mA | | 0.36 | 0.44 | |
| | | 5.5 | $I_{OL}$ = 24mA[4] | | 0.36 | 0.44 | |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | $V_I$ = $V_{CC}$, GND | | ±0.1 | ± 1.0 | µA |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | $V_I$ = $V_{CC}$ – 2.1V | 0.6 | | 1.5 | mA |
| $I_{OLD}$ | Minimum Dynamic Output Current[5] | 5.5 | $V_{OLD}$ = 1.65V Max. | | | 75 | mA |
| $I_{OHD}$ | | | $V_{OHD}$ = 3.85V Min. | | | –75 | mA |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | $V_{IN}$ = $V_{CC}$ or GND | | 2.0 | 20.0 | µA |

**Notes:**

4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0ms, one output loaded at a time.

## AC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ (V)[6] | $T_A$ = +25°C, $C_L$ = 50pF | | | $T_A$ = –40°C to +85°C, $C_L$ = 50pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| $f_{MAX}$ | Maximum Clock Frequency | 3.3 | 125 | 150 | | 100 | | MHz |
| | | 5.0 | 150 | 175 | | 125 | | |
| $t_{PLH}$ | Propagation Delay, $CP_n$ to $Q_n$ or $\overline{Q}_n$ | 3.3 | 4.0 | 8.0 | 13.5 | 3.5 | 16.0 | ns |
| | | 5.0 | 2.5 | 6.0 | 10.0 | 2.0 | 10.5 | |
| $t_{PHL}$ | Propagation Delay, $CP_n$ to $Q_n$ or $\overline{Q}_n$ | 3.3 | 3.0 | 8.0 | 14.0 | 3.0 | 14.5 | ns |
| | | 5.0 | 2.0 | 6.0 | 10.0 | 1.5 | 10.5 | |
| $t_{PLH}$ | Propagation Delay, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 3.3 | 3.0 | 8.0 | 12.0 | 2.5 | 13.0 | ns |
| | | 5.0 | 2.5 | 6.0 | 9.0 | 2.0 | 10.0 | |
| $t_{PHL}$ | Propagation Delay, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 3.3 | 3.0 | 10.0 | 12.0 | 3.0 | 13.5 | ns |
| | | 5.0 | 2.0 | 7.5 | 9.5 | 2.0 | 10.5 | |

**Note:**

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

## AC Operating Requirements for AC

| Symbol | Parameter | $V_{CC}$ (V)[7] | $T_A$ = +25°C, $C_L$ = 50pF | $T_A$ = –40°C to +85°C, $C_L$ = 50 pF | | Units |
|---|---|---|---|---|---|---|
| | | | Typ. | Guaranteed Minimum | | |
| $t_S$ | Setup Time, HIGH or LOW, $J_n$ or $\overline{K}_n$ to $CP_n$ | 3.3 | 3.5 | 6.5 | 7.5 | ns |
| | | 5.0 | 2.0 | 4.5 | 5.0 | |
| $t_H$ | Hold Time, HIGH or LOW, $J_n$ or $\overline{K}_n$ to $CP_n$ | 3.3 | –1.5 | 0 | 0 | ns |
| | | 5.0 | –0.5 | 0.5 | 0.5 | |
| $t_W$ | Pulse Width, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ | 3.3 | 2.0 | 7.0 | 7.5 | ns |
| | | 5.0 | 2.0 | 4.5 | 5.0 | |
| $t_{REC}$ | Recovery Time, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $CP_n$ | 3.3 | –2.5 | 0 | 0 | ns |
| | | 5.0 | –1.5 | 0 | 0 | |

**Note:**

7. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V

## AC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC}$ (V)[8] | $T_A$ = +25°C, $C_L$ = 50pF | | | $T_A$ = –40°C to +85°C, $C_L$ = 50pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| $f_{MAX}$ | Maximum Clock Frequency | 5.0 | 145 | 210 | | 125 | | MHz |
| $t_{PLH}$ | Propagation Delay, $CP_n$ to $Q_n$ or $\overline{Q}_n$ | 5.0 | 4.0 | 7.0 | 11.0 | 3.5 | 13.0 | ns |
| $t_{PHL}$ | Propagation Delay, $CP_n$ to $Q_n$ or $\overline{Q}_n$ | 5.0 | 3.0 | 6.0 | 10.0 | 2.5 | 11.5 | ns |
| $t_{PLH}$ | Propagation Delay, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 5.0 | 2.5 | 5.5 | 9.5 | 2.0 | 10.5 | ns |
| $t_{PHL}$ | Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 5.0 | 2.5 | 6.0 | 10.0 | 2.0 | 11.5 | ns |

**Note:**

8. Voltage range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements for ACT

| Symbol | Parameter | $V_{CC}$ (V)[9] | $T_A$ = +25°C, $C_L$ = 50pF | $T_A$ = –40°C to +85°C, $C_L$ = 50pF | | Units |
|---|---|---|---|---|---|---|
| | | | Typ. | Guaranteed Minimum | | |
| $t_S$ | Setup Time, HIGH or LOW, $J_n$ or $\overline{K}_n$ to $CP_n$ | 5.0 | 0.5 | 2.0 | 2.5 | ns |
| $t_H$ | Hold Time, HIGH or LOW, $J_n$ or $\overline{K}_n$ to $CP_n$ | 5.0 | 0 | 2.0 | 2.0 | ns |
| $t_W$ | Pulse Width, $CP_n$ or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ | 5.0 | 3.0 | 5.0 | 6.0 | ns |
| $t_{rec}$ | Recovery Time, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $CP_n$ | 5.0 | –2.5 | 0 | 0 | ns |

**Note:**

9. Voltage range 5.0 is 5.0V ± 0.5V

## Capacitance

| Symbol | Parameter | Conditions | Typ. | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = OPEN | 4.5 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_{CC}$ = 5.0V | 35.0 | pF |

## Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

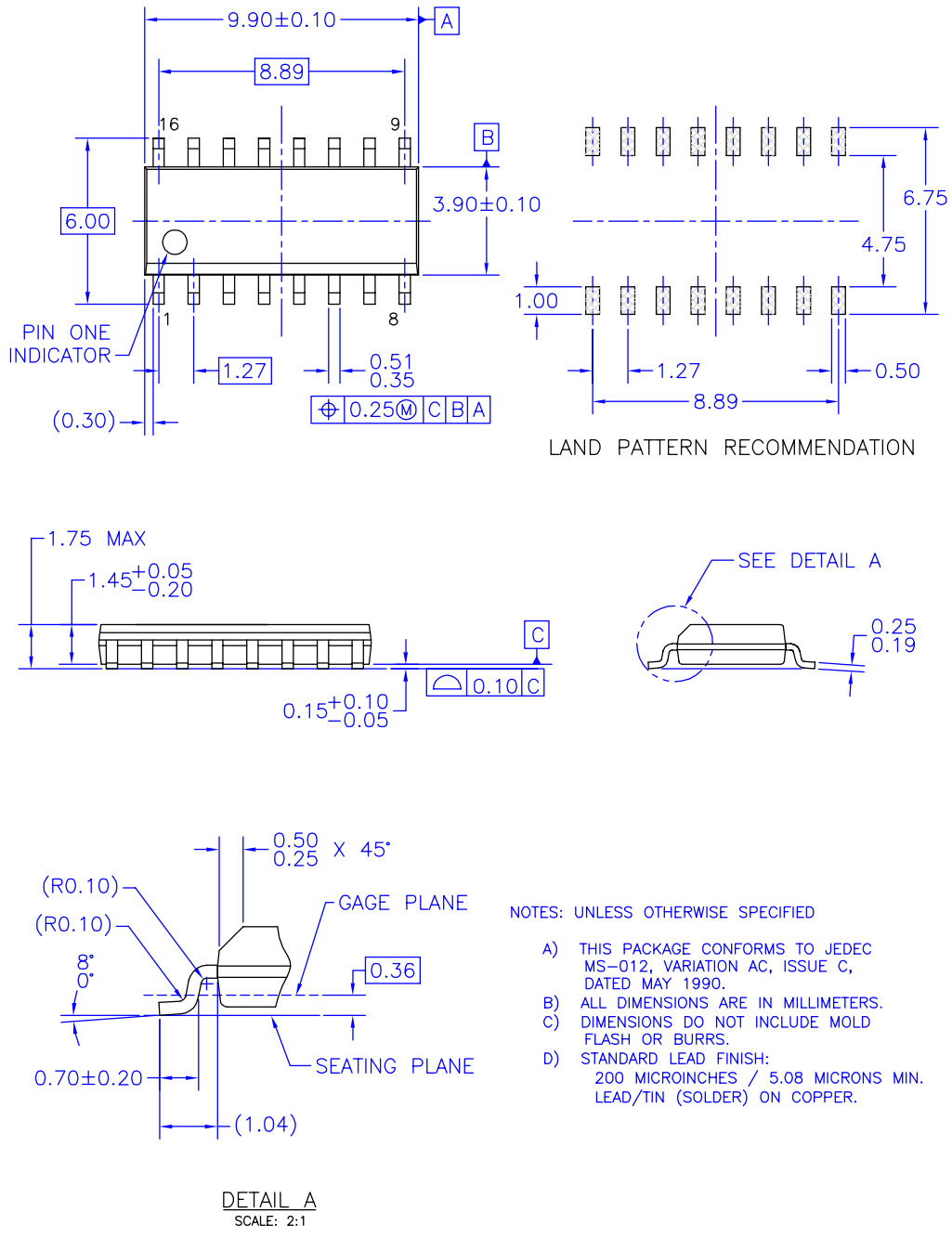
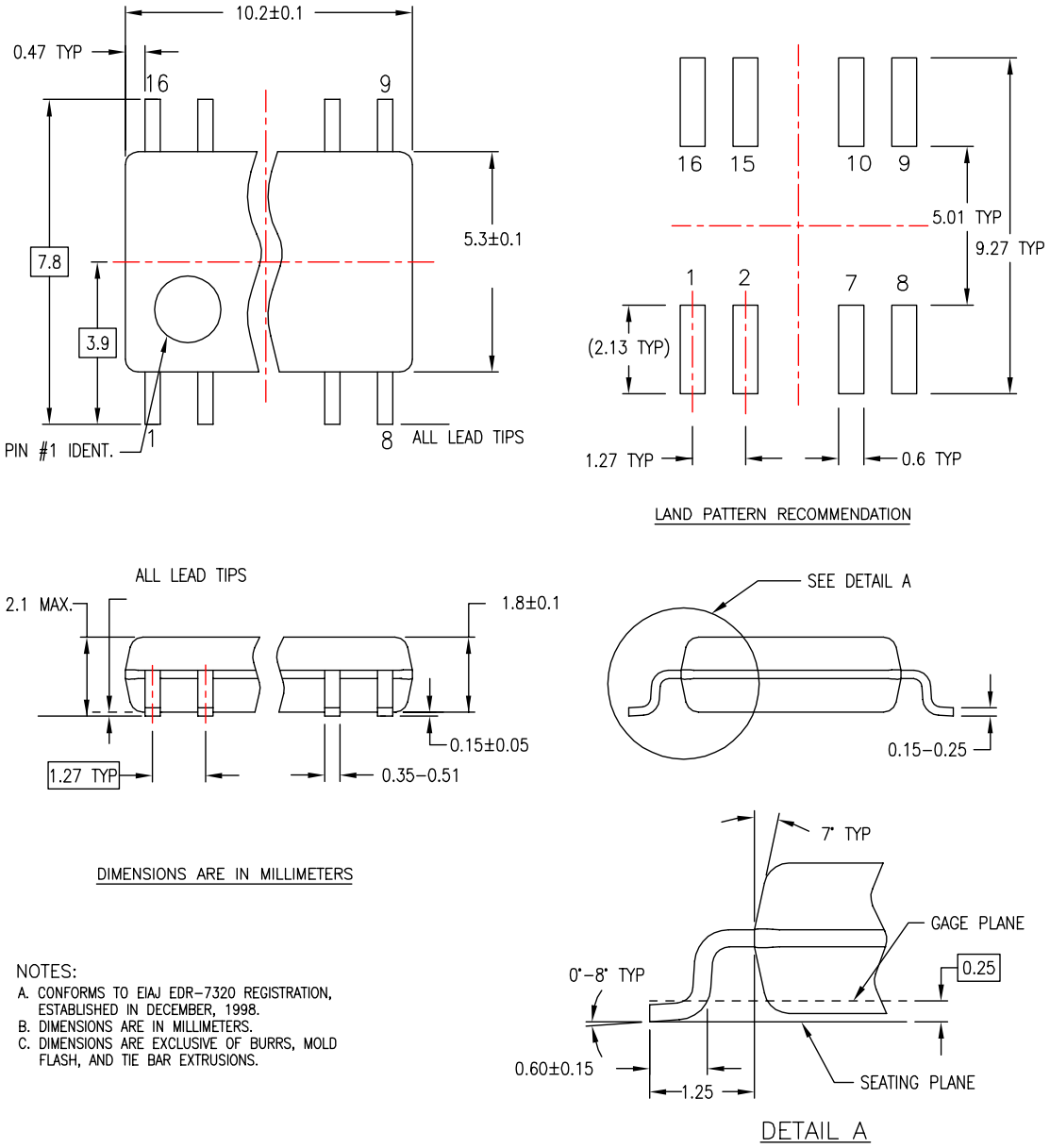



**Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M16A**

## Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.




NOTES:

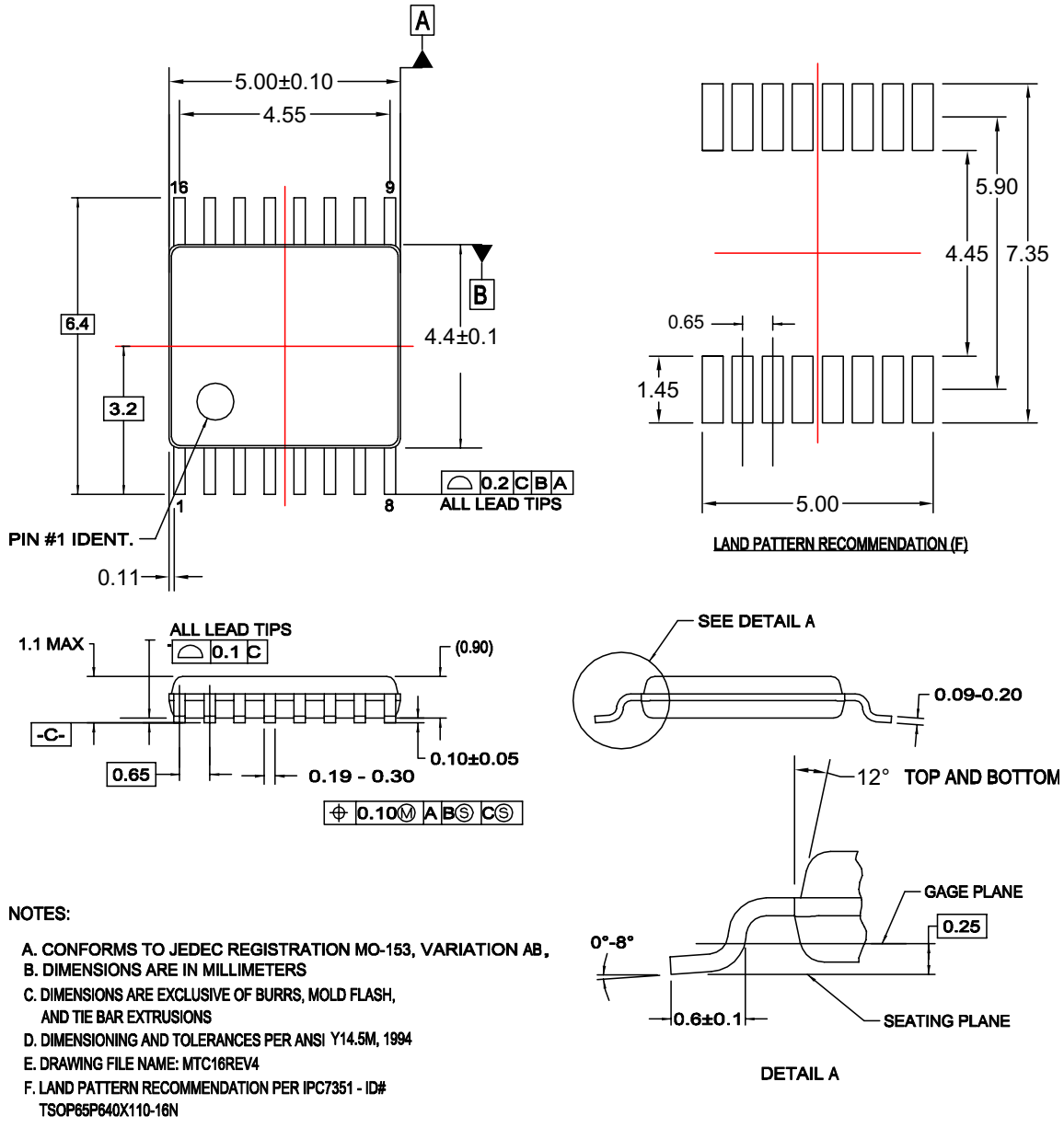
A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DREVC

**Figure 2. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M16D**

## Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REV4
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

**Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**

## Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

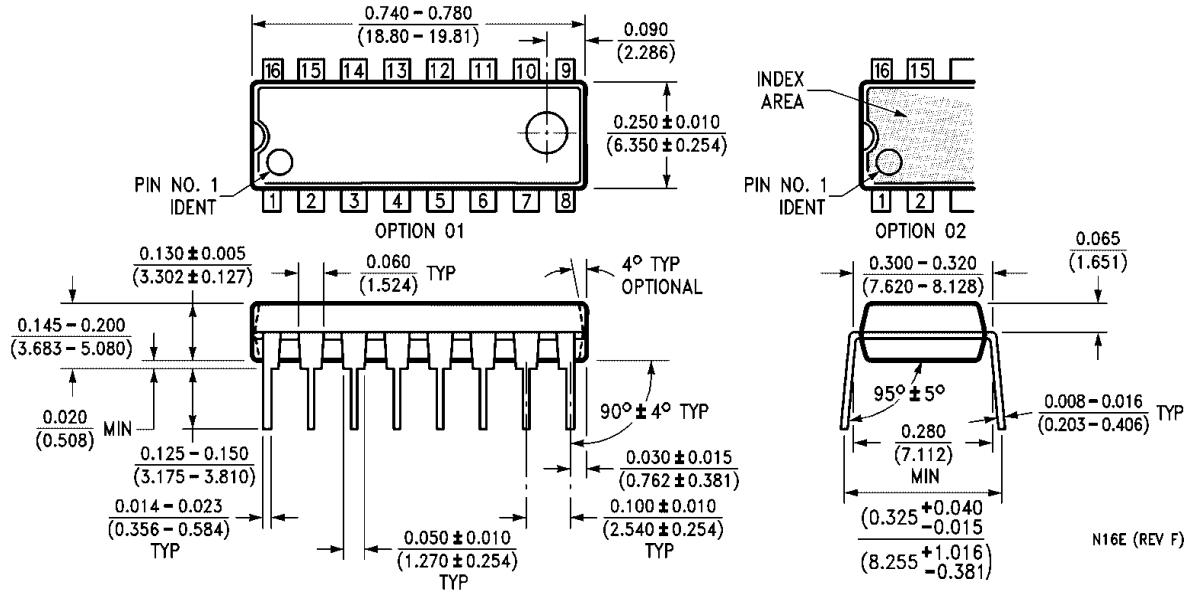



**Figure 4. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**

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QS™
QT Optoelectronics™
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RapidConfigure™
RapidConnect™
ScalarPump™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TCM™
The Power Franchise®
™
TinyBoost™
TinyBuck™
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
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Rev. I24