



Dual P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.027 @ $V_{GS} = -10$ V	-9.0
	0.039 @ $V_{GS} = -4.5$ V	-7.5

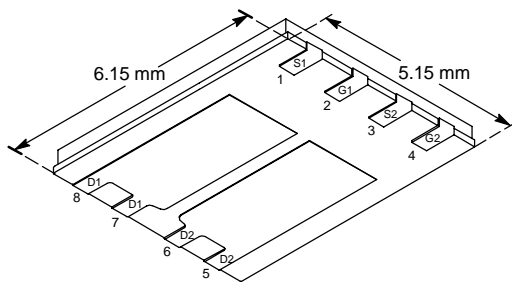
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile

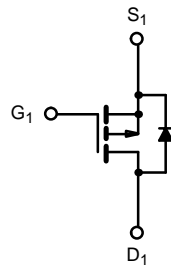
APPLICATIONS

- 3–4 Cell Li-Ion Battery Switch
- Bus Load Switch for Notebook/Desktop Computers

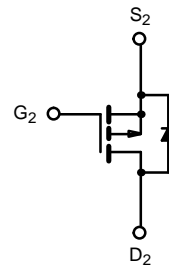
PowerPAK™ SO-8



Bottom View



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-30		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-9.0	-5.8	A
		$T_A = 70^\circ\text{C}$	-7.2	-4.7	
Pulsed Drain Current	I_{DM}	-30			
continuous Source Current (Diode Conduction) ^a	I_S	-2.9	-1.2		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	3.5	1.4	W
		$T_A = 70^\circ\text{C}$	2.2	0.9	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	26	35	$^\circ\text{C/W}$
		Steady State	60	85	
Maximum Junction-to-Case (Drain)	R_{thJC}	2.2	2.7		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

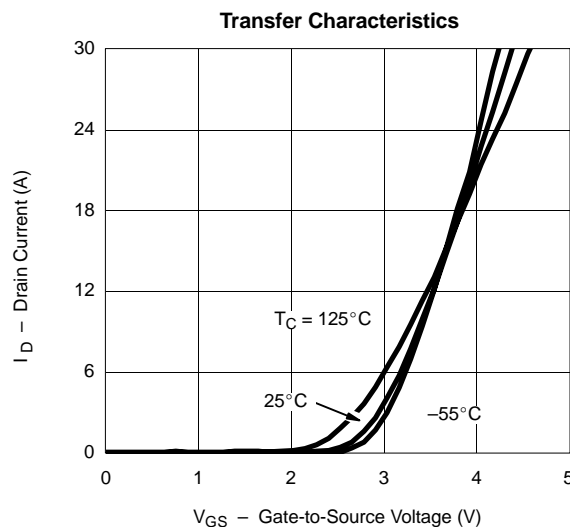
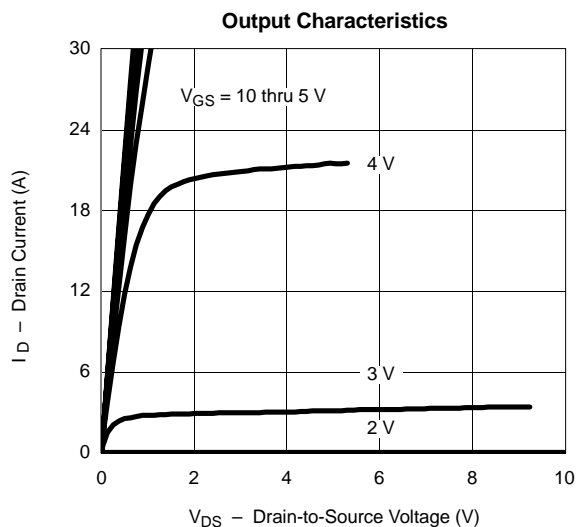
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 70^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = -9 \text{ A}$		0.022	0.027	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -5 \text{ A}$		0.032	0.039	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -2.5 \text{ A}$		14		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.9 \text{ A}, V_{GS} = 0 \text{ V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -9 \text{ A}$		42	51	nC
Gate-Source Charge	Q_{gs}			8.5		
Gate-Drain Charge	Q_{gd}			7.5		
Gate Resistance	R_G			2.9		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15 \text{ V}, R_L = 15 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -10 \text{ V}, R_G = 6 \Omega$		18	30	ns
Rise Time	t_r			29	45	
Turn-Off Delay Time	$t_{d(off)}$			65	100	
Fall Time	t_f			27	41	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.9 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		50	90	

Notes

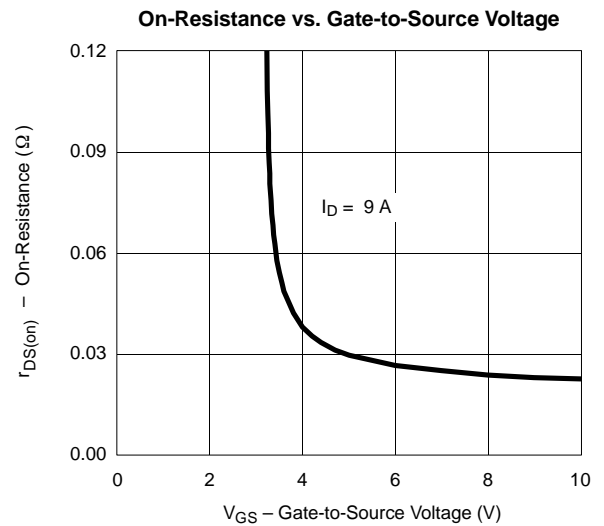
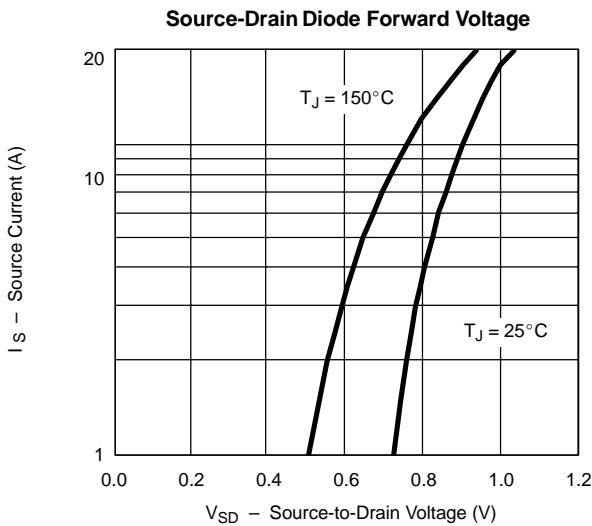
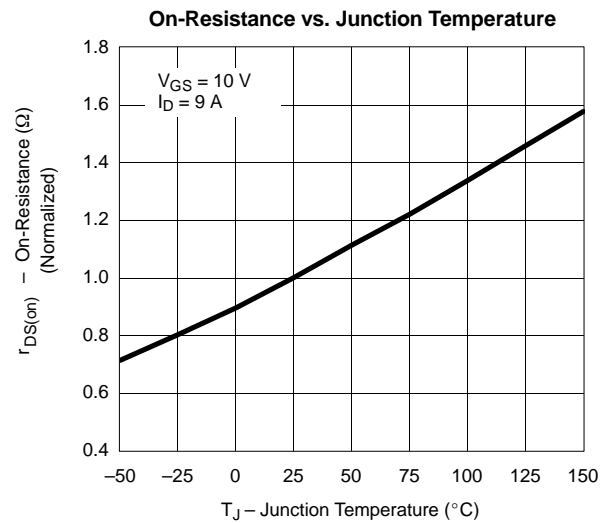
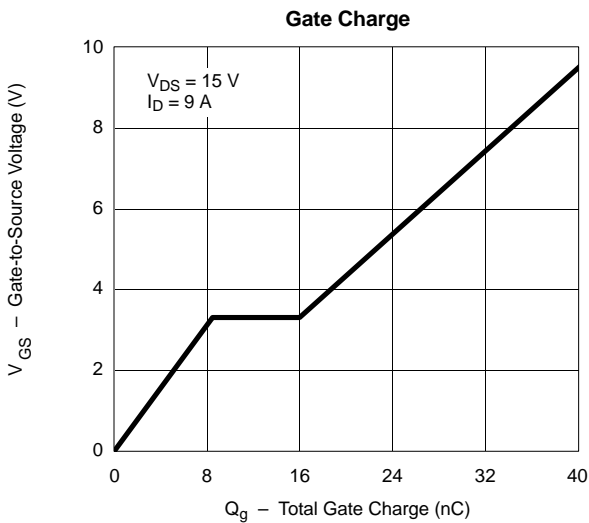
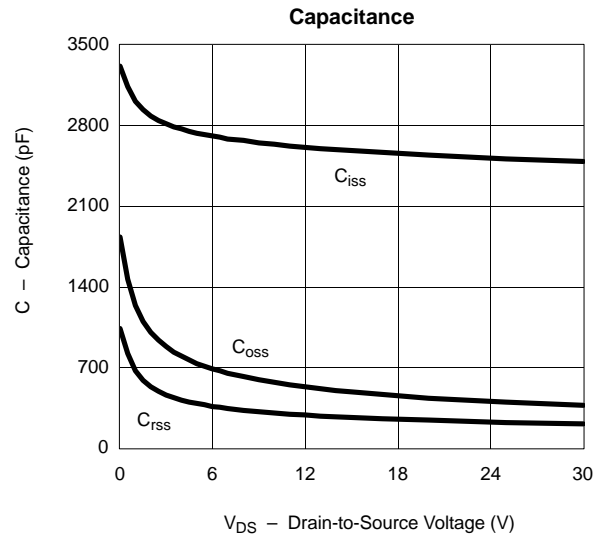
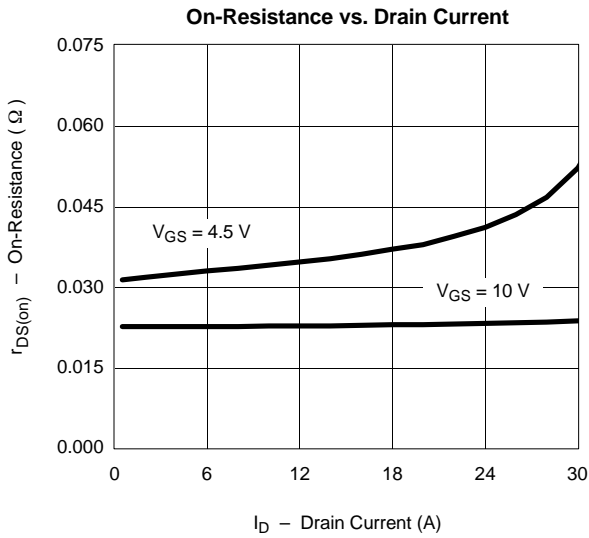
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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