M5M416165DJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS with EDO(Extended Data Out : Hyper Page) mode function, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M416165DXX-5,5S	50	13	25	13	90	540
M5M416165DXX-6,6S	60	15	30	15	110	430
M5M416165DXX-7,7S	70	20	35	20	130	385

XX=J,TP

- Standard 42 pin SOJ,50 pin TSOP
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M416165Dxx- 5,5S ---------- 660.0mW (Max)
  M5M416165Dxx- 6,6S ---------- 525.0mW (Max)
  M5M416165Dxx- 7,7S ---------- 470.0mW (Max)
- EDO mode , Read-modify-write,$\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode , $\overline{W}$ and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
  4096 refresh cycles every 64ms (A_0 ~ A_{11})
  4096 refresh cycles every 128ms (A_0 ~ A_{11}) *
  * : Applicable to self refresh version
  (M5M416165DXX-5S,-6S,-7S:option) only

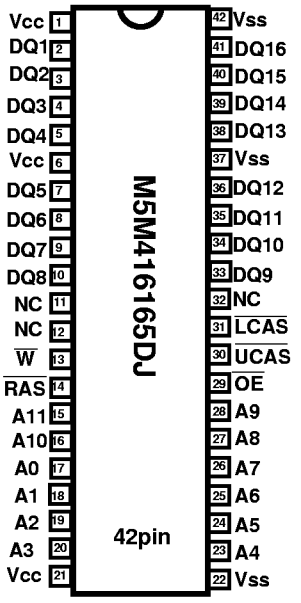
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

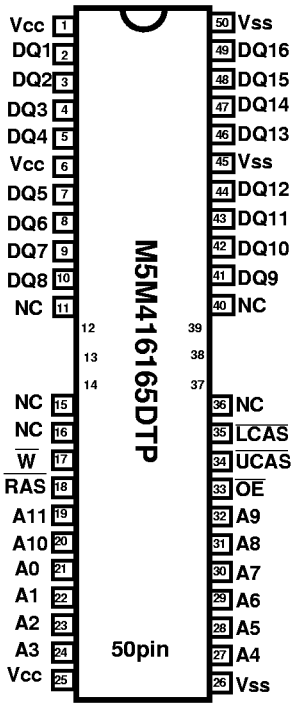
PIN DESCRIPTION

Pin Name	Function
A_0-A_{11}	Address Inputs
DQ_1-DQ_{16}	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{UCAS}$	Upper Byte Control Column Address Strobe Input
$\overline{LCAS}$	Lower Byte Control Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+5.0V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 42P0N-A (400mil SOJ)



Outline 50P3G-F (400mil TSOP Normal Bend)

MITSUBISHI ELECTRIC

M5M416165DJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

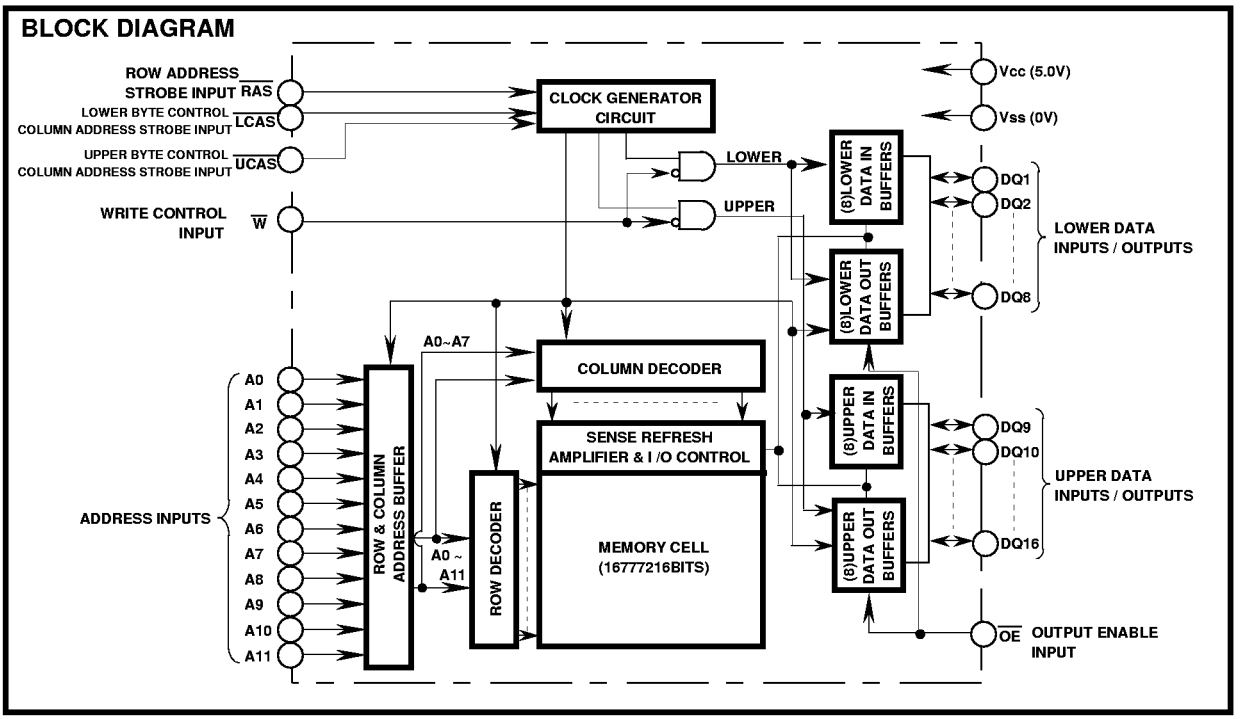
The M5M416165DJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., EDO mode, $\overline{RAS}$ only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16		
Lower byte Read	ACT	ACT	NAC	NAC	ACT	VLD	OPN	YES	EDO mode identical
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	VLD	YES	
Word Read	ACT	ACT	ACT	NAC	ACT	VLD	VLD	YES	
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC	YES	
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN	YES	
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	ACT	NAC	ACT	VLD	VLD	YES	
Self refresh	ACT	ACT	ACT	NAC	DNC	OPN	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	OPN	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



M5M416165DJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1 ~ 7	V
VI	Input voltage		-1 ~ 7	V
VO	Output voltage		-1 ~ 7	V
IO	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C , unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss

** : VIL(Min) is -2.0V when undershoot width is less than 25ns.(The width is defined as the period when the voltage level is below Vss.)

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C , Vcc=5.0V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≤ V_{OUT} ≤ 5.5V	-10		10	µA
I_I	Input current		0V ≤ V_{IN} ≤ 5.5V, Other inputs pins=0V	-10		10	µA
$I_{CC1\ (AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M416165D-5,5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			120	mA
		M5M416165D-6,6S				95	
		M5M416165D-7,7S				85	
I_{CC2}	Supply current from Vcc , stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≥ Vcc -0.2 V output open			1	
						0.3 *	
$I_{CC3\ (AV)}$	Average supply current from Vcc refreshing (Note 3,5)	M5M416165D-5,5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			120	mA
		M5M416165D-6,6S				95	
		M5M416165D-7,7S				85	
$I_{CC4(AV)}$	Average supply current from Vcc EDO-Mode (Note 3,4,5)	M5M416165D-5,5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			165	mA
		M5M416165D-6,6S				130	
		M5M416165D-7,7S				110	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M416165D-5,5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			120	mA
		M5M416165D-6,6S				95	
		M5M416165D-7,7S				85	
$I_{CC8\ (AV)}$ *	Average supply current from Vcc Extended - Refresh cycle (Note 6)	M5M416165D (S)	Stand-by: $\overline{RAS}$≥Vcc-0.2V $\overline{CAS}$≥Vcc-0.2V or $\overline{CAS}$≤0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≤0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≤0.2V or ≥Vcc-0.2V $\overline{OE}$≤0.2V or ≥Vcc-0.2V A0 ~ A9 ≤ 0.2V or ≥ Vcc-0.2V DQ=open, TRC=125µs, TRAS=TRASmin. ~ 1µs			600	µA
$I_{CC9\ (AV)}$ *	Average supply current from Vcc Self - Refresh cycle	M5M416165D (S)	$\overline{RAS}$ = $\overline{CAS}$ ≤ 0.2V			400	µA

* : Applicable to self refresh version (M5M416165DXX-5S,-6S,-7S:option) only

Note 2: Current flowing into an IC is positive, out is negative.

3: Icc1 (AV), Icc3 (AV) and Icc4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

CAPACITANCE (Ta=0 ~ 70°C , Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	M5M416165DJ, TP	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input					7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input					7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input					7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input					7	pF
$C_{I/O}$	Input/Output capacitance, data ports					7	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C , Vcc = 5.0V ± 10%, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M416165D-5,5S		M5M416165D-6,6S		M5M416165D-7,7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{CAS}$		5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{WE}$ low	(Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns

Note 6: An initial pause of 500µs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(I_{OH}=-5mA) / VOL=0.4V(I_{OL}=4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that $t_{RCD} \geq t_{RCD}$(max) and $t_{ASC} \geq t_{ASC}$(max) and $t_{CP} \geq t_{CP}$(max).

9: Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD}$(max) and $t_{ASC} \leq t_{ASC}$(max).

11: Assumes that $t_{CP} \leq t_{CP}$(max) and $t_{ASC} \geq t_{ASC}$(max).

12: t_{OEZ} (max) ,t_{WEZ}(max) ,t_{OFF}(max) and t_{REZ}(max) defines the time at which the output achieves the high impedance state ($I_{OUT} \leq | \pm 10\ \mu A |$) and is not reference to VOH(min) or VOL(max).

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and EDO Mode Cycles)

(Ta=0 ~ 70°C , Vcc = 5.0V ±10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M416165D-5,5S		M5M416165D-6,6S		M5M416165D-7,7S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		64		64		64	ms
tREF *	Refresh cycle time		128		128		128	ms
tRP	$\overline{RAS}$ high pulse width	30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note16)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width	8		10		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low (Note17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low	0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low (Note18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low	8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low	8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low (Note19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low (Note19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data (Note20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data (Note20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data (Note20)	13		15		20		ns
tWED	Delay time, $\overline{W}$ low to data (Note20)	13		15		20		ns
tT	Transition time (Note21)	1	50	1	50	1	50	ns

* : Applicable to self refresh version (M5M416165DXX-5S,-6S,-7S:option) only

Note 14: The timing requirements are assumed t_T =2ns.

15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

16: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.

17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

18: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

19: Either t_{DZC} or t_{DZO} must be satisfied.

20: Either t_{RDD} or t_{CDD} or t_{ODD} or t_{WED} must be satisfied.

21: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M416165D-5,5S		M5M416165D-6,6S		M5M416165D-7,7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 22)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time	25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time	15		18		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M416165D-5,5S		M5M416165D-6,6S		M5M416165D-7,7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	8		10		13		ns
tWP	Write pulse width	8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M416165D-5,5S		M5M416165D-6,6S		M5M416165D-7,7S		
		Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width	75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width	38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low (Note24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for EDO mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

EDO Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle, , Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M416165D-5,5S		M5M416165D-6,6S		M5M416165D-7,7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	EDO mode read/write cycle time (Note26)	20		25		30		ns
t_{HPRWC}	EDO mode read write / read modify write cycle time	57		66		79		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low	5		5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note27)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note28)	8	13	10	16	10	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note24)	45		52		62		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until CAS access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	52		62		72		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	62		72		82		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	30		35		40		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective EDO mode cycle.

26: $t_{HPC(min)}$ is specified in the case of read-only and early write-only in EDO mode.

27: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

28: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M416165D-5,-5S		M5M416165D-6,-6S		M5M416165D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	17		17		22		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

TIMING REQUIREMENTS (Ta=0 ~ 70°C , Vcc=5.0V±10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M416165D-5S		M5M416165D-6S		M5M416165D-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		µs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

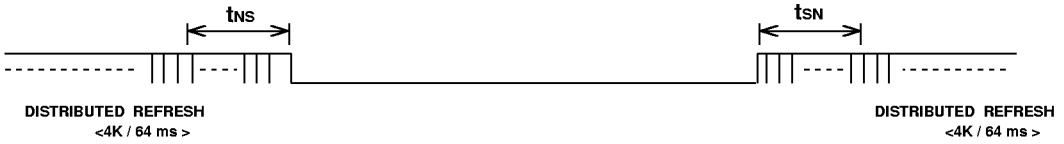
Note 14: The timing requirements are assumed t_T =2ns.

15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

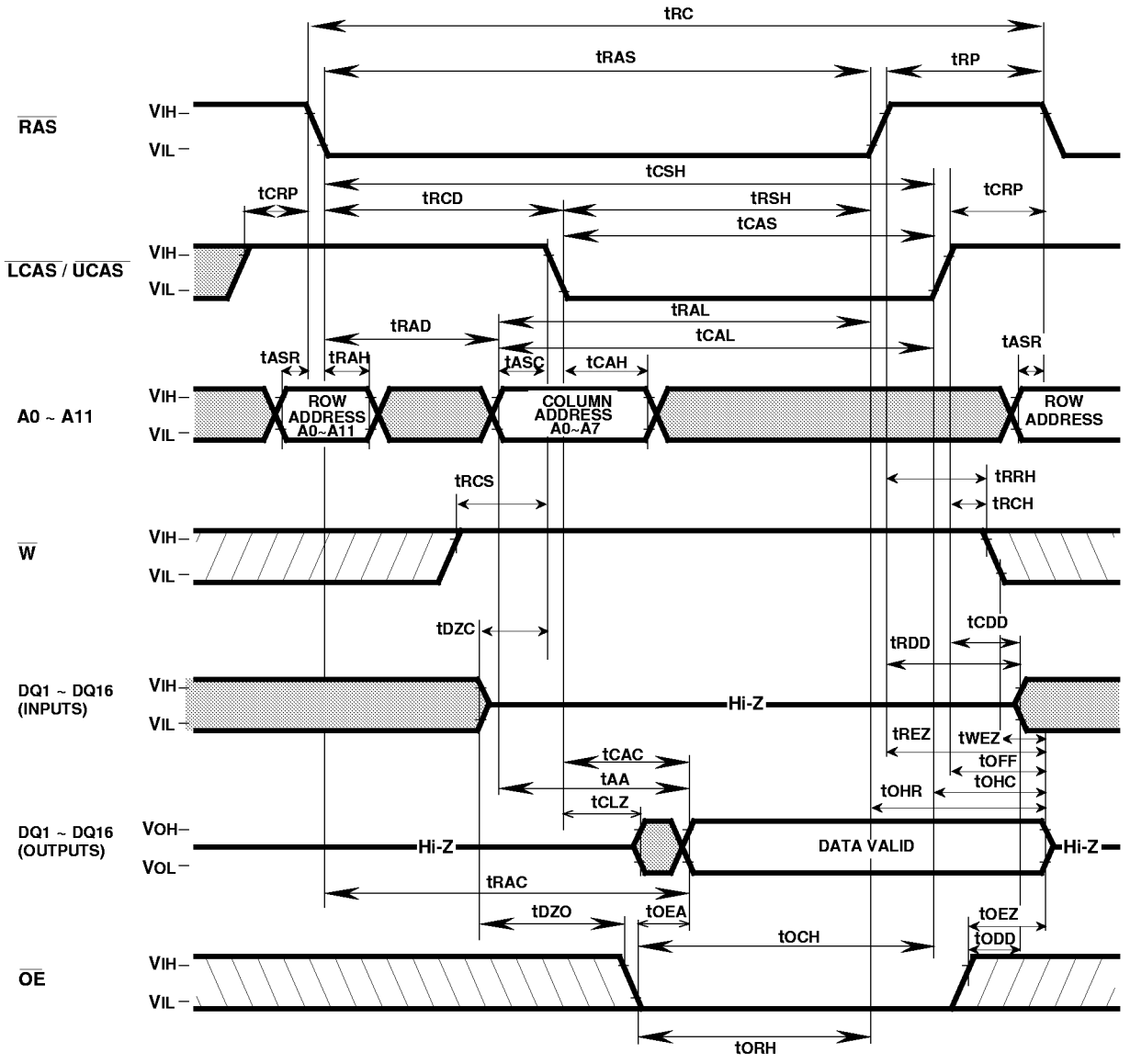
The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of $t_{NS} \leq 64$ ms and $t_{SN} \leq 64$ ms.



(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of t_{NS} + $t_{SN} \leq 64$ ms.

Timing Diagrams (Note 30)
Read Cycle

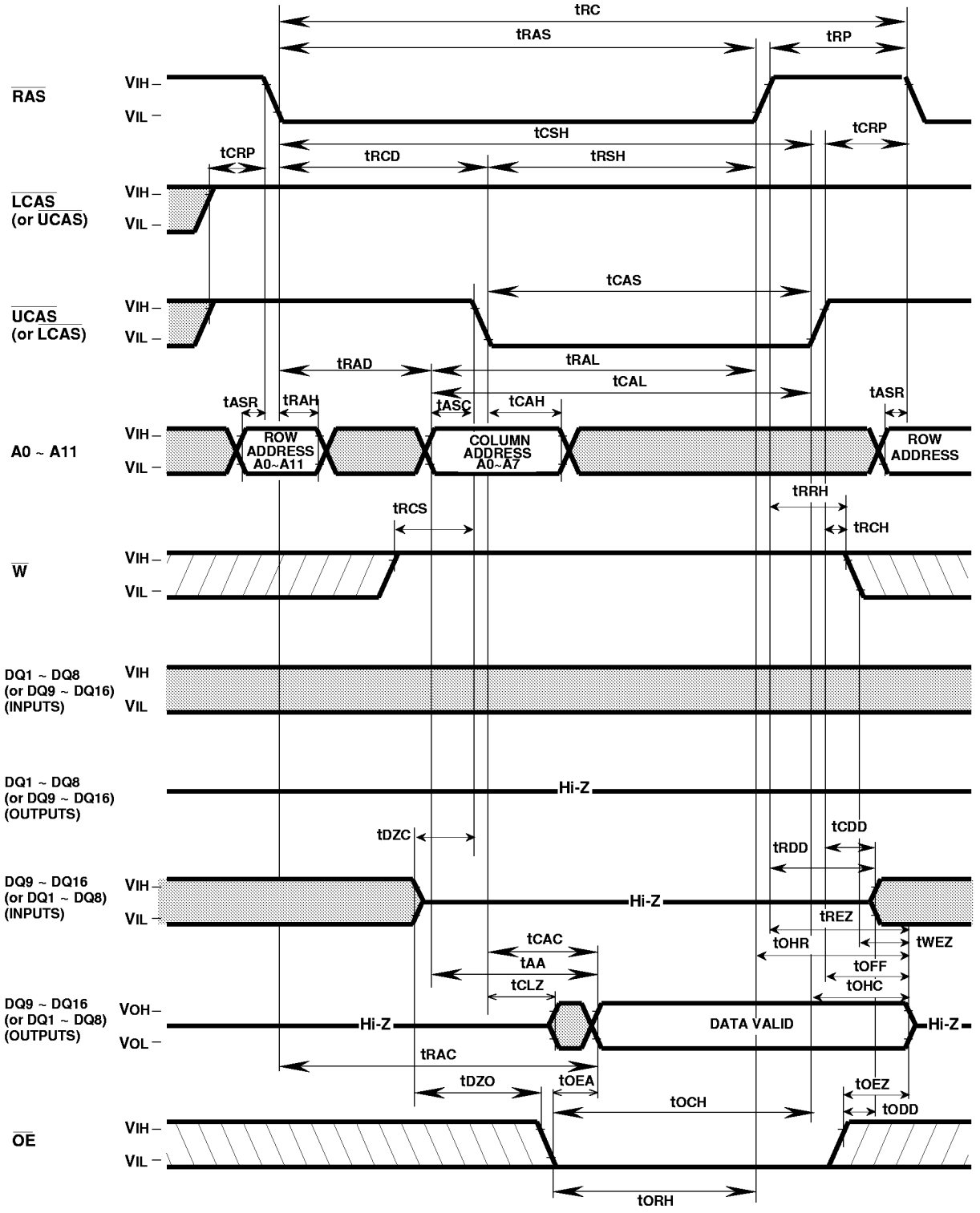


Note 30

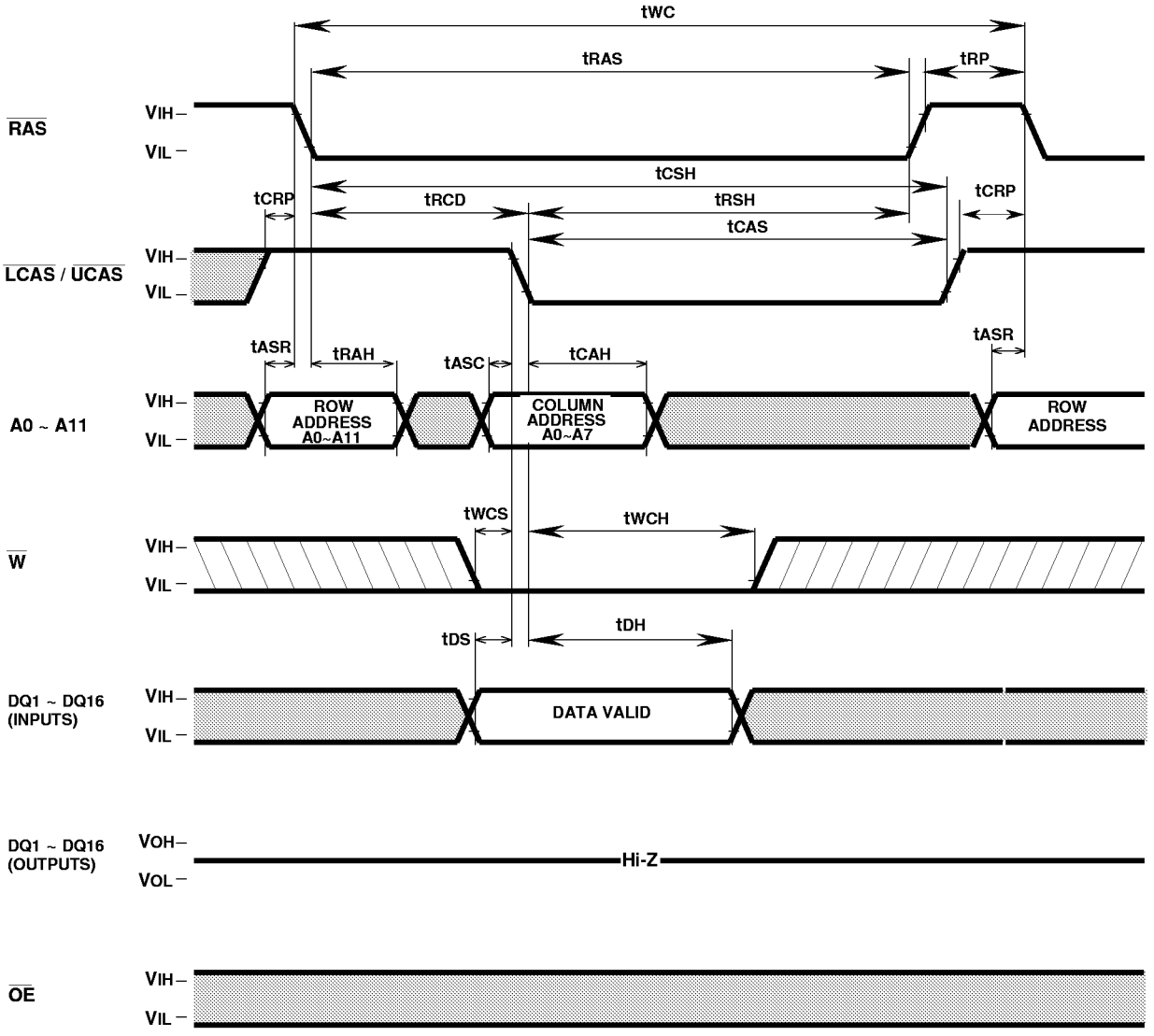
Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

Indicates the invalid output.

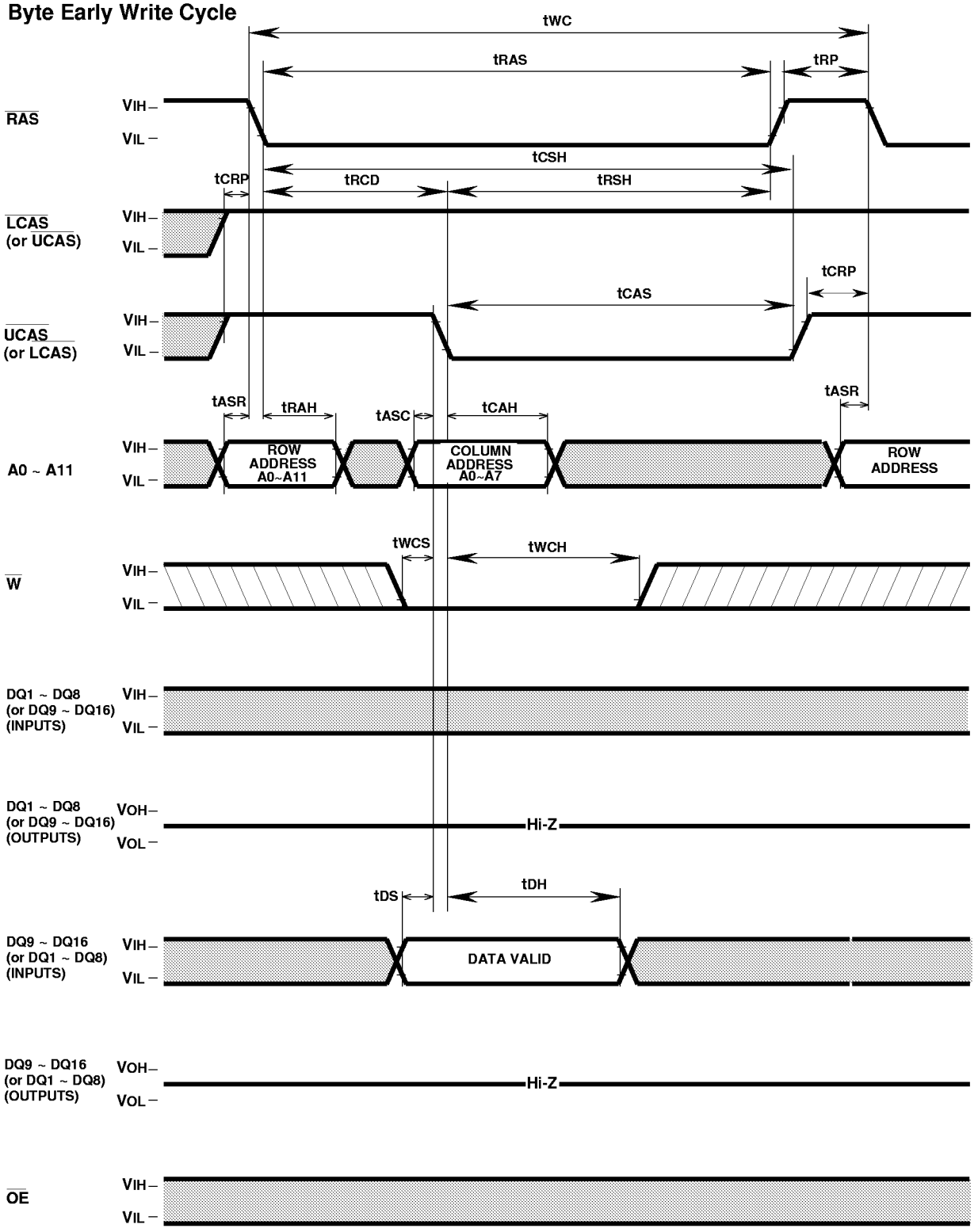
Byte Read Cycle



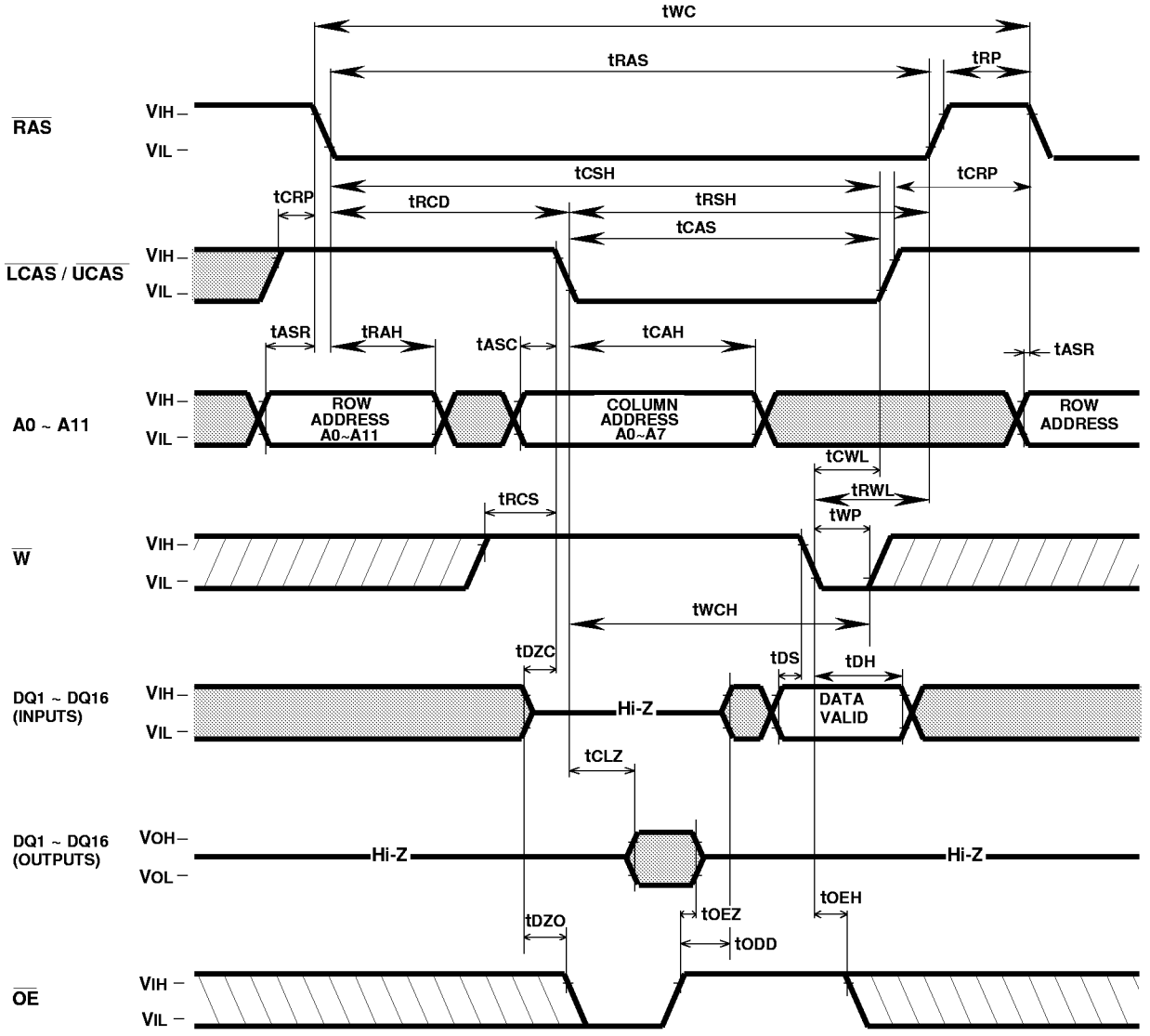
Early Write Cycle



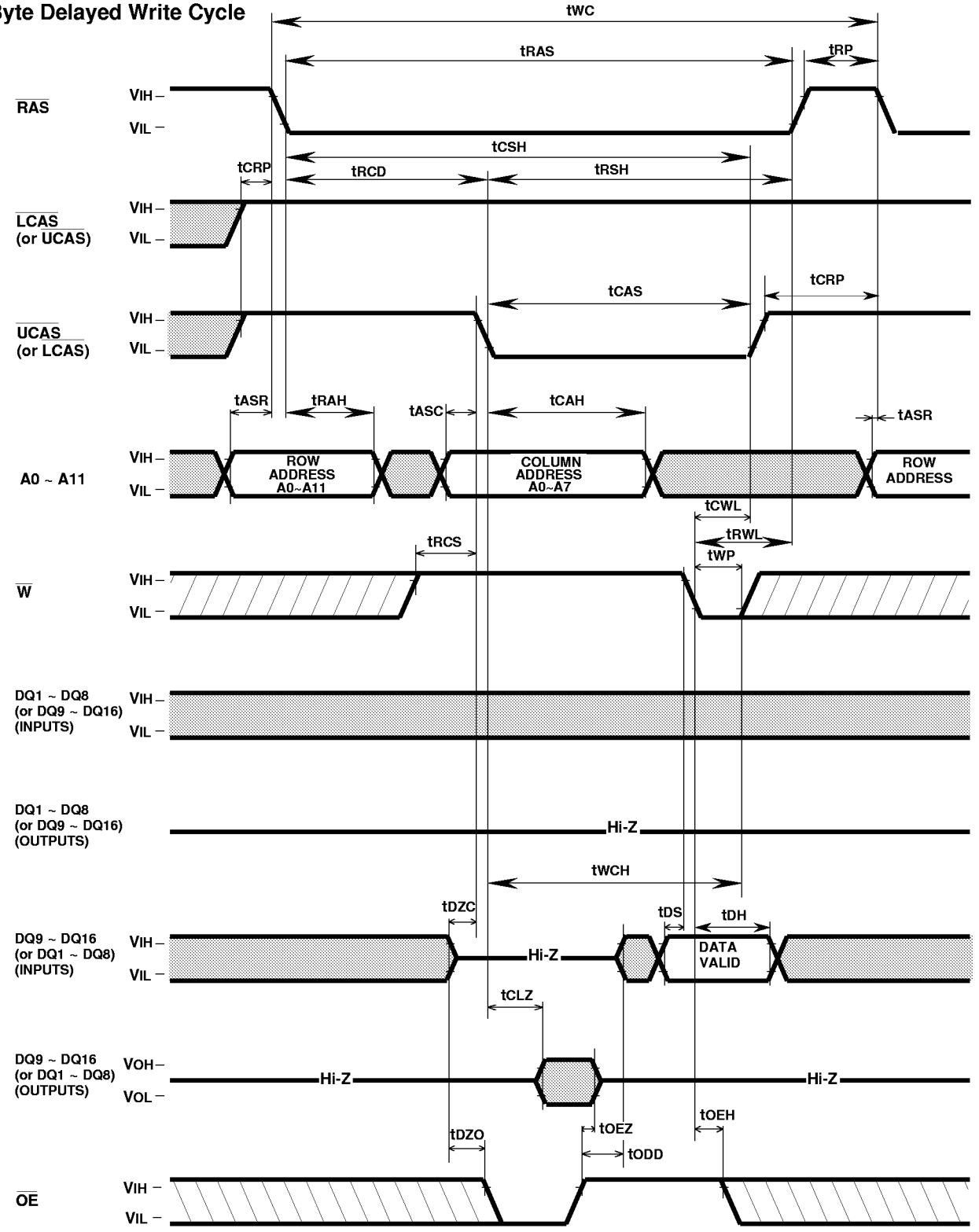
Byte Early Write Cycle



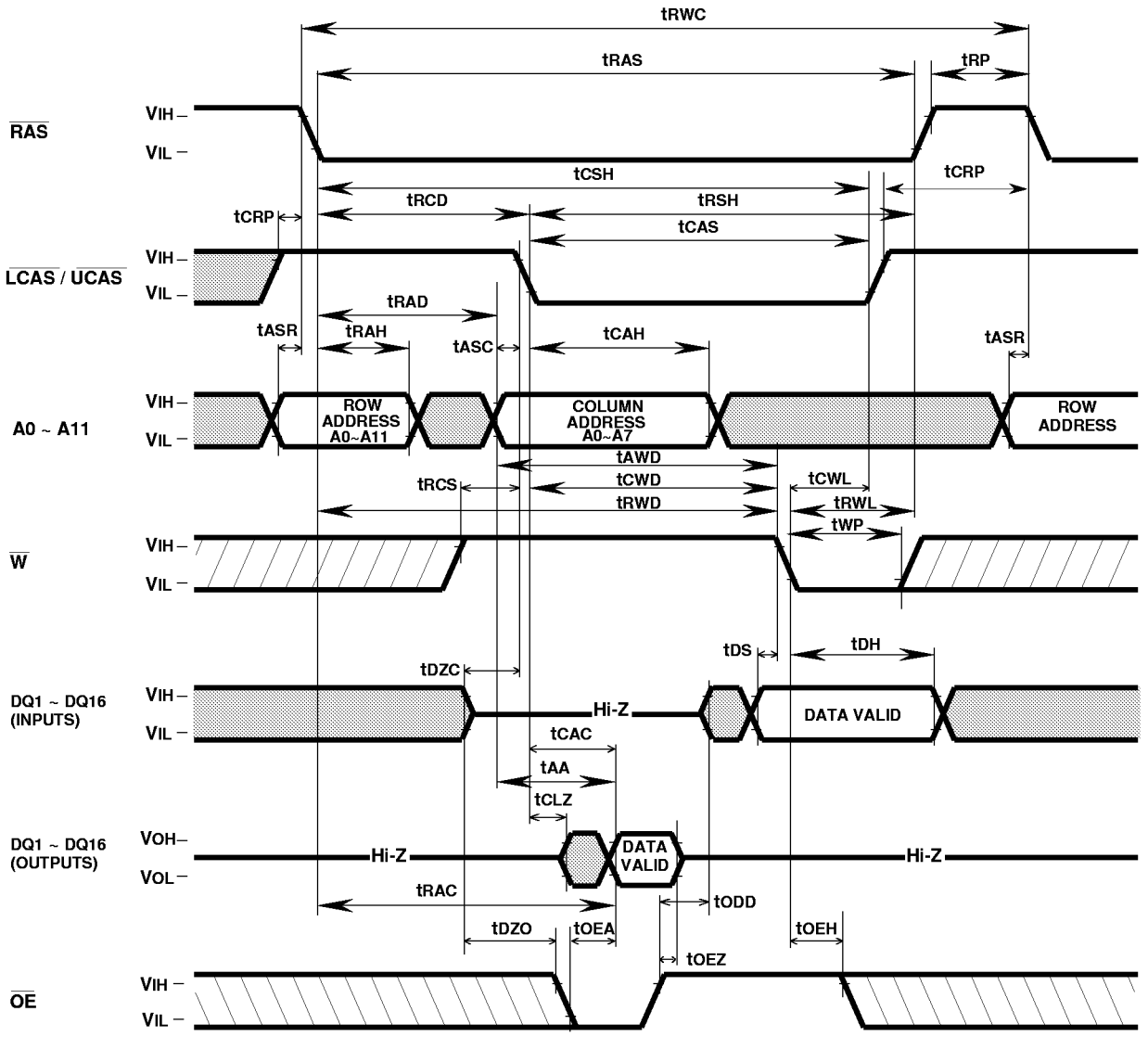
Delayed Write Cycle



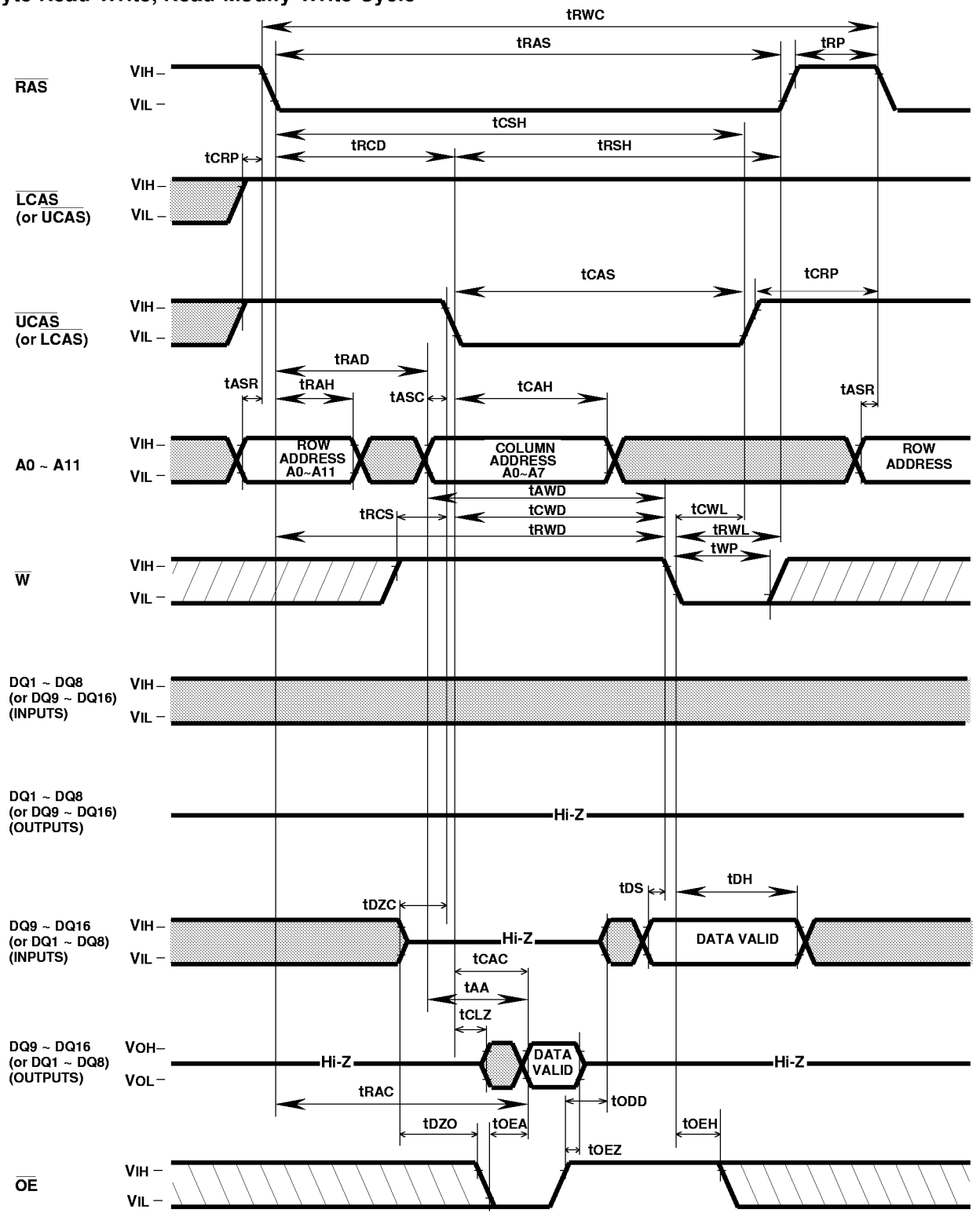
Byte Delayed Write Cycle



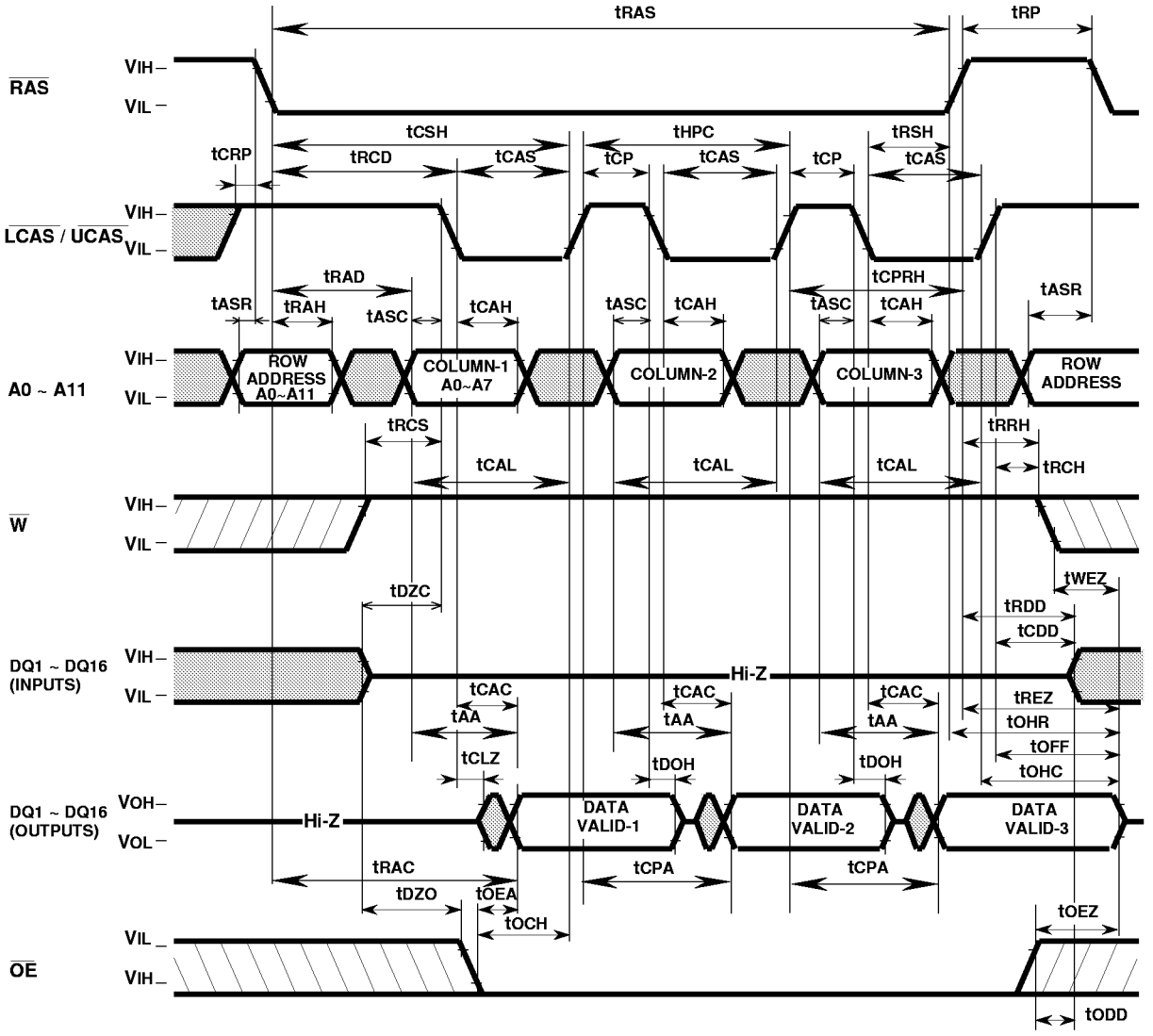
Read-Write, Read-Modify-Write Cycle



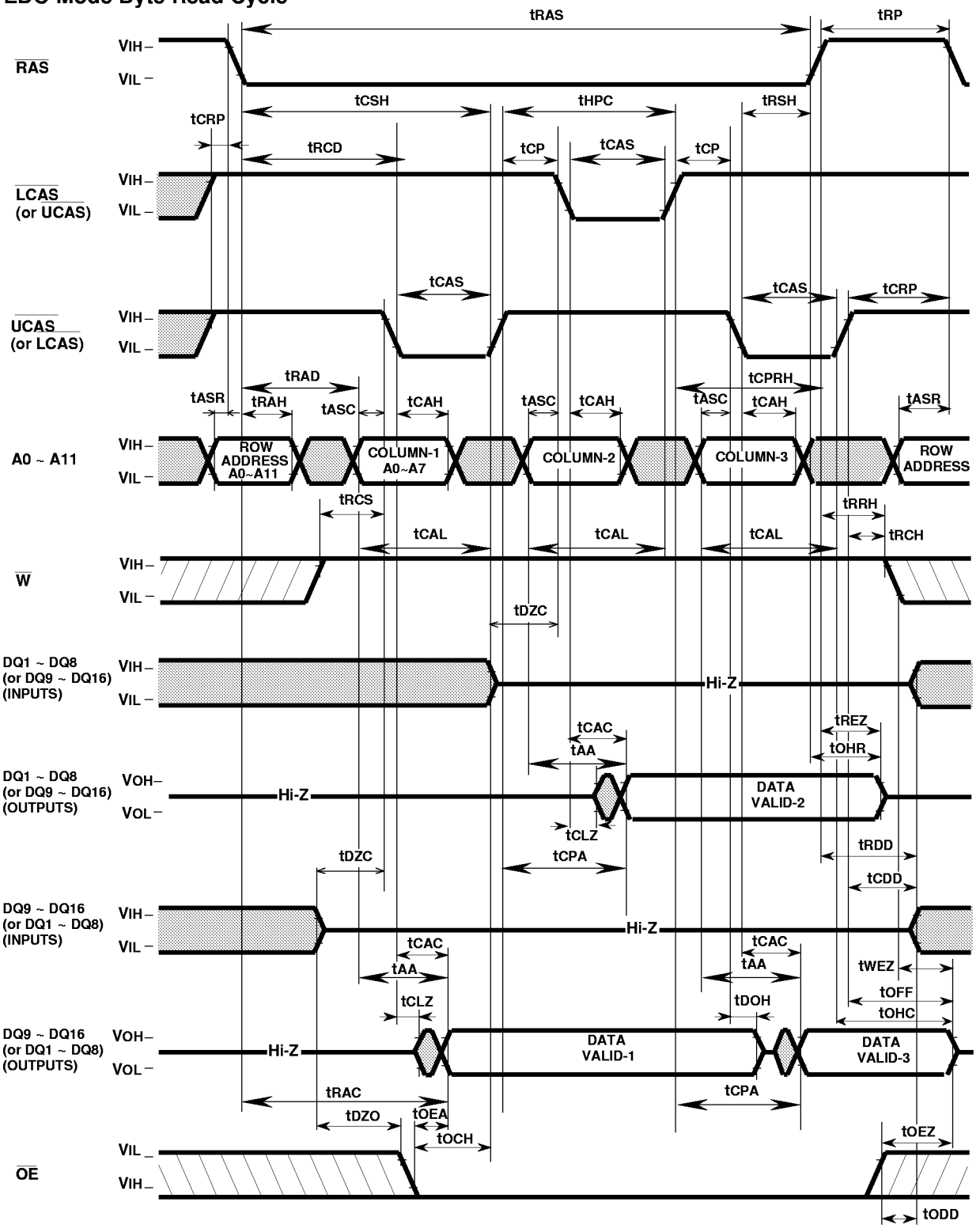
Byte Read-Write, Read-Modify-Write Cycle



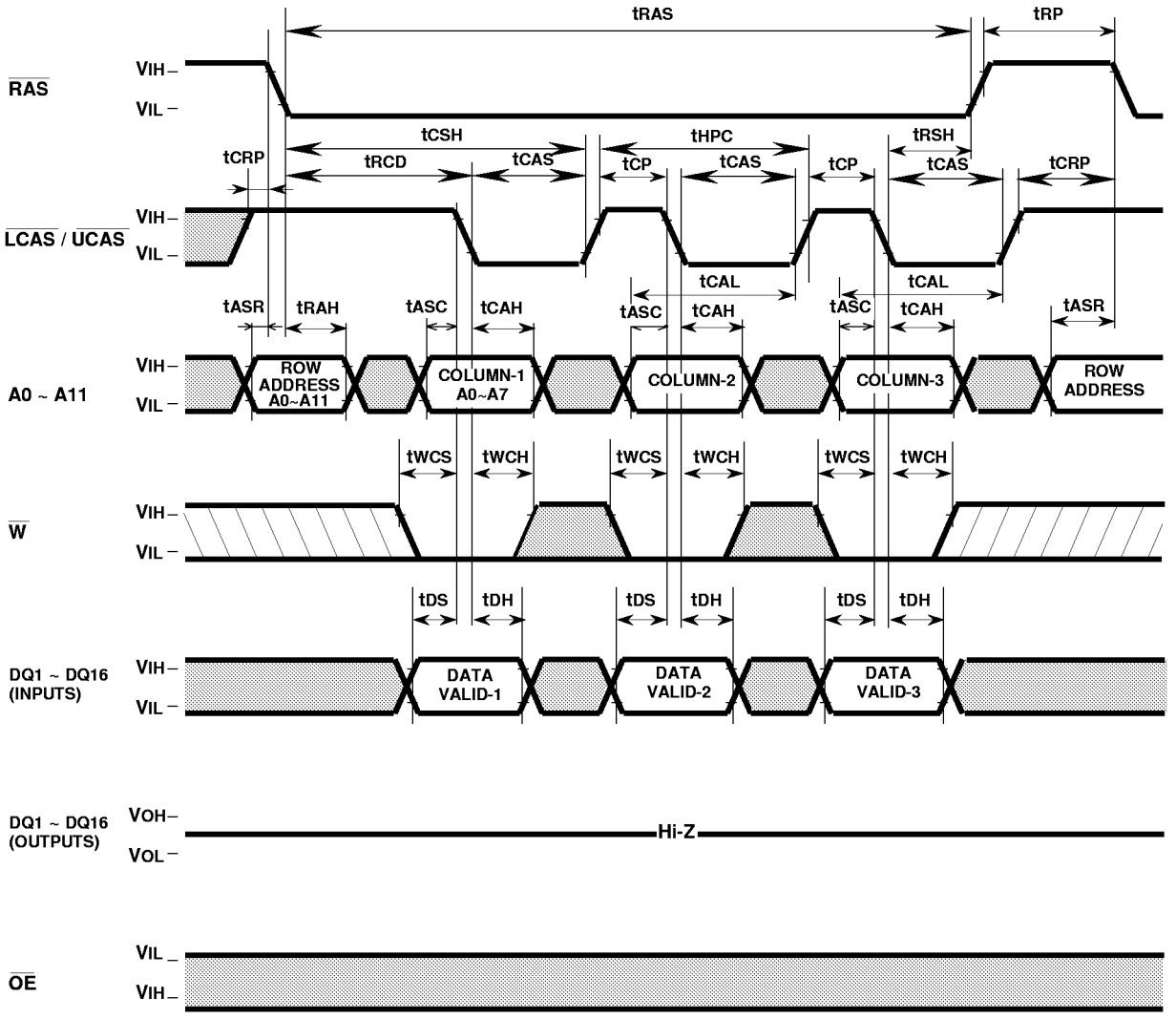
EDO Mode Read Cycle



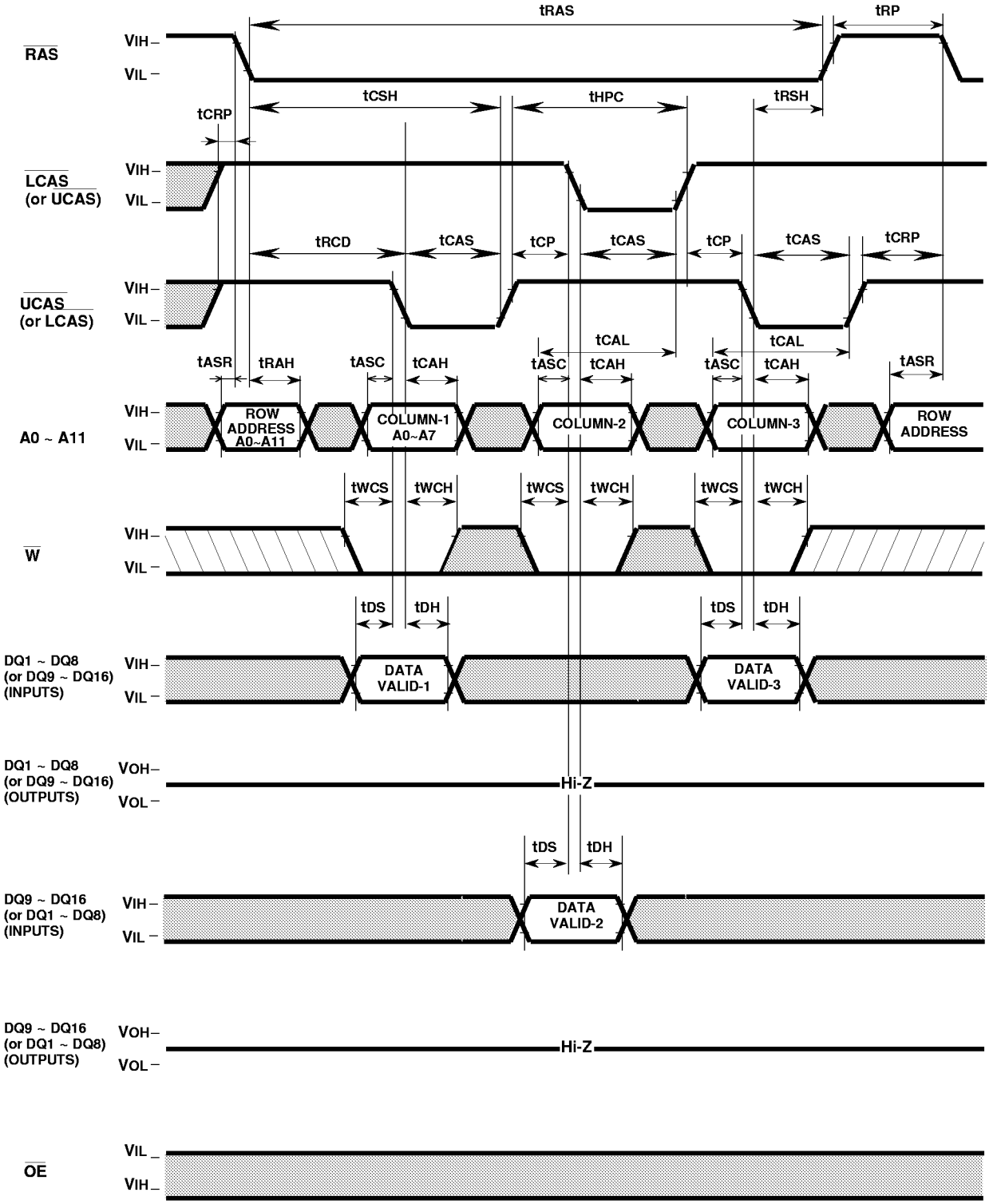
EDO Mode Byte Read Cycle



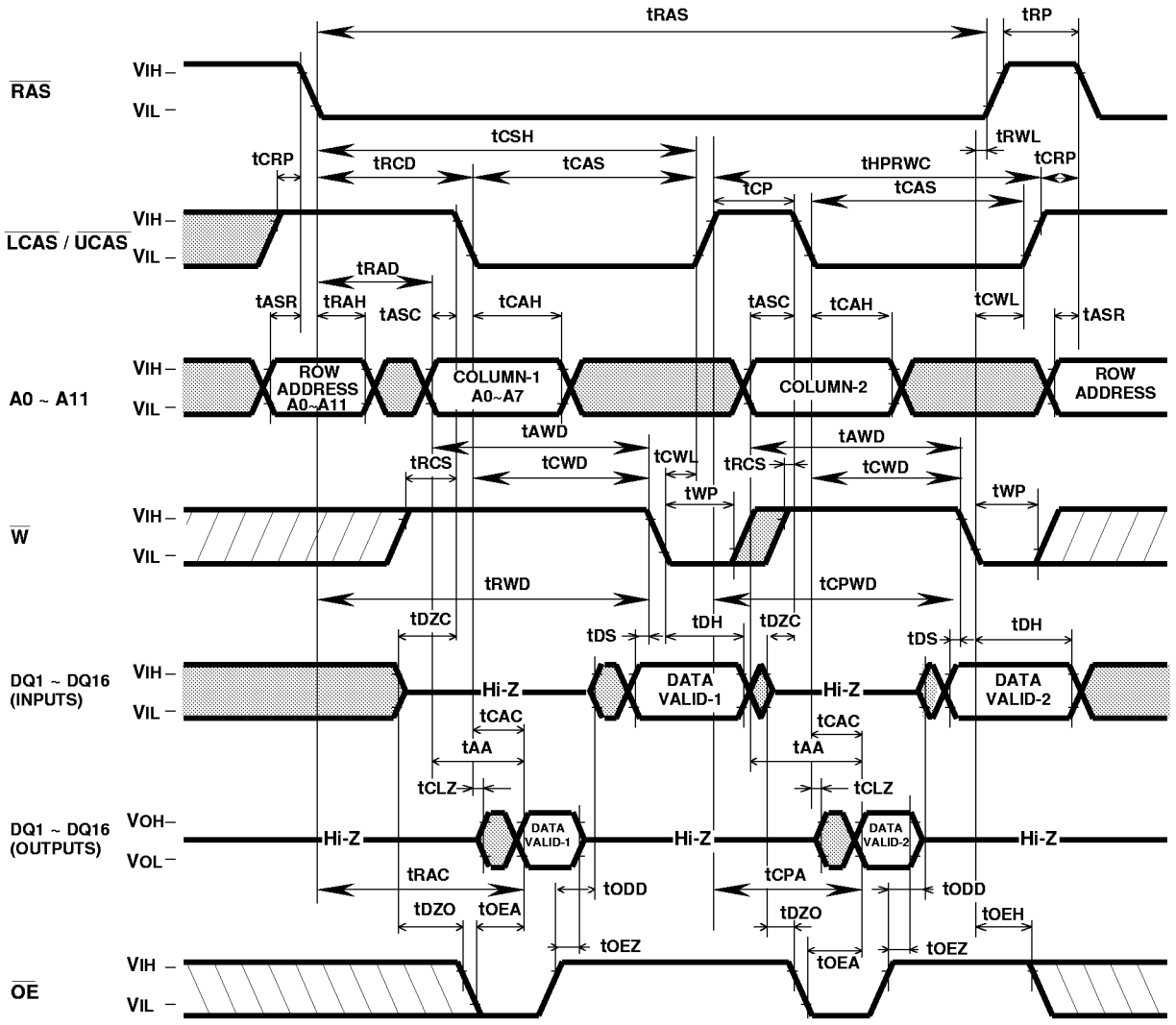
EDO Mode Early Write Cycle



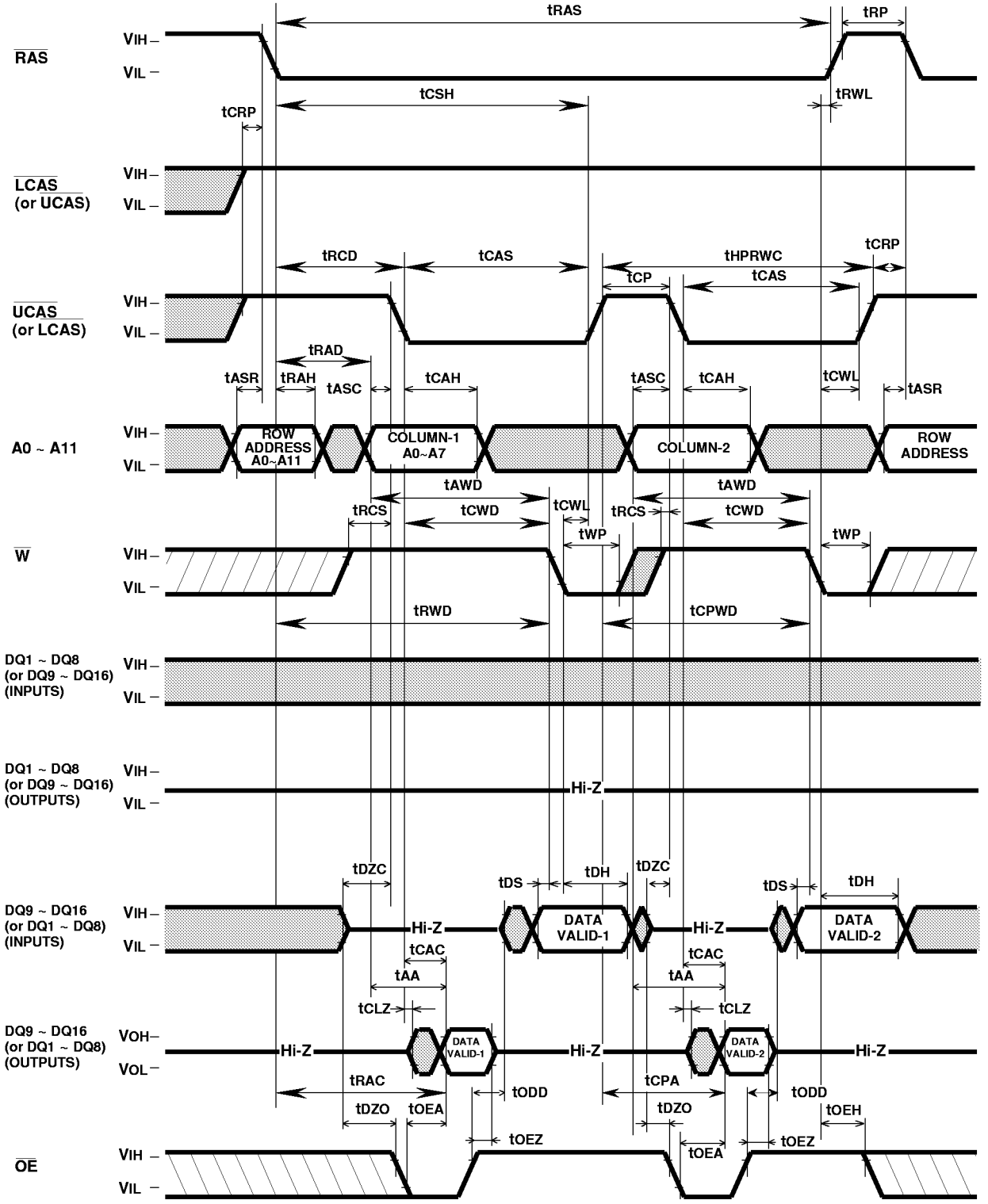
EDO Mode Byte Early Write Cycle



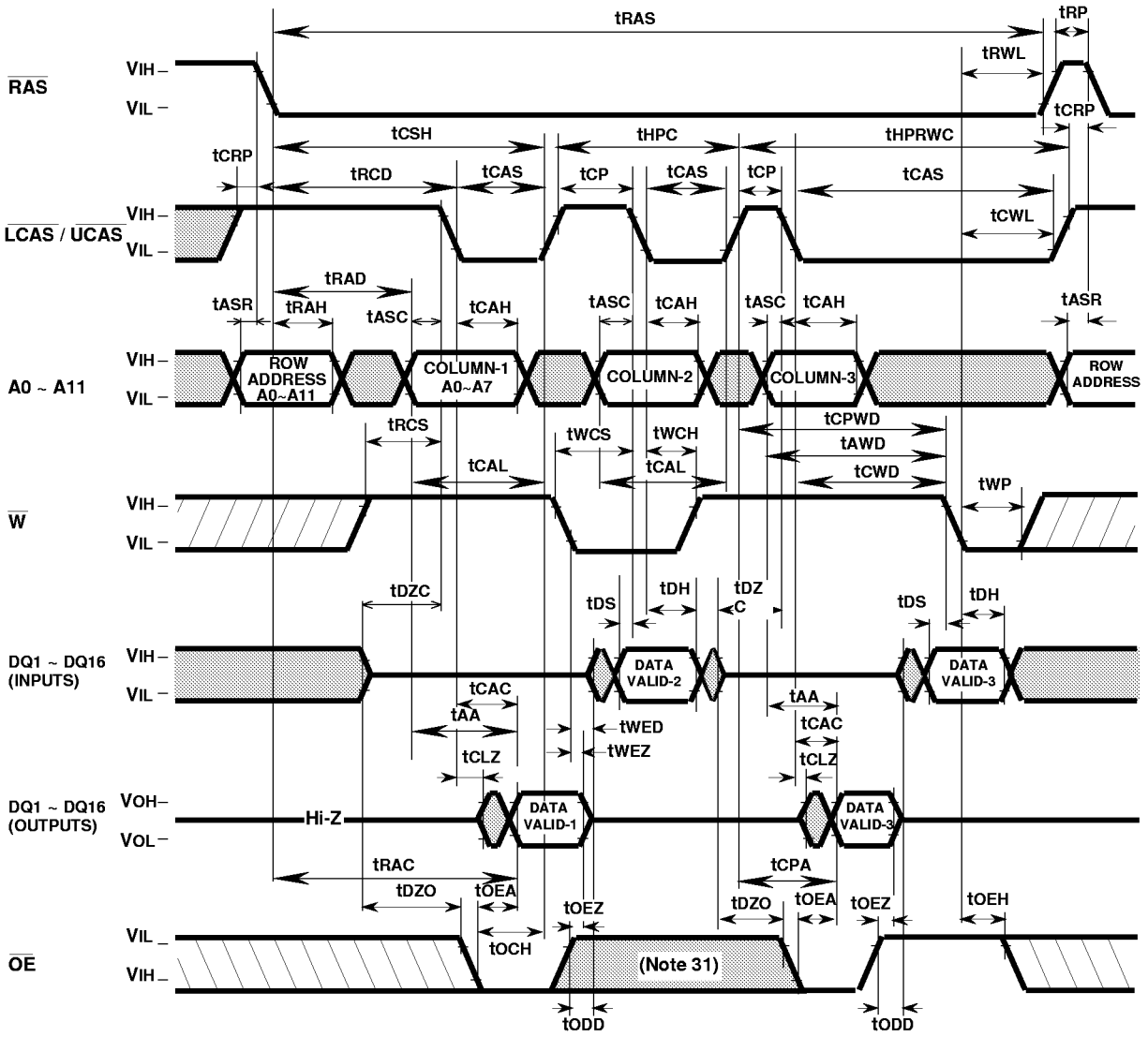
EDO Mode Read-Write,Read-Modify-Write Cycle



EDO Mode Byte Read-Write,Read-Modify-Write Cycle

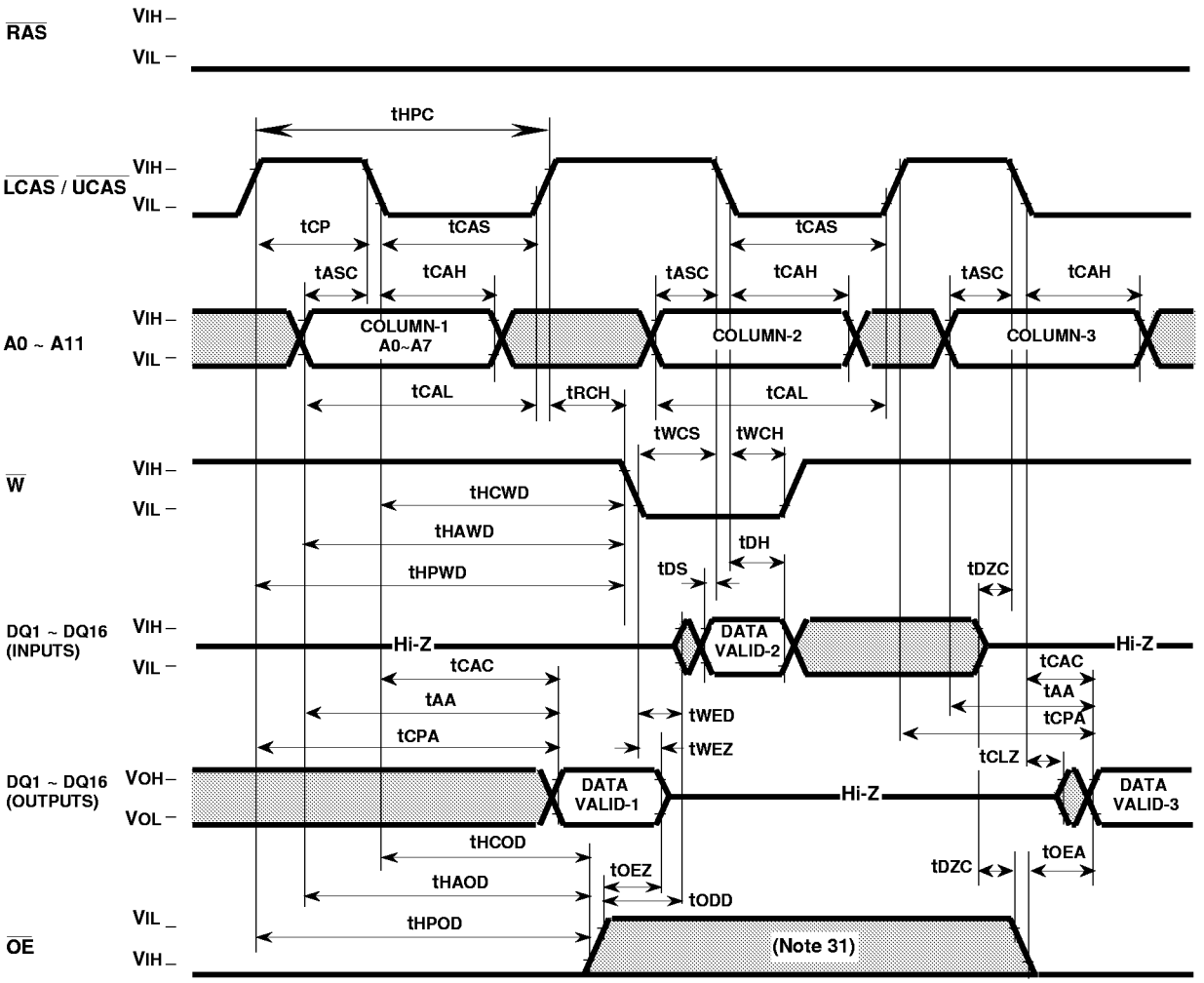


EDO Mode Mix Cycle (1) (Note 31)



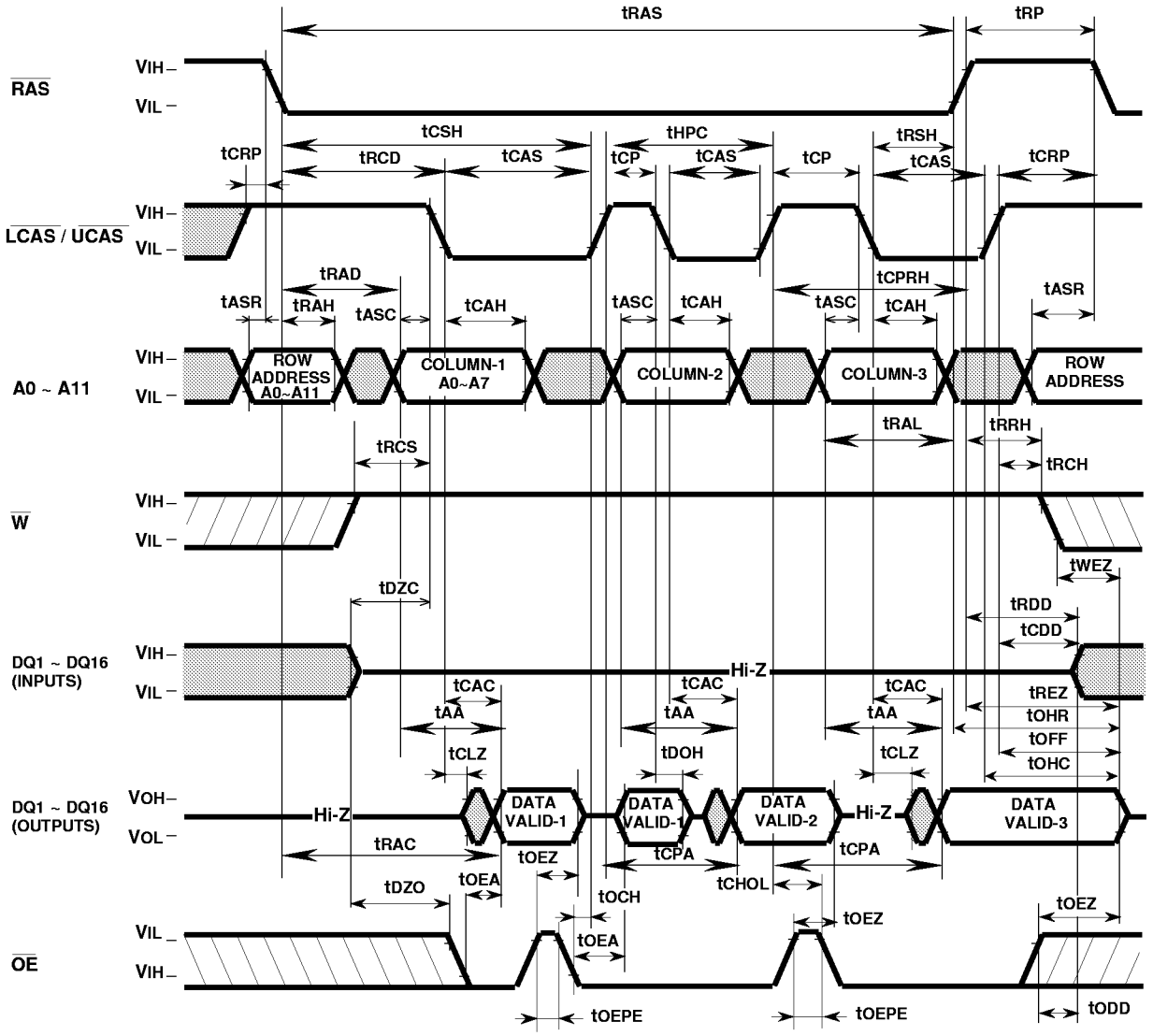
(Note 31: $\overline{OE}$ =L ; $\overline{W}$ Hi-Z control
$\overline{OE}$ =H ; $\overline{OE}$ Hi-Z control)

EDO Mode Mix Cycle (2) (Note 31)

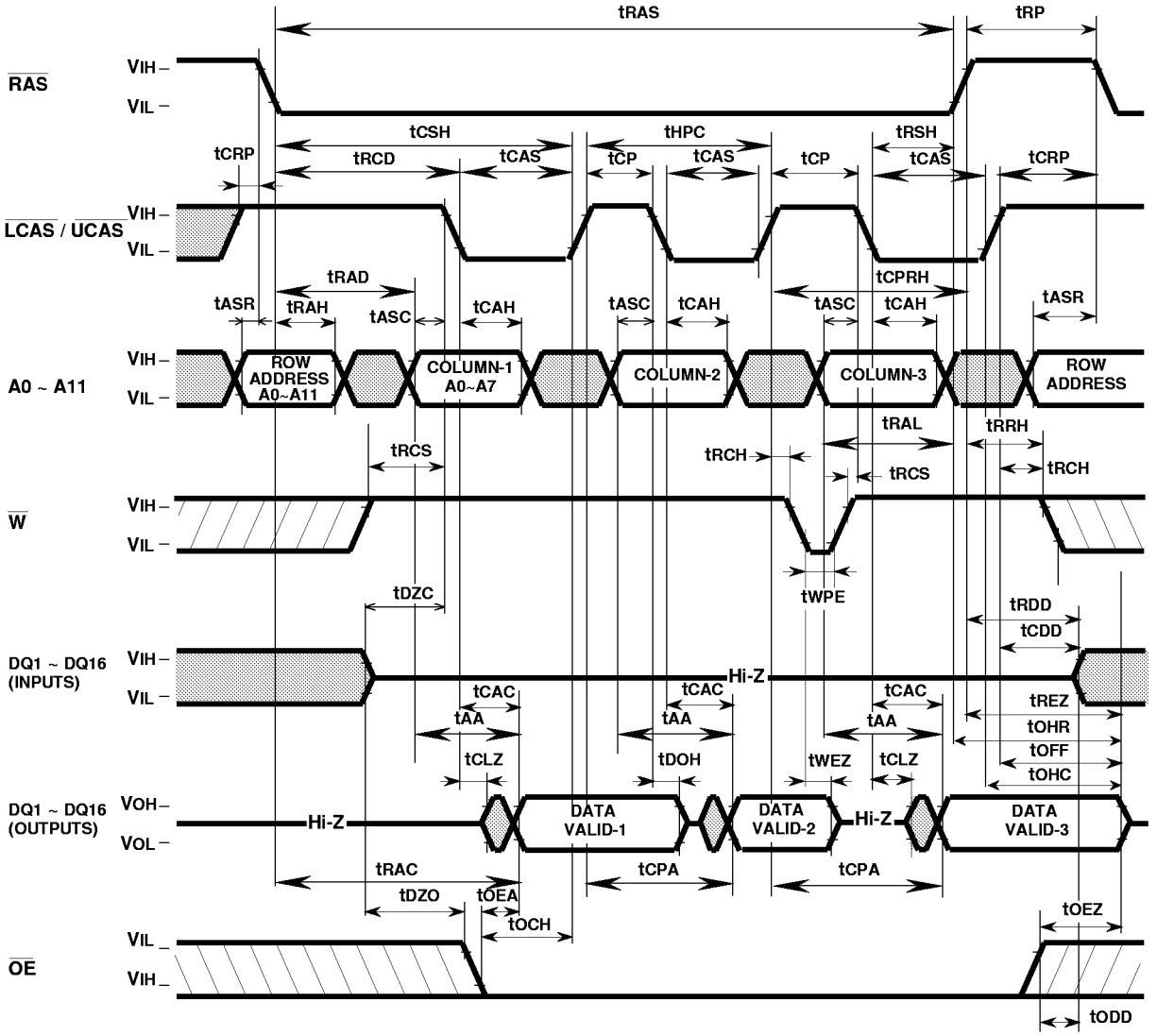


(Note 31: $\overline{OE}$ =L ; $\overline{W}$ Hi-Z control
$\overline{OE}$ =H ; $\overline{OE}$ Hi-Z control)

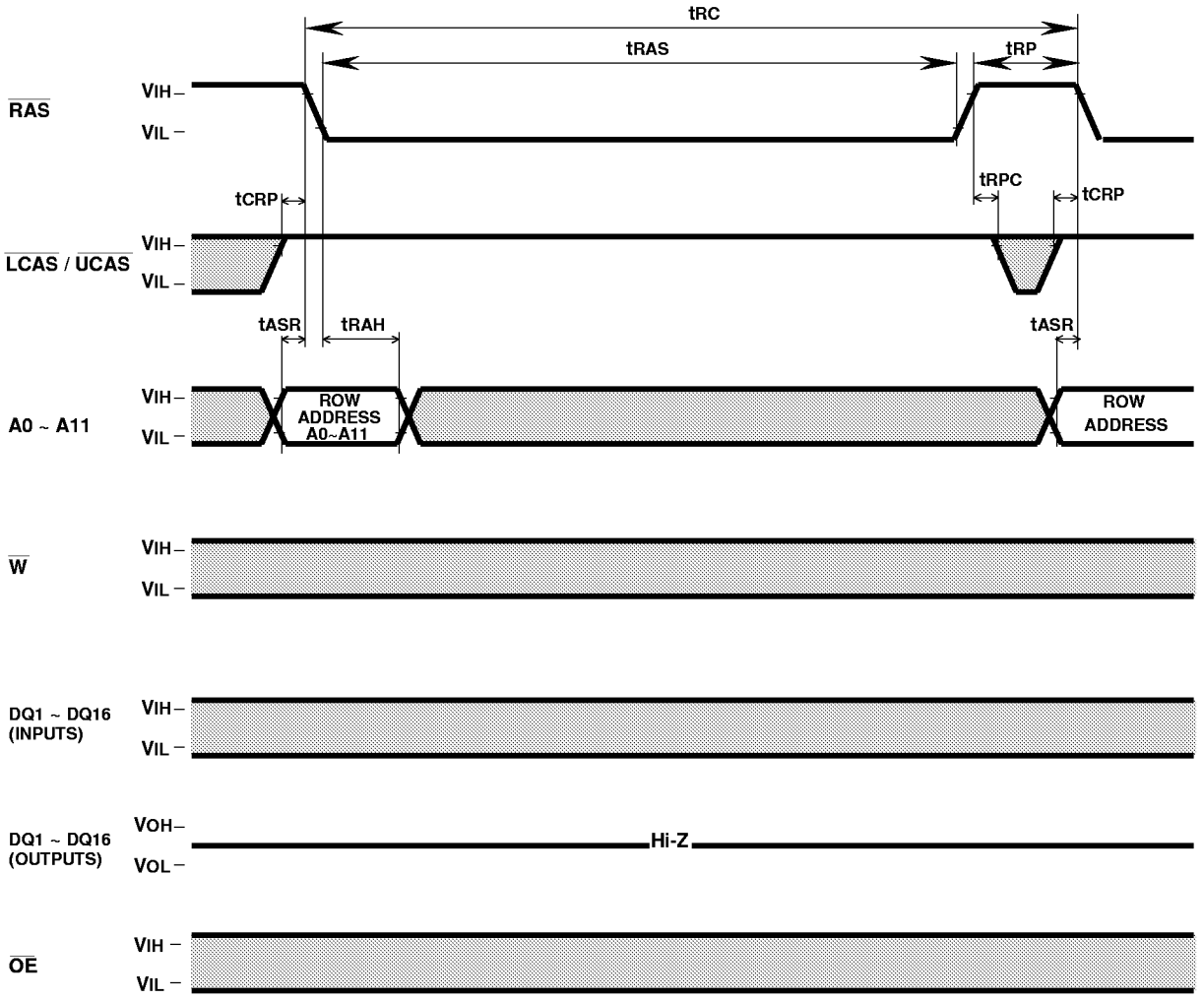
EDO Mode Read Cycle (Hi-Z control by $\overline{OE}$)



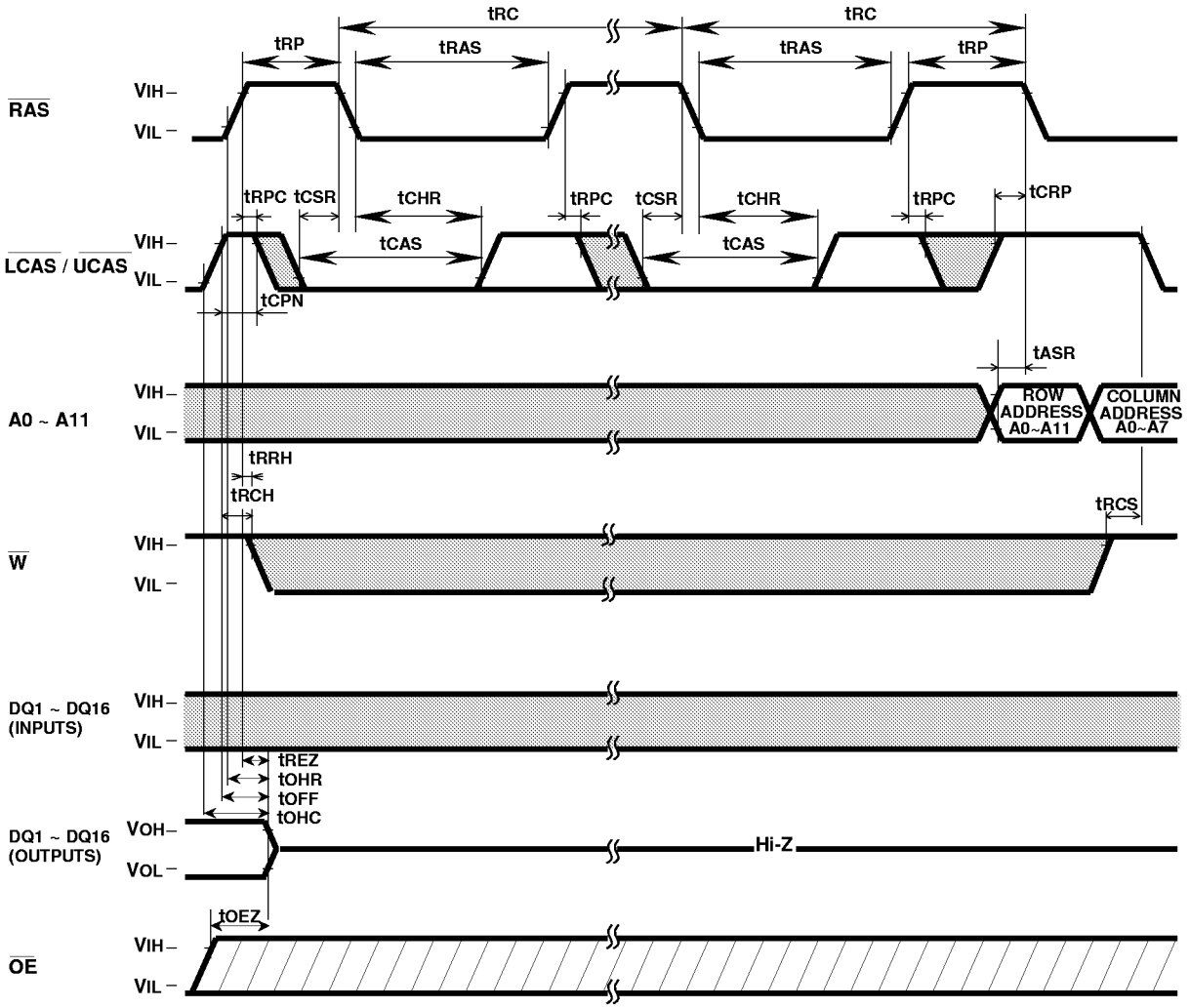
EDO Mode Read Cycle (Hi-Z control by $\overline{W}$)



$\overline{RAS}$-only Refresh Cycle

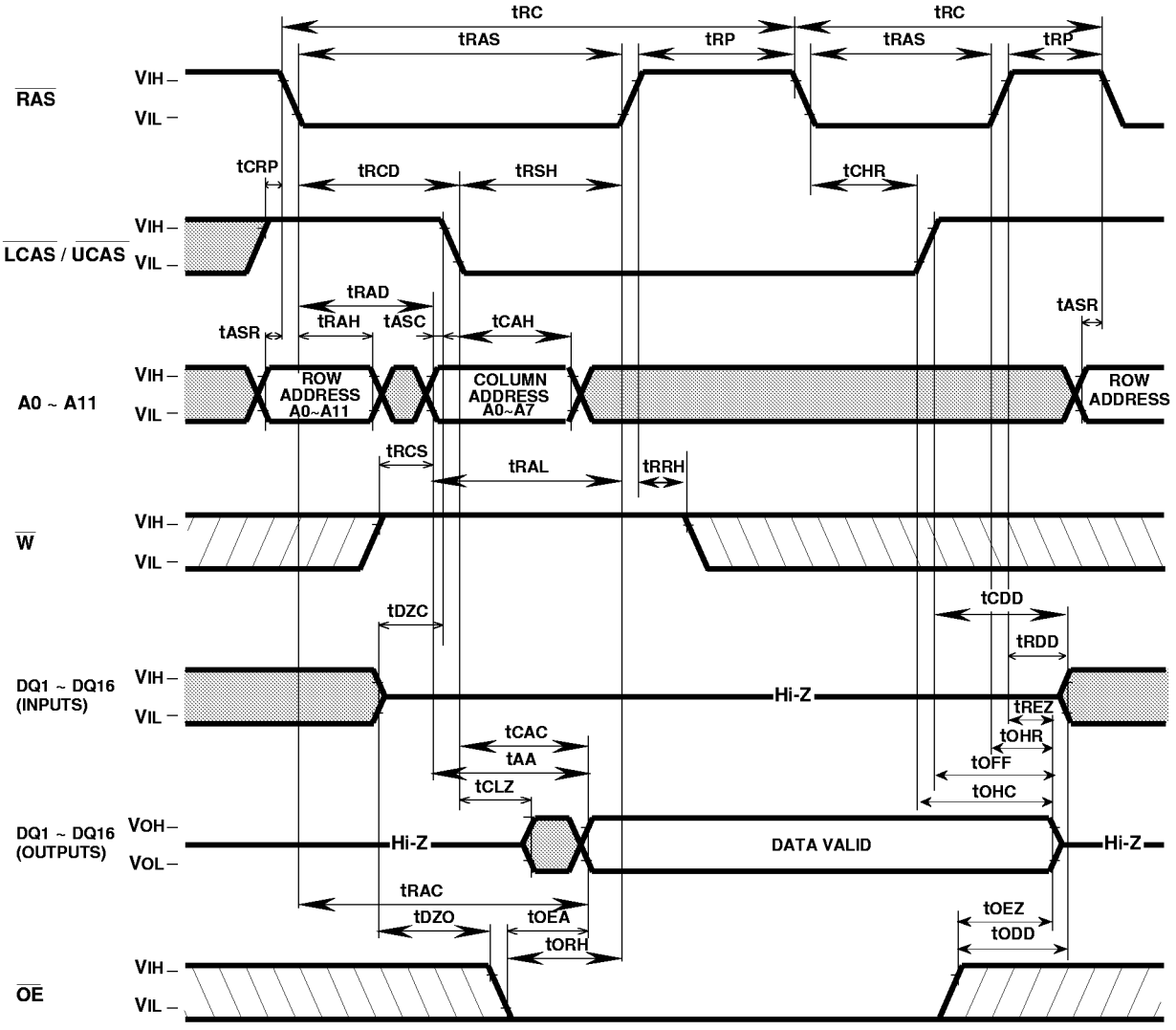


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*



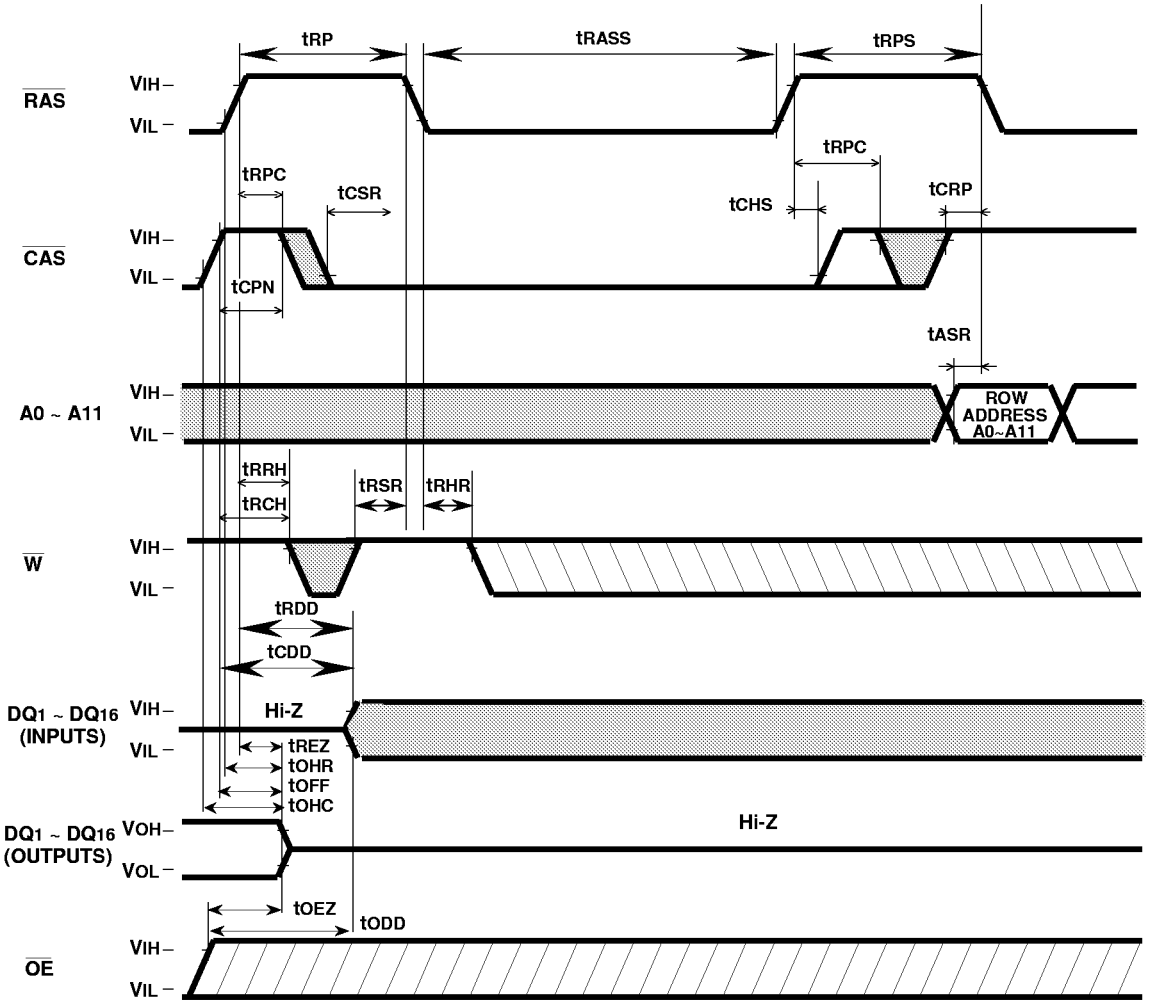
* :Applicable to self refresh version (M5M416165Dxx-5s,-6s,-7s : option) only

Hidden Refresh Cycle (Read) (Note 32)



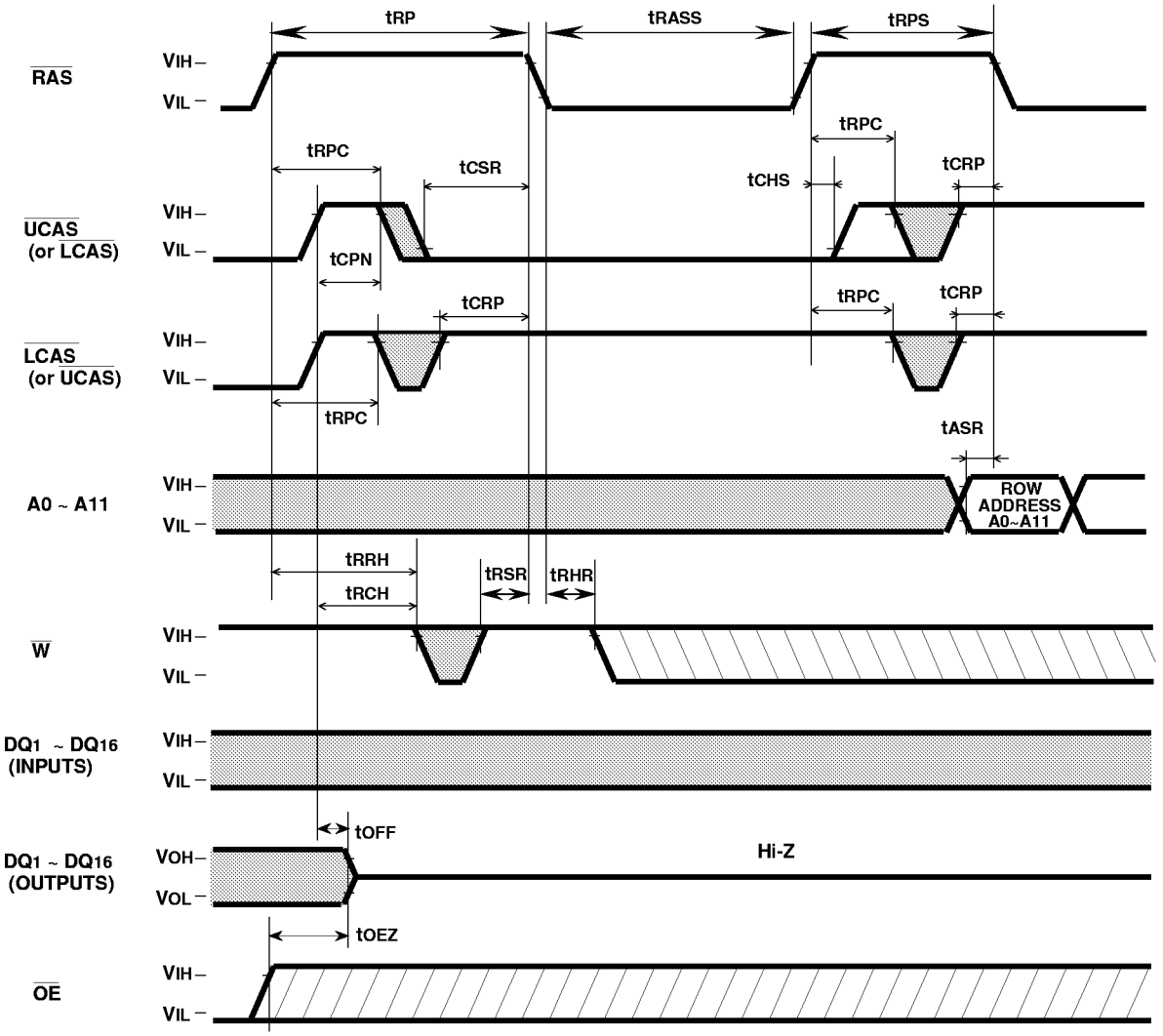
Note 32: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle *



* :Applicable to self refresh version (M5M416165Dxx-5s,-6s,-7s : option) only

Upper (Lower) Self Refresh Cycle *



* :Applicable to self refresh version (M5M416165Dxx-5s,-6s,-7s : option) only