CYPRESS SEMICONDUCTOR

512K x 8 SRAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 30 ns**
- **Low active power**
  - **1.9W (max.)**
- **JEDEC-compatible pinout**
- **32-pin, 0.6-inch-wide DIP package**
- **TTL-compatible inputs and outputs**

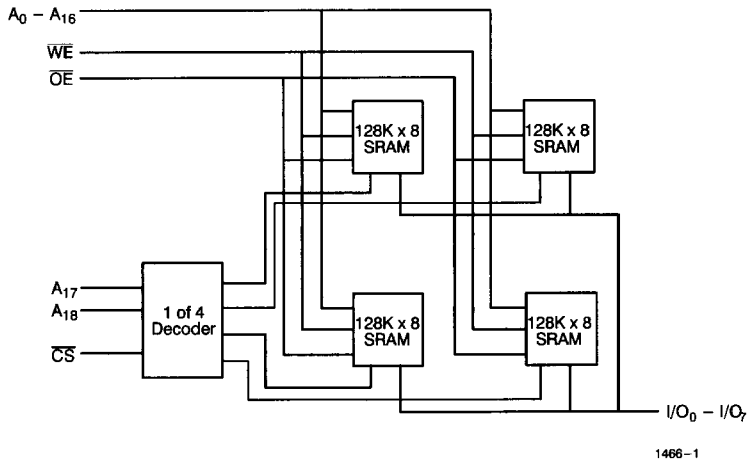
Functional Description

The CYM1466 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 128K x 8 RAMs in ceramic leadless chip carrier packages mounted on a ceramic substrate. A decoder is used to interpret the higher-order addresses (A_{17} and A_{18}) and to select one of the four RAMs.

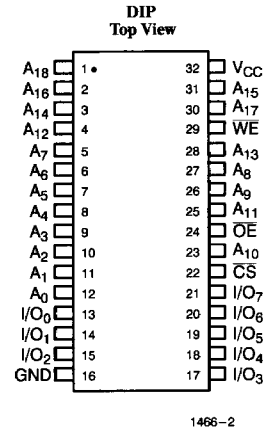
Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select and output enable ($\overline{OE}$) LOW while write enable remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins $(I/O)_0$ through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

		1466-30	1466-35	1466-45	1466-55	1466-70	1466-85	1466-100	1466-120
Maximum Access Time (ns)		30	35	45	55	70	85	100	120
Maximum Operating Current (mA)	Mil	250	250	250	250	250	110	110	110
Maximum Standby Current (mA)	Mil	120	120	120	120	120	15	15	15

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 65°C to +125°C

Supply Voltage to Ground Potential ..... −0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... 0V to V_{CC}

DC Input Voltage ..... −0.3V to V_{CC} +0.3V

Operating Range

Range	Ambient Temperature	V_{CC}
Military	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		1466-30 1466-35 1466-45 1466-55 1466-70 Min.	1466-30 1466-35 1466-45 1466-55 1466-70 Max.	1466-85 1466-100 1466-120 Min.	1466-85 1466-100 1466-120 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	2.4				V
			I_{OH} = − 1.0 mA			2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8.0 mA		0.4			V
			I_{OL} = 2.0 mA				0.4	
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	V_{CC} = Max., $0 \le V_I \le V_{CC}$		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{CC} = Max., $0 \le V_O \le V_{CC}$		−20	+20	−20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_O = 0 mA, $\overline{CS} \le V_{IL}$			250		110	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \ge V_{IH}$, I_O = 0 mA			120		15	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \ge V_{CC}$ − 0.2V, V_{CC} − 0.2V ≤ V_I ≤ 0.2V, I_O = 0 mA			40		10	mA

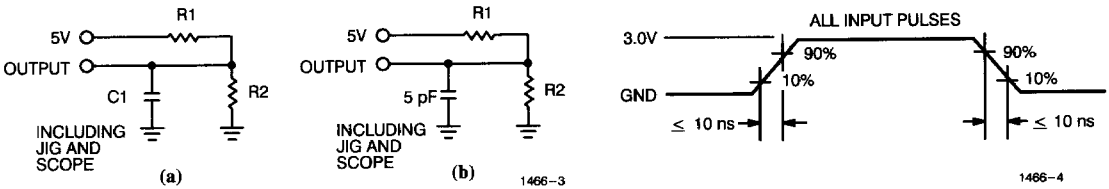
Capacitance[1]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	45	pF
C_{OUT}	Output Capacitance		45	pF

Notes:

1. Tested on a sample basis.

AC Test Loads and Waveforms



9 MODULES

Load Capacitor and Resistor Values

	1466-30 1466-35 1466-45 1466-55 1466-70	1466-85 1466-100 1466-120	Units
C1	30	100	pF
R1	0.481	1.84	kΩ
R2	0.255	1.00	kΩ

Switching Characteristics Over the Operating Range[2]

Parameters	Description	1466-30		1466-35		1466-45		1466-55		1466-70		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	30		35		45		55		70		ns
t_{AA}	Address to Data Valid		30		35		45		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		30		35		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[3]		10		15		20		25		30	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[3]		10		15		20		25		30	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	30		35		45		55		70		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	26		26		30		45		50		ns
t_{AW}	Address Set-Up to Write End	26		26		30		45		50		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up from Write Start	5		5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	18		20		25		35		45		ns
t_{SD}	Data Set-Up to Write End	12		16		20		25		30		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]	0	10	0	15	0	15	0	15	0	15	ns

Switching Characteristics Over the Operating Range[4] (continued)

Parameters	Description	1466-85 Min.	1466-85 Max.	1466-100 Min.	1466-100 Max.	1466-120 Min.	1466-120 Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	85		100		120		ns
t_{AA}	Address to Data Valid		85		100		120	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		85		100		120	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		40		50		60	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]		35		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[3]		35		35		45	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	85		100		120		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	55		90		100		ns
t_{AW}	Address Set-Up to Write End	55		90		100		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up from Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	55		75		85		ns
t_{SD}	Data Set-Up to Write End	35		40		45		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]	0	15	0	35	0	40	ns

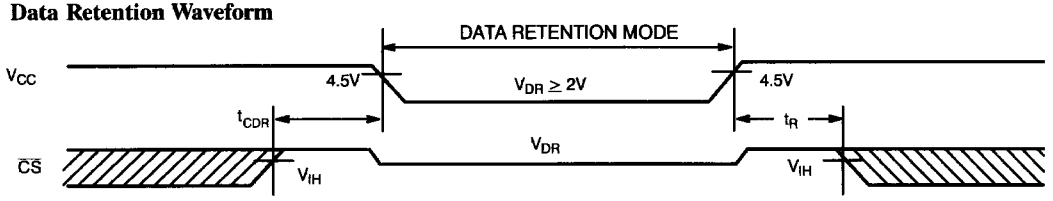
Data Retention Characteristics (L Version Only)

Parameters	Description	Test Conditions	1466-30, 1466-35, 1466-45, 1466-55, 1466-70 Min.	1466-30, 1466-35, 1466-45, 1466-55, 1466-70 Max.	1466-85, 1466-100, 1466-120 Min.	1466-85, 1466-100, 1466-120 Max.	Units
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{DR} = 3.0V$		6000		1000	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time		0		0		ns
t_R[4]	Operation Recovery Time		t_{RC}		t_{RC}		ns

Notes:

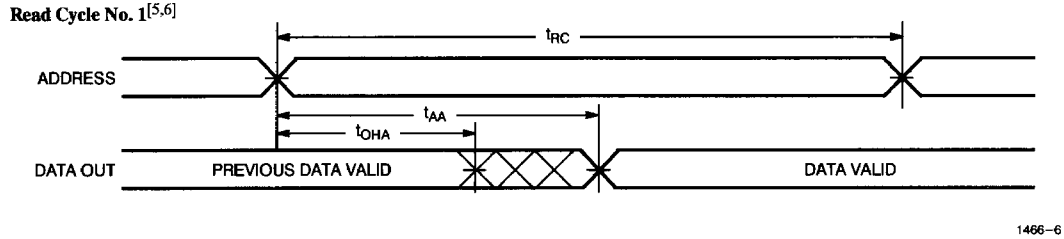
2. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance.
3. $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
4. Guaranteed, not tested.
5. $\overline{WE}$ is HIGH for the read cycle.
6. Device is continuously selected, $\overline{CS} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remians in a high-impedance state.

Data Retention Waveform

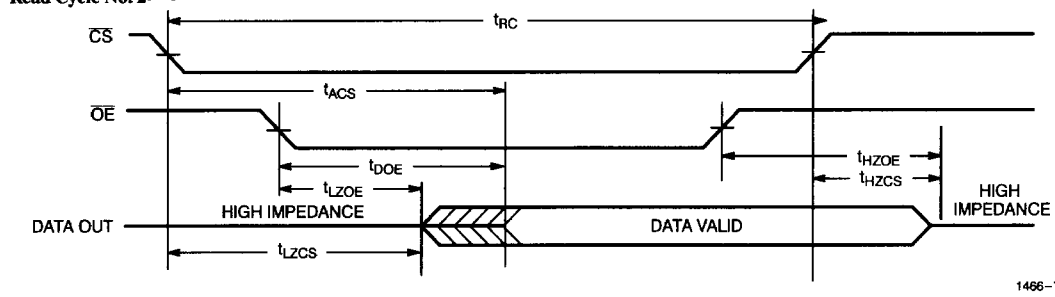


Switching Waveforms

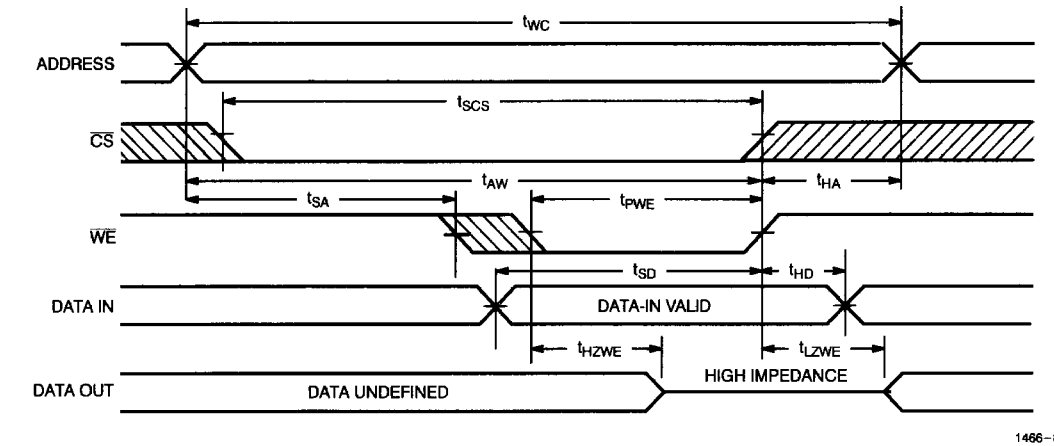
Read Cycle No. 1[5,6]



Read Cycle No. 2[5,7]

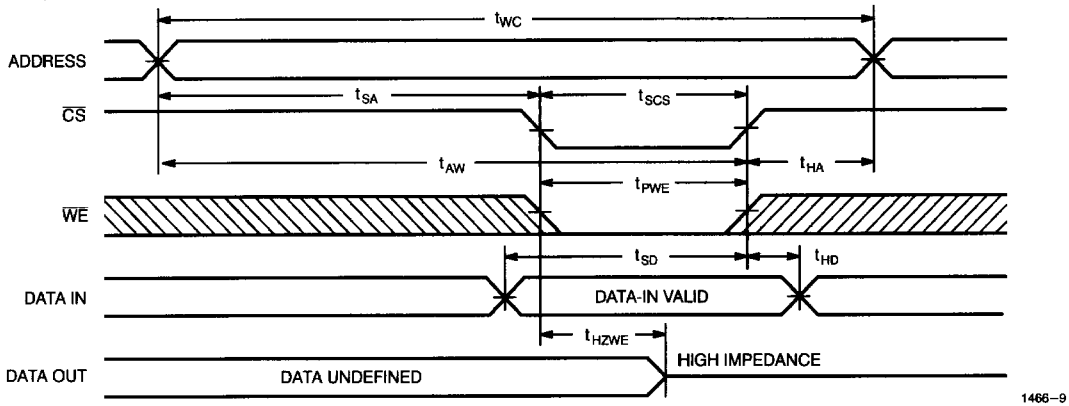


Write Cycle No. 1 ($\overline{WE}$ Controlled)[8]



Switching Waveforms (continued)[8,9]

Write Cycle No. 2 ($\overline{CS}$ Controlled)



Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$		
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CYM1466HD-30M	HD12	Military
	CYM1466LHD-30M	HD12	
	CYM1466HD-30MB	HD12	
	CYM1466LHD-30MB	HD12	
35	CYM1466HD-35M	HD12	Military
	CYM1466LHD-35M	HD12	
	CYM1466HD-35MB	HD12	
	CYM1466LHD-35MB	HD12	
45	CYM1466HD-45M	HD12	Military
	CYM1466LHD-45M	HD12	
	CYM1466HD-45MB	HD12	
	CYM1466LHD-45MB	HD12	
55	CYM1466HD-55M	HD12	Military
	CYM1466LHD-55M	HD12	
	CYM1466HD-55MB	HD12	
	CYM1466LHD-55MB	HD12	
70	CYM1466HD-70M	HD12	Military
	CYM1466LHD-70M	HD12	
	CYM1466HD-70MB	HD12	
	CYM1466LHD-70MB	HD12	
85	CYM1466HD-85M	HD12	Military
	CYM1466LHD-85M	HD12	
	CYM1466HD-85MB	HD12	
	CYM1466LHD-85MB	HD12	
100	CYM1466HD-100M	HD12	Military
	CYM1466LHD-100M	HD12	
	CYM1466HD-100MB	HD12	
	CYM1466LHD-100MB	HD12	
120	CYM1466HD-120M	HD12	Military
	CYM1466LHD-120M	HD12	
	CYM1466HD-120MB	HD12	
	CYM1466LHD-120MB	HD12	

Document #: 38-M-00044-A