Integrated Device Technology, Inc.

CMOS ASYNCHRONOUS FIFO
2,048 x 9, 4,096 x 9, 8,192 x 9, 16,384 x 9, 32,768 x 9 and 65,536 x 9

IDT7203
IDT7204
IDT7205
IDT7206
IDT7207
IDT7208

FEATURES:

- First-In/First-Out Dual-Port memory
- 2,048 x 9 organization (IDT7203)
- 4,096 x 9 organization (IDT7204)
- 8,192 x 9 organization (IDT7205)
- 16,384 x 9 organization (IDT7206)
- 32,768 x 9 organization (IDT7207)
- 65,636 x 9 organization (IDT7208)
- High-speed: 12ns access time
- Low power consumption
  — Active: 660mW (max.)
  — Power-down: 44mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable in both word depth and width
- Pin and functionally compatible with IDT720X family
- Status Flags: Empty, Half-Full, Full
- Retransmit capability
- High-performance CMOS technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing for #5962-88669 (IDT7203), 5962-89567 (IDT7203), and 5962-89568 (IDT7204) are listed on this function
- Industrial temperature range (–40°C to +85°C) is available (for plastic packages only)

DESCRIPTION:

The IDT7203/7204/7205/7206/7207/7208 are dual-port memory buffers with internal pointers that load and empty data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins.

The device's 9-bit width provides a bit for a control or parity at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows the read pointer to be reset to its initial position when $\overline{RT}$ is pulsed LOW. A Half-Full Flag is available in the single device and width expansion modes.

These FIFOs are fabricated using IDT's high-speed CMOS technology. They are designed for applications requiring asynchronous and simultaneous read/writes in multiprocessing, rate buffering and other applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.
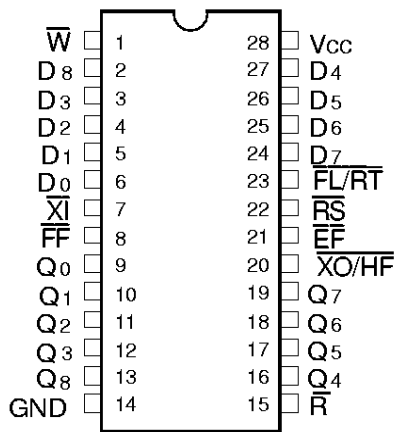
FUNCTIONAL BLOCK DIAGRAM
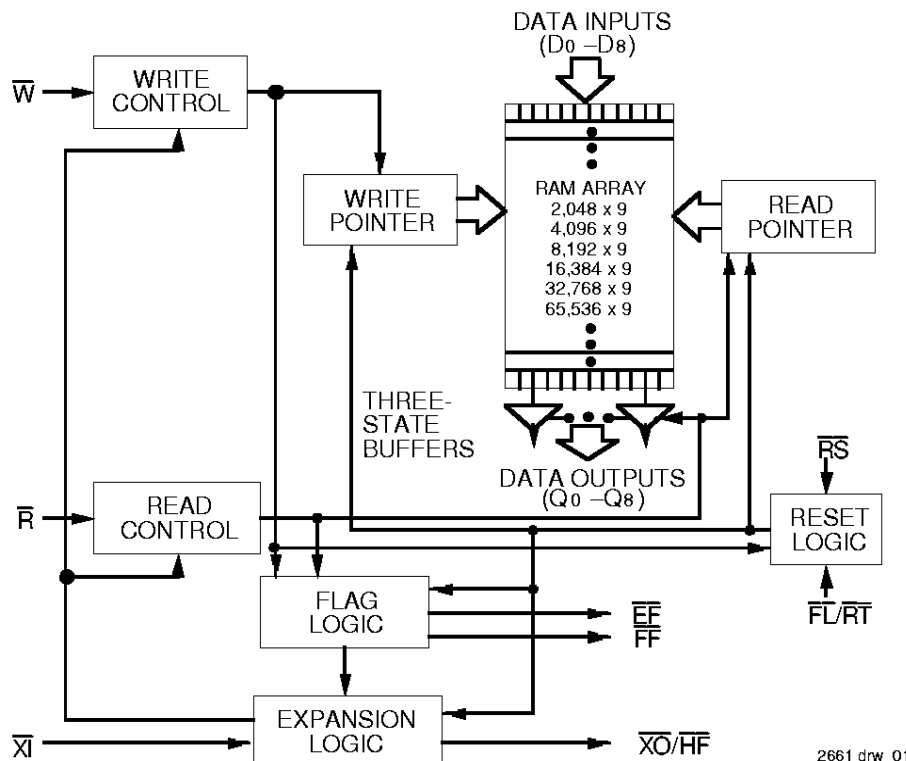
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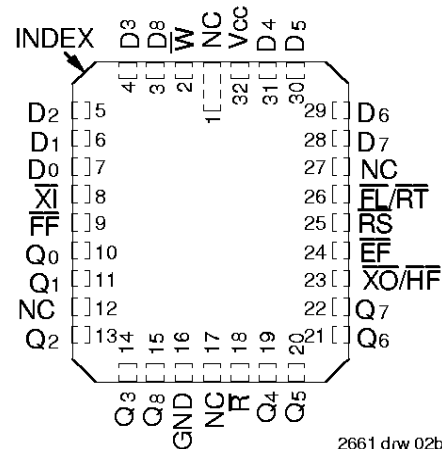**MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES**

SEPTEMBER 1997

IDT7203/7204/7205/7206/7207/7208 CMOS ASYNCHRONOUS FIFO
2,048 x 9, 4,096 x 9, 8,192 x 9, 16,384 x 9, 32,768 x 9 and 65,536 x 9

MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

PIN CONFIGURATIONS

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    W̄  □ 1      28 □ Vcc
    D8 □ 2      27 □ D4
    D3 □ 3      26 □ D5
    D2 □ 4      25 □ D6
    D1 □ 5      24 □ D7
    D0 □ 6      23 □ FL/R̄T̄
    X̄Ī □ 7      22 □ R̄S̄
    F̄F̄ □ 8      21 □ ĒF̄
    Q0 □ 9      20 □ XO/H̄F̄
    Q1 □ 10     19 □ Q7
    Q2 □ 11     18 □ Q6
    Q3 □ 12     17 □ Q5
    Q8 □ 13     16 □ Q4
   GND □ 14     15 □ R̄
```

2661 drw 02a

TOP VIEW

Package Type	Reference Identifier	Order Code	Device Availability
PLASTIC DIP	P28-1	P	All devices
PLASTIC THIN DIP	P28-2	TP	All except 7207/7208
CERDIP	D28-1	D	All except 7208
THIN CERDIP	D28-3	TD	Only for 7203/7204/7205
SOIC	SO28-3	SO	Only for 7204

NOTES:
1. This package is only available in the military temperature range.
2. Consult factory for CERPACK pinout.

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INDEX   D3 D8 W̄ NC Vcc D4 D5
        4  3  2  1  32 31 30
   D2 [ 5              29 ] D6
   D1 [ 6              28 ] D7
   D0 [ 7              27 ] NC
   X̄Ī [ 8              26 ] FL/R̄T̄
   F̄F̄ [ 9              25 ] R̄S̄
   Q0 [ 10             24 ] ĒF̄
   Q1 [ 11             23 ] XO/H̄F̄
   NC [ 12             22 ] Q7
   Q2 [ 13             21 ] Q6
        14 15 16 17 18 19 20
        Q3 Q8 GND NC R̄ Q4 Q5
```

2661 drw 02b

TOP VIEW

Package Type	Reference Identifier	Order Code	Device Availability
PLCC	J32-1	J	All devices
LCC[1]	L32-1	L	All except 7208

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Military	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
TSTG	Storage Temperature	−55 to +125	−65 to +155	°C
IOUT	DC Output Current	−50 to +50	−50 to +50	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH[1]	Input High Voltage Commercial	2.0	—	—	V
VIH[1]	Input High Voltage Military	2.2	—	—	V
VIL[1]	Input Low Voltage Commercial and Military	—	—	0.8	V
TA	Operating Temperature Commercial	0 to +70	—	—	°C
TA	Operating Temperature Industrial	−40 to +85	—	—	°C
TA	Operating Temperature Military	−55 to +125	—	—	°C

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NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Industrial: V_{CC} = 5V ± 10%, T_A = –40°C to +85°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT7203 IDT7204 Commercial and Industrial[1] t_A = 12, 15, 20, 25, 35, 50 ns			IDT7203 IDT7204 Military[2] t_A = 20, 30, 40, 50, 65, 80, 120 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[4]	Input Leakage Current (Any Input)	–1	—	1	–1	—	1	μA
I_{LO}[5]	Output Leakage Current	–10	—	10	–10	—	10	μA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}[6,7,8]	Active Power Supply Current	—	—	120	—	—	150	mA
I_{CC2}[6,8,9]	Standby Current ($\overline{R}=\overline{W}=\overline{RS}=\overline{FL}/\overline{RT}=V_{IH}$)	—	—	12	—	—	25	mA
I_{CC3}[6,8,9]	Power Down Current	—	—	2	—	—	4	mA

Symbol	Parameter	IDT7205 IDT7206 IDT7207 IDT7208[1,3] Commercial and Industrial[1] t_A = 15, 20, 25, 35, 50 ns			IDT7205 IDT7206 IDT7207 Military t_A = 20, 30, 50 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[4]	Input Leakage Current (Any Input)	–1	—	1	–1	—	1	μA
I_{LO}[5]	Output Leakage Current	–10	—	10	–10	—	10	μA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}[6,7,8]	Active Power Supply Current	—	—	120	—	—	150	mA
I_{CC2}[6,8,9]	Standby Current ($\overline{R}=\overline{W}=\overline{RS}=\overline{FL}/\overline{RT}=V_{IH}$)	—	—	12	—	—	25	mA
I_{CC3}[6,8,9]	Power Down Current	—	—	8	—	—	12	mA

2661 tbl 03

NOTES:
1. Industrial temperature range product for the 25 ns speed grade is available as a standard device (excluding the 7208). All other speed grades are available by special order.
2. Speed grades of 65, 80, and 120 ns are only available in the ceramic DIP.
3. Only commercial speed grades of 20, 25 and 35 ns are available for the 7208.
4. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
5. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
6. Tested with outputs open (I_{OUT} = 0).
7. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
8. Icc measurements are made with outputs open.
9. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2661 tbl 07

CAPACITANCE[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES: 2661 tbl 08
1. This parameter is sampled and not 100% tested.
2. With output deselected.

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Industrial: Vcc = 5V ± 10%, TA = –40°C to +85°C; Military: Vcc = 5V ± 10%, TA = –55°C to +125°C)

Symbol	Parameters	Commercial 7203L12 7204L12 Min.	Max.	Commercial 7203L15 7204L15 7205L15 7206L15 7207L15 Min.	Max.	Com'l & Mil. 7203L20 7204L20 7205L20 7206L20 7207L20 / Commercial 7208L20 Min.	Max.	Com'l & Ind'l[2] 7203L25 7204L25 7205L25 7206L25 7207L25 / Commercial 7208L25 Min.	Max.	Military 7203L30 7204L30 7205L30 7206L30 7207L30 Min.	Max.	Com'l 7203L35 7204L35 7205L35 7206L35 7207L35 / Commercial 7208L35 Min.	Max.	Unit
fs	Shift Frequency	—	50	—	40	—	33.3	—	28.5	—	25	—	22.2	MHz
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
tA	Access Time	—	12	—	15	—	20	—	25	—	30	—	35	ns
tRR	Read Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
tRPW	Read Pulse Width[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
tRLZ	Read LOW to Data Bus LOW[4]	3	—	5	—	5	—	5	—	5	—	5	—	ns
tWLZ	Write HIGH to Data Bus Low-Z[4 5]	3	—	5	—	5	—	5	—	5	—	10	—	ns
tDV	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	5	—	5	—	ns
tRHZ	Read HIGH to Data Bus High-Z[4]	—	12	—	15	—	15	—	18	—	20	—	20	ns
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
tWPW	Write Pulse Width[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	9	—	11	—	12	—	15	—	18	—	18	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tRSC	Reset Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
tRS	Reset Pulse Width[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
tRSS	Reset Set-up Time[4]	12	—	15	—	20	—	25	—	30	—	35	—	ns
tRTR	Reset Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
tRTC	Retransmit Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
tRT	Retransmit Pulse Width[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
tRTS	Retransmit Set-up Time[4]	12	—	15	—	20	—	25	—	30	—	35	—	ns
tRSR	Retransmit Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
tEFL	Reset to EF LOW	—	12	—	25	—	30	—	35	—	40	—	45	ns
tHFH, tFFH	Reset to HF and FF HIGH	—	17	—	25	—	30	—	35	—	40	—	45	ns
tRTF	Retransmit LOW to Flags Valid	—	20	—	25	—	30	—	35	—	40	—	45	ns
tREF	Read LOW to EF LOW	—	12	—	15	—	20	—	25	—	30	—	30	ns
tRFF	Read HIGH to FF HIGH	—	14	—	15	—	20	—	25	—	30	—	30	ns
tRPE	Read Pulse Width after EF HIGH	12	—	15	—	20	—	25	—	30	—	35	—	ns
tWEF	Write HIGH to EF HIGH	—	12	—	15	—	20	—	25	—	30	—	30	ns
tWFF	Write LOW to FF LOW	—	14	—	15	—	20	—	25	—	30	—	30	ns
tWHF	Write LOW to HF Flag LOW	—	17	—	25	—	30	—	35	—	40	—	45	ns
tRHF	Read HIGH to HF Flag HIGH	—	17	—	25	—	30	—	35	—	40	—	45	ns
tWPF	Write Pulse Width after FF HIGH	12	—	15	—	20	—	25	—	30	—	35	—	ns
tXOL	Read/Write LOW to XO LOW	—	12	—	15	—	20	—	25	—	30	—	35	ns
tXOH	Read/Write HIGH to XO HIGH	—	12	—	15	—	20	—	25	—	30	—	35	ns
tXI	XI Pulse Width[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
tXIR	XI Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
tXIS	XI Set-up Time	8	—	10	—	10	—	10	—	10	—	15	—	ns

NOTES:

2661 tbl 05

1. Timings referenced as in AC Test Conditions.
2. Industrial temperature range product for the 25 ns speed grade is available as a standard device. All other speed grades are available by special order.
3. Pulse widths less than minimum are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.

AC ELECTRICAL CHARACTERISTICS[1] (Continued)

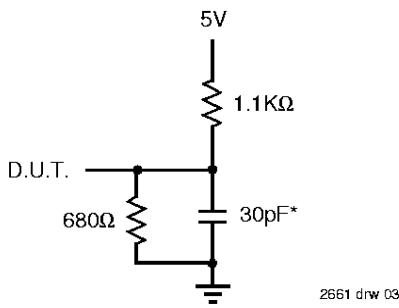(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

Symbol	Parameters	Military 7203L40 7204L40		Com'l & Mil. 7203L50 7204L50 7205L50 7206L50 7207L50		Military[2] 7203L65 7204L65		7203L80 7204L80		7203L120 7204L120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fs	Shift Frequency	—	20	—	15	—	12.5	—	10	—	7	MHz
tRC	Read Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
tA	Access Time	—	40	—	50	—	65	—	80	—	120	ns
tRR	Read Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
tRPW	Read Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
tRLZ	Read LOW to Data Bus LOW[4]	5	—	10	—	10	—	10	—	10	—	ns
tWLZ	Write HIGH to Data Bus Low-Z[4, 5]	10	—	15	—	15	—	20	—	20	—	ns
tDV	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	5	—	ns
tRHZ	Read HIGH to Data Bus High-Z[4]	—	25	—	30	—	30	—	30	—	35	ns
tWC	Write Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
tWPW	Write Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
tWR	Write Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
tDS	Data Set-up Time	20	—	30	—	30	—	40	—	40	—	ns
tDH	Data Hold Time	0	—	5	—	10	—	10	—	10	—	ns
tRSC	Reset Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
tRS	Reset Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
tRSS	Reset Set-up Time[4]	40	—	50	—	65	—	80	—	120	—	ns
tRSR	Reset Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
tRTC	Retransmit Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
tRT	Retransmit Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
tRTS	Retransmit Set-up Time[4]	40	—	50	—	65	—	80	—	120	—	ns
tRSR	Retransmit Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
tEFL	Reset to EF LOW	—	50	—	65	—	80	—	100	—	140	ns
tHFH, tFFH	Reset to HF and FF HIGH	—	50	—	65	—	80	—	100	—	140	ns
tRTF	Retransmit LOW to Flags Valid	—	50	—	65	—	80	—	100	—	140	ns
tREF	Read LOW to EF Flag LOW	—	35	—	45	—	60	—	60	—	60	ns
tRFF	Read HIGH to FF HIGH	—	35	—	45	—	60	—	60	—	60	ns
tRPE	Read Pulse Width after EF HIGH	40	—	50	—	65	—	80	—	120	—	ns
tWEF	Write HIGH to EF HIGH	—	35	—	45	—	60	—	60	—	60	ns
tWFF	Write LOW to FF LOW	—	35	—	45	—	60	—	60	—	60	ns
tWHF	Write LOW to HF LOW	—	50	—	65	—	80	—	100	—	140	ns
tRHF	Read HIGH to HF HIGH	—	50	—	65	—	80	—	100	—	140	ns
tWPF	Write Pulse Width after FF HIGH	40	—	50	—	65	—	80	—	120	—	ns
tXOL	Read/Write LOW to XO LOW	—	40	—	50	—	65	—	80	—	120	ns
tXOH	Read/Write HIGH to XO HIGH	—	40	—	50	—	65	—	80	—	120	ns
tXI	XI Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
tXIR	XI Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
tXIS	XI Set-up Time	15	—	15	—	15	—	15	—	15	—	ns

NOTES:

2661 tbl 06

1. Timings referenced as in AC Test Conditions.
2. Speed grades 65, 80, and 120ns are only available in the CERDIP package.
3. Pulse widths less than minimum are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.

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MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

2661 drw 03

OR EQUIVALENT CIRCUIT

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

Inputs:

DATA IN (D0–D8) — Data inputs for 9-bit wide data.

Controls:

RESET ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown in Figure 2 (i.e. tRSS before the rising edge of $\overline{RS}$) and should not change until tRSR after the rising edge of $\overline{RS}$.**

WRITE ENABLE ($\overline{W}$) — A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered-to, with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW, and will remain set until the difference between the write pointer and read pointer is less-than or equal to one-half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW on the falling edge of the last write signal, which inhibits further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after tRFF, allowing a new valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$) — A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$), provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (Q0 through Q8) will return to a high-impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go

LOW, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high-impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after tWEF and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$) — This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7203/7204/7205/7206/7207/7208 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. The status of the Flags will change depending on the relative locations of the read and write pointers. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than 2,048/4,096/8,192/16,384/32,768/65,536 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode.

EXPANSION IN ($\overline{XI}$) — This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy-Chain Mode.

Outputs:

FULL FLAG ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations, when the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 2,048/4,096/8,192/16,384/32,768/65,536 writes.

EMPTY FLAG ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$) — This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory. There will be an $\overline{XO}$ pulse when the Write pointer reaches the last location of memory, and an additional $\overline{XO}$ pulse when the Read pointer reaches the last location of memory.

DATA OUTPUTS (Q0-Q8) — Q0-Q8 are data outputs for 9-bit wide data. These outputs are in a high-impedance condition whenever Read ($\overline{R}$) is in a HIGH state.
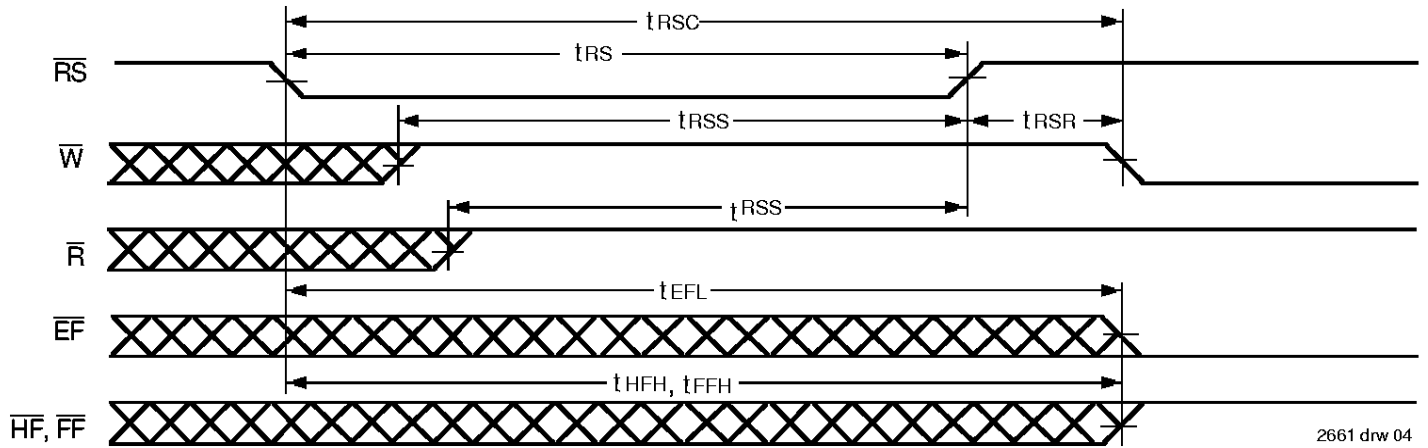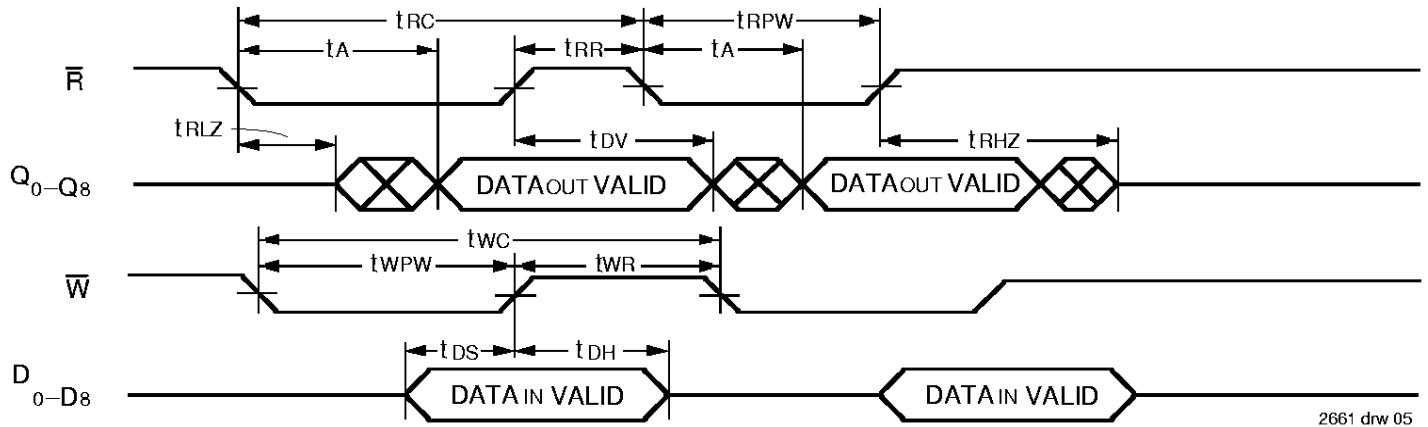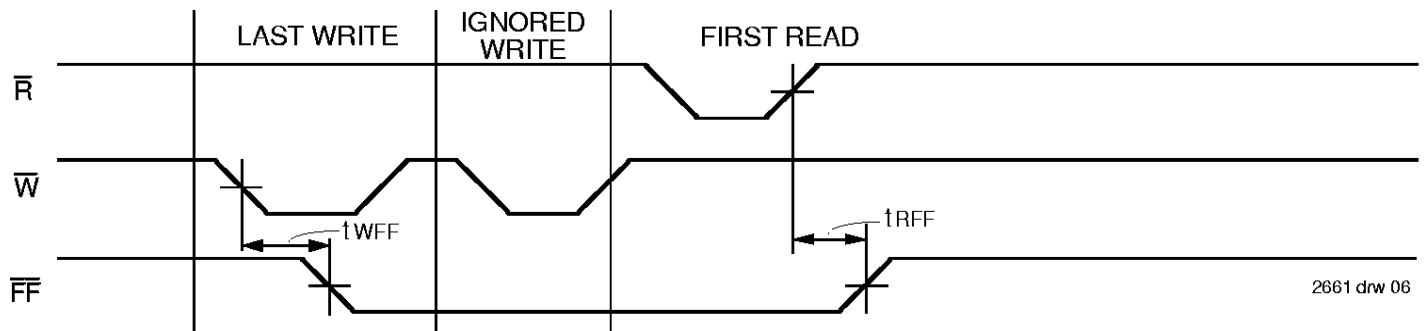
NOTE:
1. $\overline{W}$ and $\overline{R}$ = V$_{IH}$ around the rising edge of $\overline{RS}$.

Figure 2. Reset

Figure 3. Asynchronous Write and Read Operation
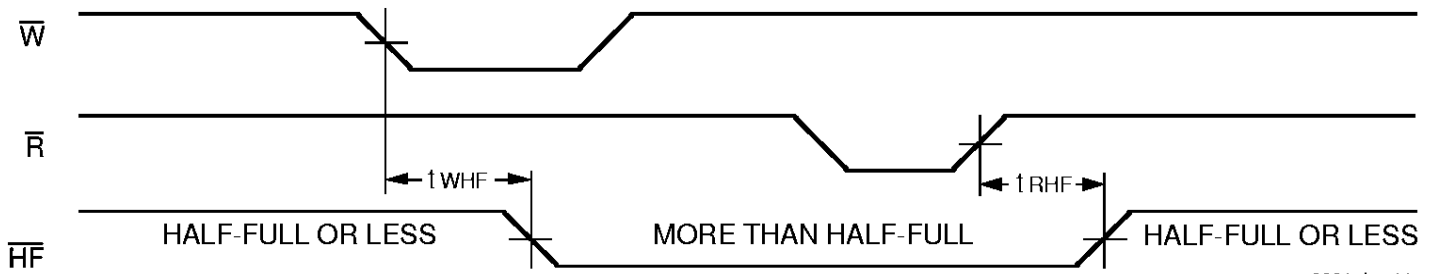
Figure 4. Full Flag Timing From Last Write to First Read

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Figure 5. Empty Flag Timing From Last Read to First Write

2661 drw 08

NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

2661 drw 09

Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse.

2661 drw 10

Figure 8. Minimum Timing for a Full Flag Coincident Write Pulse.

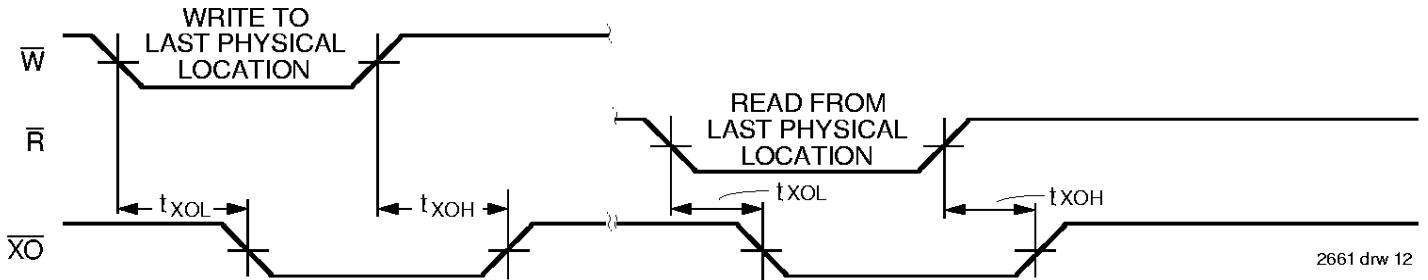**Figure 9. Half-Full Flag Timing**

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Figure 10. Expansion Out
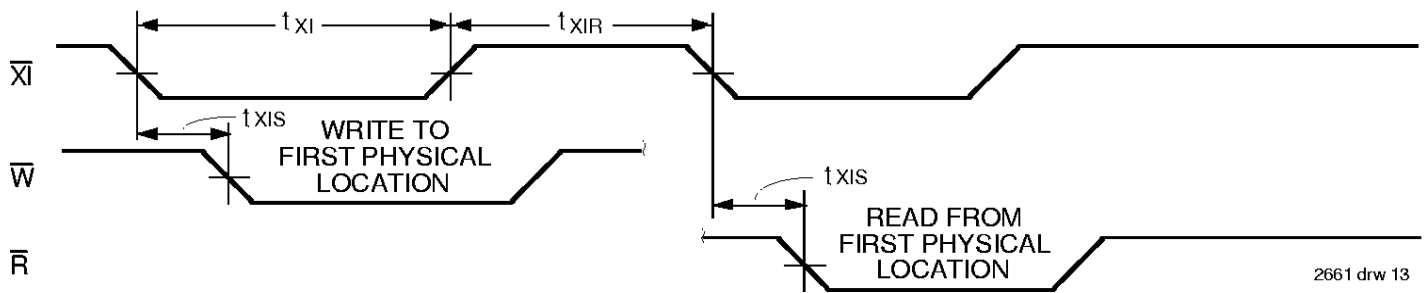
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Figure 11. Expansion In

2661 drw 13

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information on the IDT7203/7204/7205/7206/7207, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Single Device Mode

A single IDT7203/7204/7205/7206/7207/7208 may be used when the application requirements are for 2,048/4,096/8,192/16,384/32,768/65,536 words or less. These FIFOs are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Depth Expansion

These FIFOs can easily be adapted to applications when the requirements are for greater than 2,048/4,096/8,192/16,384/32,768/65,536 words. Figure 14 demonstrates Depth Expansion using three IDT7203/7204/7205/7206/7207/7208s. Any depth can be attained by adding additional IDT7203/7204/7205/7206/7207/7208s. These devices operate in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information on the IDT7203/7204/7205/7206/7207, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

USAGE MODES:

Width Expansion

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7203/7204/7205/7206/7207/7208s. Any word width can be attained by adding additional IDT7203/7204/7205/7206/7207/7208s (Figure 13).

Bidirectional Operation

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7203/7204/7205/7206/7207/7208s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in (t_{WEF} + t_A) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

Compound Expansion

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).
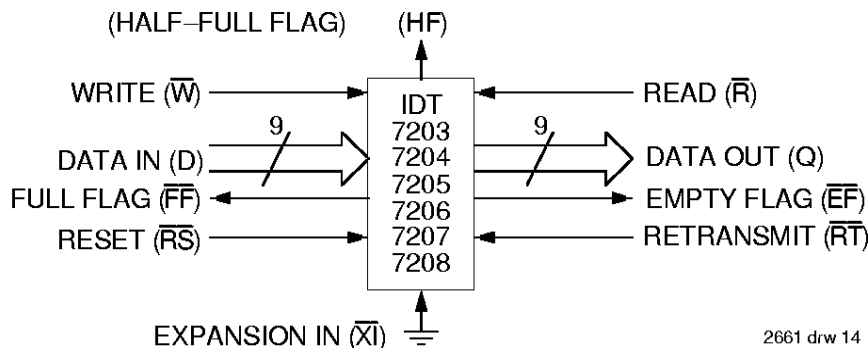
Figure 12. Block Diagram of 2,048 x 9, 4,096 x 9, 8,192 x 9, 16,384 x 9, 32,768 x 9, 65,536 x 9 FIFO Used in Single Device Mode
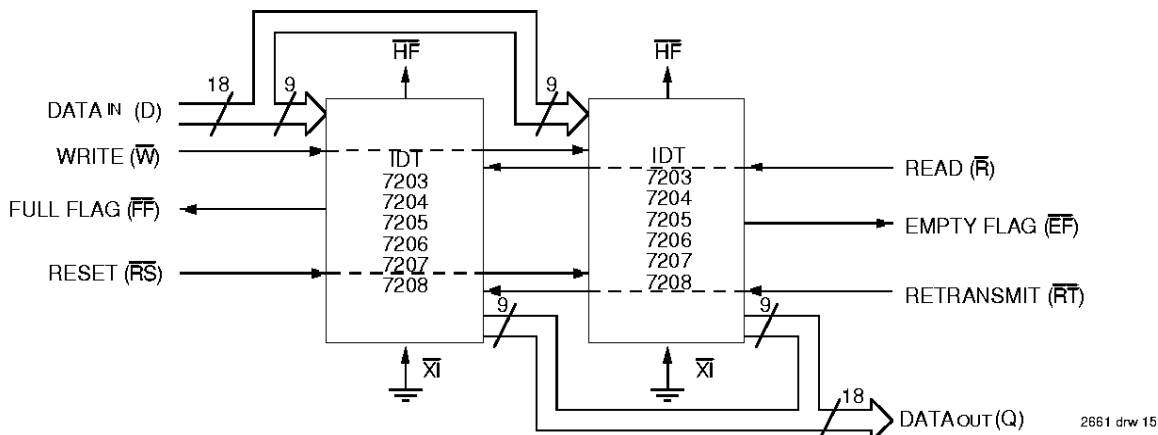
NOTE:
1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

Figure 13. Block Diagram of 2,048 x 18, 4,096 x 18, 8,192 x 18, 16,384 x 18, 32,768 x 18, 65,536 x 18 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT
SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE: 2661 tbl 09
1. Pointer will Increment if flag is HIGH.

TABLE II – RESET AND FIRST LOAD
DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES: 2661 tbl 10
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

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Figure 14. Block Diagram of 6,144 x 9, 12,288 x 9, 24,576 x 9, 49,152 x 9, 98,304 x 9, 196,608 x 9 FIFO Memory (Depth Expansion)

NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.
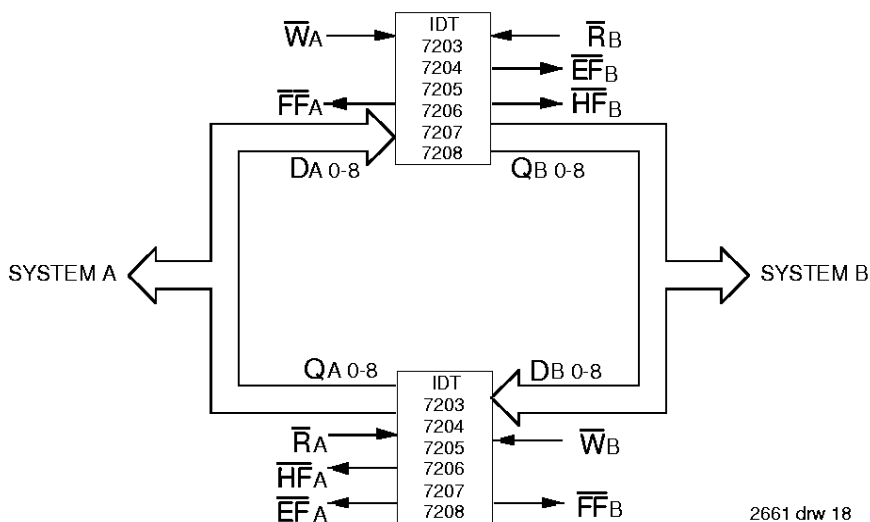
Figure 15. Compound FIFO Expansion

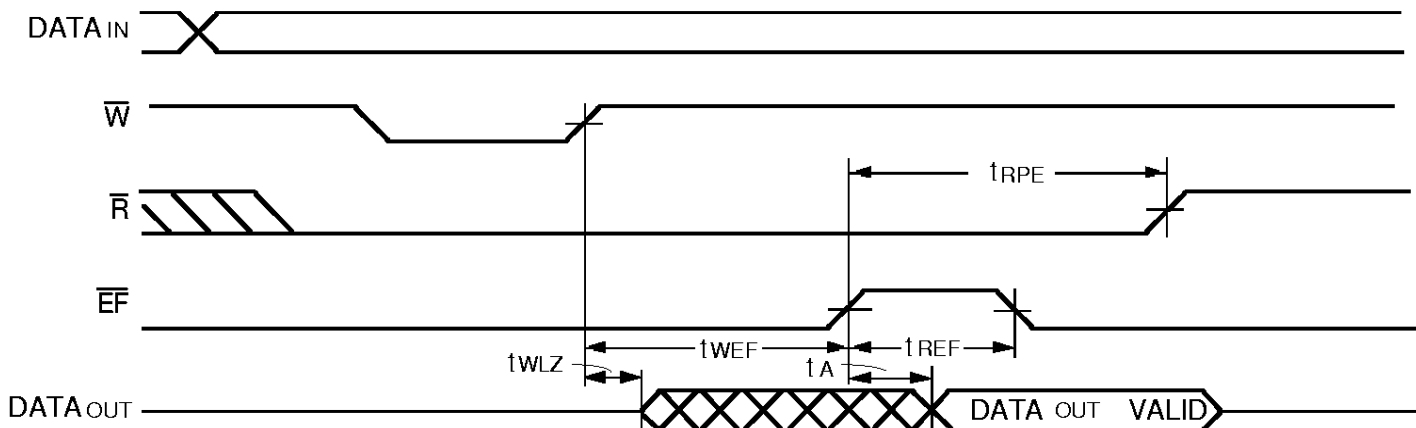**Figure 16. Bidirectional FIFO Operation**
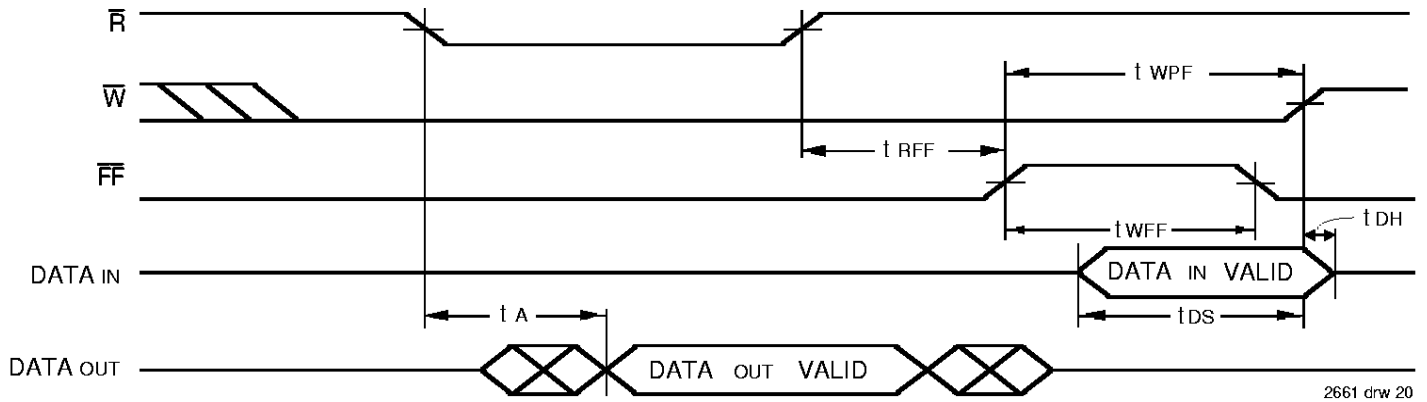

Figure 17. Read Data Flow-Through Mode

Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT	XXXX	X	XX	X	X
	Device Type	Power	Speed	Package	Process/Temperature Range

Blank	Commercial (0°C to +70°C)	
I(1)	Industrial (–40 to +85°C)	
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B	

P	Plastic DIP	P28-1	
TP	Plastic Thin DIP	P28-2	(all except 7207/7208)
D	CERDIP	D28-1	(all except 7208)
TD	Thin CERDIP	D28-3	(only for 7203/7204/7205)
J	Plastic Leaded Chip Carrier PLCC	J32-1	
L(2)	Leadless Chip Carrier LCC	L32-1	(all except 7208)
SO	Small Outline IC SOIC	SO28-3	(only 7204)

12	Commercial 7203/04 Only	
15	Commercial Only	
20(3)		
25(3)	Commercial and Industrial	Access Time (tA)
30	Military Only	Speed in
35(3)	Commercial Only	Nanoseconds
40	Military 7203/04 Only	
50		
65		
80	Military 7203/04DB Only	
120		

L	Low Power

7203	2,048 x 9 FIFO
7204	4,096 x 9 FIFO
7205	8,192 x 9 FIFO
7206	16,384 x 9 FIFO
7207	32,768 x 9 FIFO
7208(3)	65,536 x 9 FIFO

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NOTES:
1. Industrial temperature range is available for plastic packages by special order for speed grades faster than 25 ns (excluding the 7208).
2. The LCC is only available in the military temperature range.
3. The 7208 is only available in commercial speed grades of 20, 25 and 35 ns.