

SN74ALVCH162830

1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

SCES082G – AUGUST 1996 – REVISED JUNE 1999

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Thin Very Small-Outline Package**

NOTE: For tape and reel order entry:
The DBBR package is abbreviated to GR.

description

This 1-bit to 2-bit address driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVCH162830 is characterized for operation from -40°C to 85°C.

**DBB PACKAGE
(TOP VIEW)**

	1		80		1Y3
2Y2	2		79		2Y3
1Y2	3		78		GND
GND	4		77		1Y4
2Y1	5		76		2Y4
1Y1	6		75		V_{CC}
V_{CC}	7		74		1Y5
A1	8		73		2Y5
A2	9		72		GND
GND	10		71		1Y6
A3	11		70		2Y6
A4	12		69		GND
GND	13		68		1Y7
A5	14		67		2Y7
A6	15		66		V_{CC}
V_{CC}	16		65		1Y8
A7	17		64		2Y8
A8	18		63		GND
GND	19		62		1Y9
A9	20		61		2Y9
$\overline{OE1}$	21		60		1Y10
$\overline{OE2}$	22		59		2Y10
A10	23		58		GND
GND	24		57		1Y11
A11	25		56		2Y11
A12	26		55		V_{CC}
V_{CC}	27		54		1Y12
A13	28		53		2Y12
A14	29		52		GND
GND	30		51		1Y13
A15	31		50		2Y13
A16	32		49		GND
GND	33		48		1Y14
A17	34		47		2Y14
A18	35		46		V_{CC}
V_{CC}	36		45		1Y15
2Y18	37		44		2Y15
1Y18	38		43		GND
GND	39		42		1Y16
2Y17	40		41		2Y16
1Y17					



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 1999, Texas Instruments Incorporated

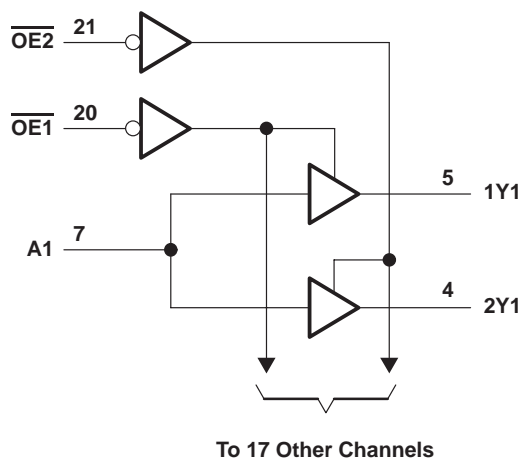
SN74ALVCH162830
1-BIT TO 2-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS

SCES082G – AUGUST 1996 – REVISED JUNE 1999

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	A	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	± 50 mA
Continuous current through each V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3)	106°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH162830
1-BIT TO 2-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS

SCES082G – AUGUST 1996 – REVISED JUNE 1999

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	-2	mA
		V _{CC} = 2.3 V	-6	
		V _{CC} = 2.7 V	-8	
		V _{CC} = 3 V	-12	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	2	mA
		V _{CC} = 2.3 V	6	
		V _{CC} = 2.7 V	8	
		V _{CC} = 3 V	12	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74ALVCH162830
1-BIT TO 2-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS

SCES082G – AUGUST 1996 – REVISED JUNE 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V
	I _{OH} = -2 mA	1.65 V	1.2			
	I _{OH} = -4 mA	2.3 V	1.9			
	I _{OH} = -6 mA	2.3 V	1.7			
		3 V	2.4			
	I _{OH} = -8 mA	2.7 V	2			
I _{OH} = -12 mA	3 V	2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 2 mA	1.65 V			0.45	
	I _{OL} = 4 mA	2.3 V			0.4	
	I _{OL} = 6 mA	2.3 V			0.55	
		3 V			0.55	
	I _{OL} = 8 mA	2.7 V			0.6	
I _{OL} = 12 mA	3 V			0.8		
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _I (hold)	V _I = 0.58 V	1.65 V	25			μA
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V	2.3 V	-45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	V _I = 0 to 3.6 V‡	3.6 V			±500	
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		4.5	pF
	Data inputs				5	
C _O	Outputs	V _O = V _{CC} or GND	3.3 V		7.5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	§	1.2	3.8	4		1.7	3.5	ns
t _{en}	\overline{OE}	Y	§	1	5.7	5.7		1	4.8	ns
t _{dis}	\overline{OE}	Y	§	1.5	6.2	5.4		1.7	5.2	ns

§ This information was not available at the time of publication.

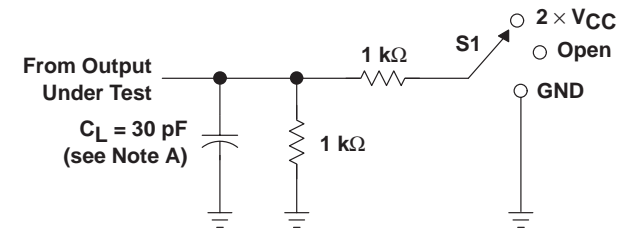


operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	All outputs enabled	$C_L = 0, f = 10\text{ MHz}$	†	50	54	pF
	All outputs disabled		†	8	8	

† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8\text{ V}$

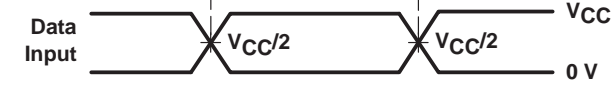


LOAD CIRCUIT

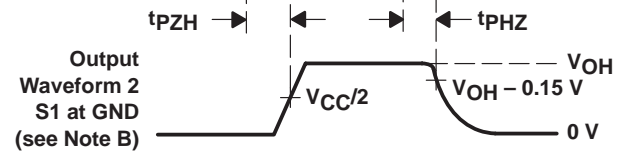
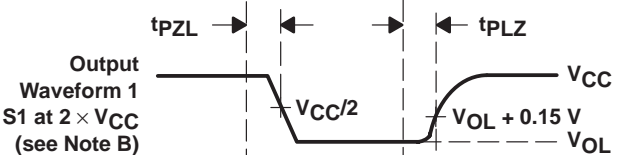
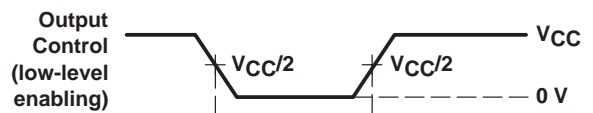
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



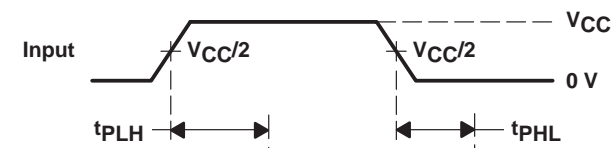
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

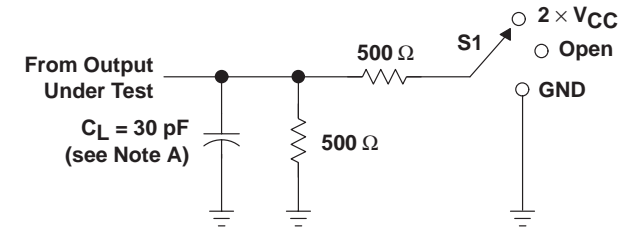
Figure 1. Load Circuit and Voltage Waveforms

SN74ALVCH162830
1-BIT TO 2-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS

SCES082G – AUGUST 1996 – REVISED JUNE 1999

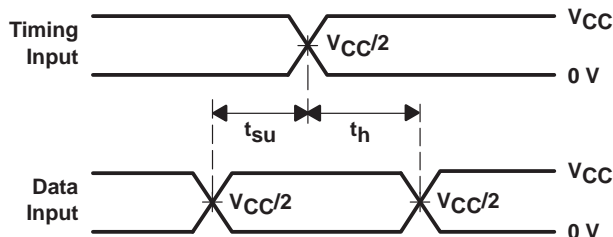
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 V \pm 0.2 V$

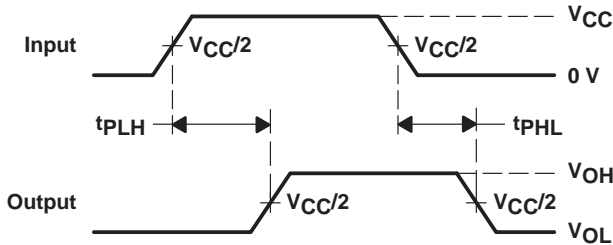


LOAD CIRCUIT

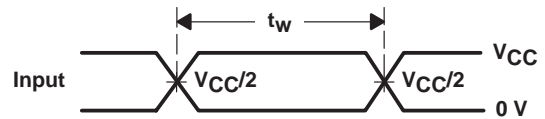
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



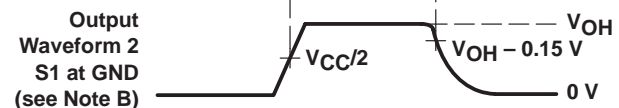
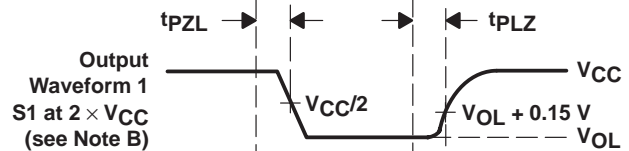
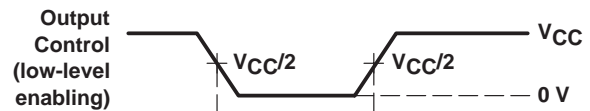
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



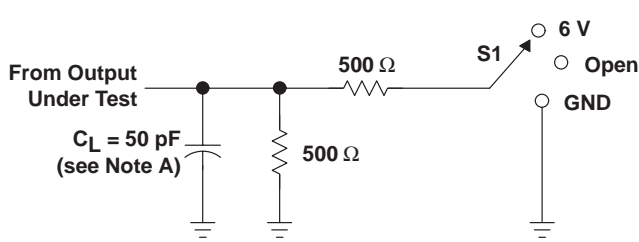
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

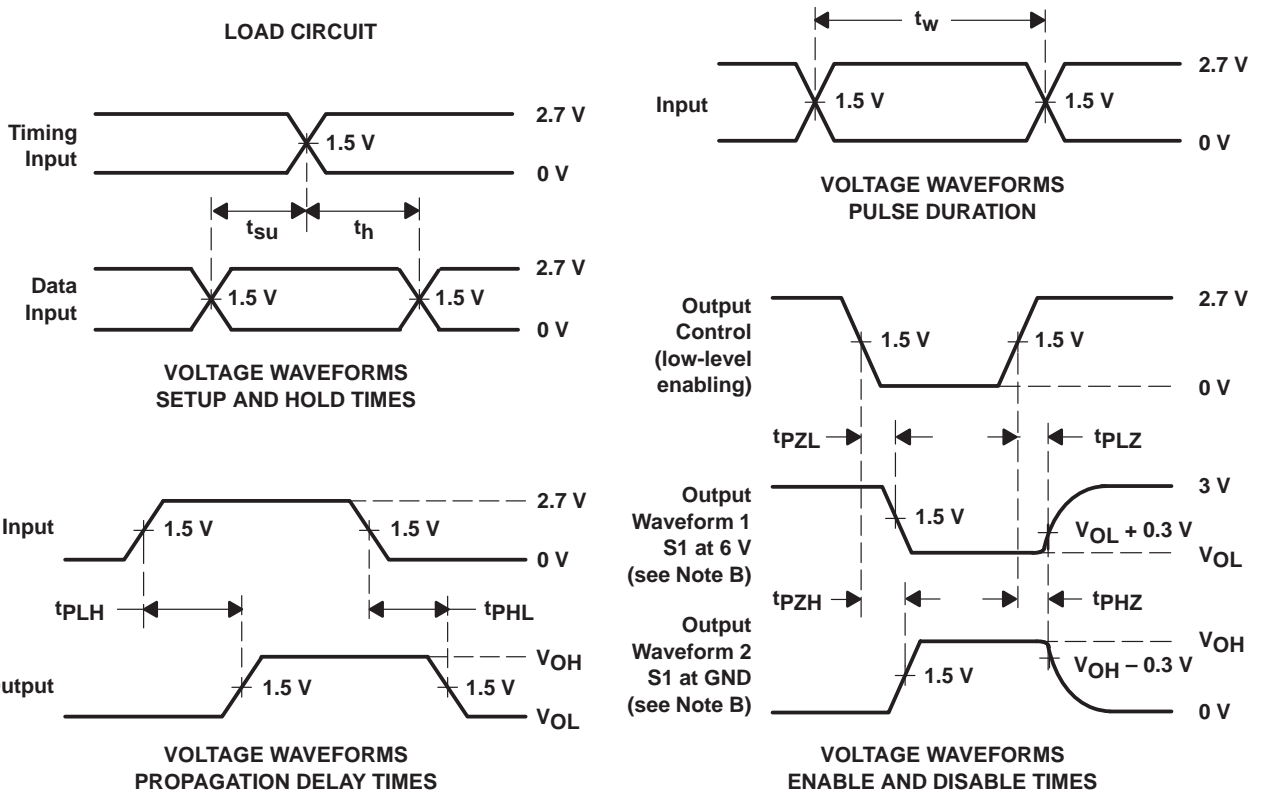
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.