OKI semiconductor

MSM548512

524,288-Word x 8-Bit HIGH-SPEED PSRAM

GENERAL DESCRIPTION

The MSM548512 is a 4 Mbit, high-speed, and low-power CMOS Pseudo Static RAM organized as 524,288 words × 8 bits.

The MSM548512 is fabricated using OKI's CMOS silicon gate process technology. This process, coupled with single-transister memory storage cells, permits maximum circuit density, minimum chip size and high speed.

The -L series have self refresh mode in addition to address refresh mode and auto-refresh mode. In the self refresh mode the internal refresh timer and address counter refresh the dynamic memory cells automatically. This series allows low power consumption when using standby mode with self refresh. The -D series does not use self refresh mode.

The MSM548512 also features a static RAM-like write function that writes the data into the memory cell at the rising edge of $\overline{WE}$.

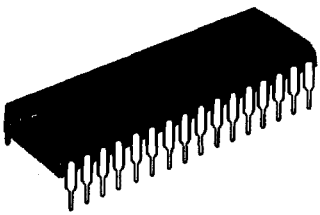
FEATURES

- Large capacity: 4 Mbits (524,288 x 8)
- Fast access time: 80 ns max.
- Low power: 200µA max. (standby with self refresh)
- Refresh free: Self refresh (-L series)
- Logic compatible: SRAM $\overline{WE}$ pin, no address multiplex
- Package compatible: SRAM standard package
600 mil DIP, 525 mil SOP
- Single power supply: 5V ± 10%
- Refresh: 2048 cycle/32 ms auto-address refresh

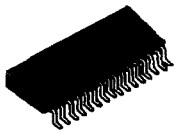
ORDERING INFORMATION

Part Number	Self Refresh	Access Time	Package
MSM548512D-80RS	No	80ns	600 mil,
MSM548512D-10RS	No	100ns	32-pin
MSM548512D-12RS	No	120ns	Plastic
MSM548512L-80RS	Yes	80ns	DIP
MSM548512L-10RS	Yes	100ns	
MSM548512L-12RS	Yes	120ns	
MSM548512D-80GS	No	80ns	525 mil,
MSM548512D-10GS	No	100ns	32-pin
MSM548512D-12GS	No	120ns	Plastic
MSM548512L-80GS	Yes	80ns	SOP
MSM548512L-10GS	Yes	100ns	
MSM548512L-12GS	Yes	120ns	

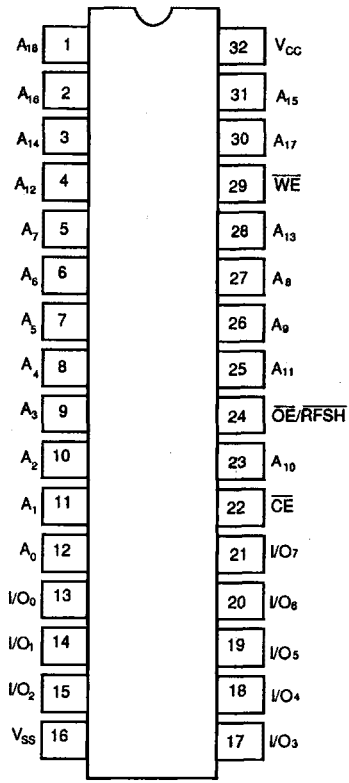
PIN CONFIGURATION



32-Pin Plastic DIP



32-Pin Plastic SOP



(TOP VIEW)

PIN DEFINITION

Pin Name	FUNCTION
A0-A18	Address Input
I/O0-I/O7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$/$\overline{RFSH}$	Output Enable/Refresh Input
$\overline{WE}$	Write Enable Input
V_{CC}	Power
V_{SS}	Ground

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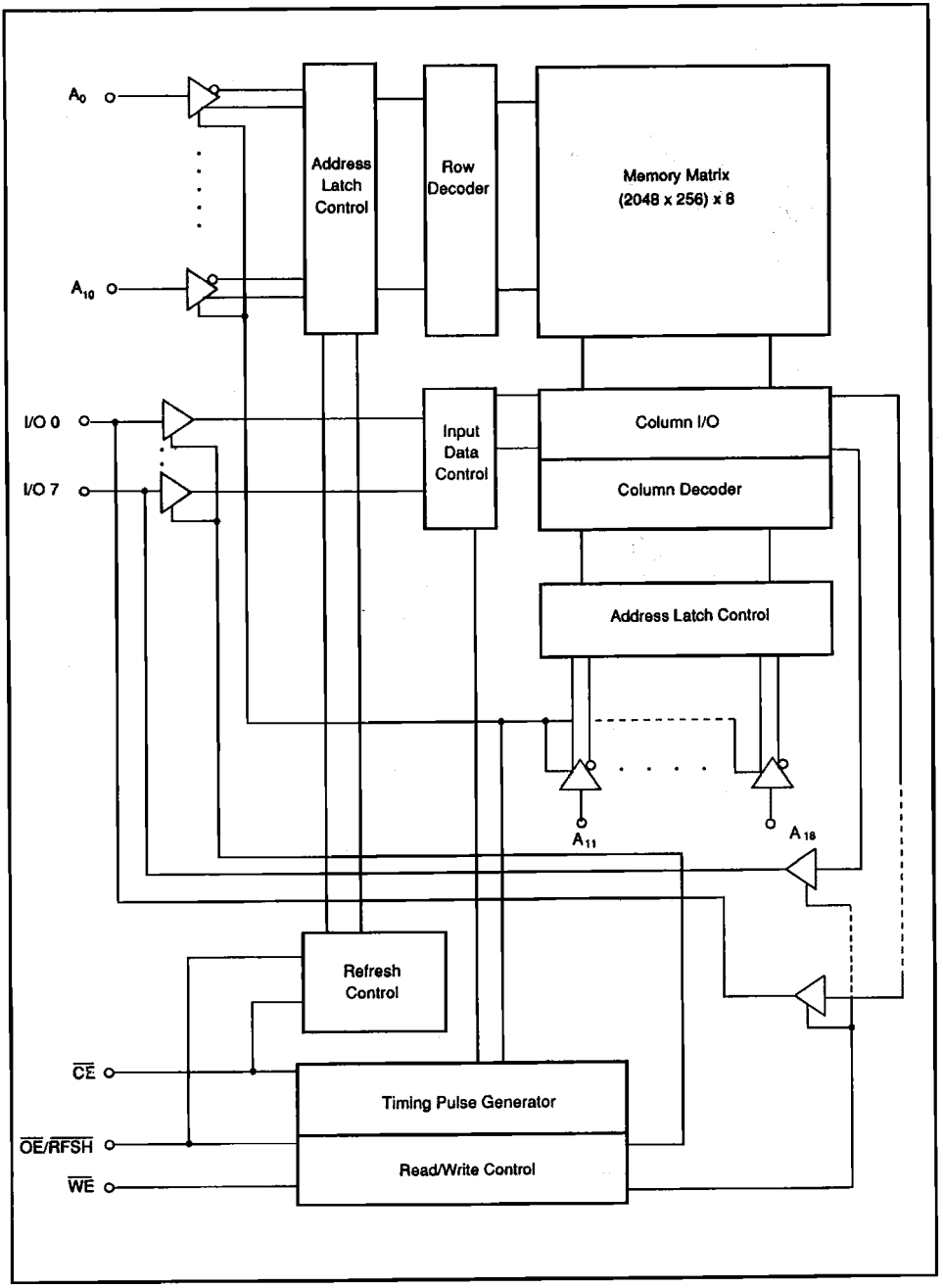
BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE}$	$\overline{OE}/\overline{RFSH}$	$\overline{WE}$	I/O Pin	Mode
L	L	H	Low Z	Read
L	X	L	High Z	Write
L	H	H	High Z	—
H	L	X	High Z	Refresh *1
H	H	X	High Z	Standby

*1 -L Version
L Low-Level Input
H High-Level Input
X Don't Care

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin from Vss *1	V_T	−1.0 ~ +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C
Storage Temperature (biased)	T_{bias}	−10 ~ +85	°C
Short Circuit Output Current	I_{os}	50	mA

*1 To V_{ss}

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC RECOMMENDED OPERATING CONDITIONS

(Ta = 0 ~ +70°C)

Item	Symbol	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	−0.5 *1	—	0.8	V

*1 −3.0V when pulse width is less than 10ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0°C ~ +70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions
Operating Current	I_{CC1}	—	50	75	mA	$I_{I/O}$=Open, t_{cyc}=min.
Standby Current	I_{SB1}	—	1	2	mA	$\overline{CE}$=V_{IH}, $\overline{OE}$/$\overline{RFSH}$=V_{IH}, V_{in}≧0V
	I_{SB2}	—	100	200	uA	$\overline{CE}$=V_{CC}–0.2V, V_{in}≧0V, $\overline{OE}$/$\overline{RFSH}$≧V_{CC}–0.2V
Self Refresh Current	I_{CC2}	—	1	2	mA	$\overline{CE}$=V_{IH}, $\overline{OE}$/$\overline{RFSH}$=V_{IL}, V_{in}≧0V
	I_{CC3}	—	100	200	uA	$\overline{CE}$≧V_{CC}–0.2V, V_{in}≧0V, $\overline{OE}$/$\overline{RFSH}$≧0.2V only L-version
Input Leakage Current	I_{LI}	–10	—	10	µA	V_{CC}=5.5V, V_{in}=Vss~V_{CC}
Output Leakage Current	I_{LO}	–10	—	10	µA	$\overline{OE}$/$\overline{RFSH}$=V_{IH}, $V_{I/O}$=Vss~V_{CC}
Output Low Level	V_{OL}	—	—	0.4	V	I_{OL}=2.1mA
Output High Level	V_{OH}	2.4	—	—	V	I_{OH}=–1mA

CAPACITANCE

(V_{CC} = 5V ± 10%, f = 1MHz, Ta = 25°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions
Input Capacitance	C_{in}	—	—	8	pF	V_{in}=0V
I/O Pin Capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$=0V

Note: This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

Measurement conditions:

Input pulse level	V_{IH}=2.4V, V_{IL}=0.4V
Output reference level	V_{OH}=2.0V, V_{OL}=0.8V
Rising and falling time	5ns
Output load	1TTL + 100pF
Input timing reference level	High=2.2V, Low=0.8V

(V_{CC} = 5V ± 10%, Ta = 0°C ~ +70°C)

Parameter	Symbol	-80		-10		-12		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Random Read, Write Cycle Time	t_{RC}	160	—	180	—	210	—	ns	
Random Read Modify Write Cycle Time	t_{RWC}	220	—	240	—	280	—	ns	
$\overline{CE}$ Access Time	t_{CEA}	—	80	—	100	—	120	ns	
$\overline{OE}$ Access Time	t_{OEA}	—	30	—	40	—	50	ns	
Chip Disable to Output in High-Z	t_{CHZ}	—	25	—	25	—	30	ns	6
$\overline{CE}$ to Output in Low-Z	t_{CLZ}	20	—	20	—	20	—	ns	
$\overline{OE}$ Disable to Output in High-Z	t_{OHZ}	—	25	—	25	—	30	ns	6
$\overline{OE}$ Output in Low-Z	t_{OLZ}	0	—	0	—	0	—	ns	
$\overline{CE}$ Pulse Width	t_{CE}	80n	10μ	100n	10μ	120n	10μ	s	
$\overline{CE}$ Precharge Time	t_P	70	—	70	—	80	—	ns	
Address Set-Up Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	20	—	25	—	30	—	ns	
Read Command Set-Up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
$\overline{OE}$ Command Hold Time	t_{OHC}	15	—	15	—	15	—	ns	
$\overline{OE}$ Delay Time	t_{OCD}	0	—	0	—	0	—	ns	
Write Command Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Chip Enable Time	t_{CW}	80	—	100	—	120	—	ns	
Input Data Set Time	t_{DW}	20	—	25	—	30	—	ns	
Input Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	
Output Active from End of Write	t_{OW}	5	—	5	—	5	—	ns	
Write Enable to Output in High-Z	t_{WHZ}	—	20	—	25	—	30	ns	6
Transition Time	t_T	3	50	3	50	3	50	ns	11
$\overline{RFSH}$ Delay Time from $\overline{CE}$	t_{RFD}	70	—	70	—	80	—	ns	
$\overline{RFSH}$ Precharge Time	t_{FP}	40	—	40	—	40	—	ns	
$\overline{RFSH}$ Pulse Width (Auto-Refresh)	t_{FAP}	80n	8μ	80n	8μ	80n	8μ	s	
Auto-Refresh Cycle Time	t_{FC}	160	—	180	—	210	—	ns	
$\overline{RFSH}$ Pulse Width (Self Refresh)	t_{FAS}	8	—	8	—	8	—	us	13
$\overline{CE}$ Delay Time from $\overline{RFSH}$ in Self Refresh Mode	t_{AFS}	600	—	600	—	600	—	ns	13
Refresh Period (2048 Cycles/32ms)	t_{REF}	—	32	—	32	—	32	ms	

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Notes 1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to Ground.

3. I_{CC1} depends on output loading. Specified values are obtained with the output open.

4. An initial pause of 100 µs is required after power-up, followed by more than 8 initial cycles, before proper device operation is achieved.

5. AC measurements assume tT = 5ns.

6. tCHZ, tOHZ, tWHZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

7. In write cycles, the input data is latched at the earlier rising point of either $\overline{CE}$ or $\overline{WE}$. Write operation is achieved when both $\overline{CE}$ and $\overline{WE}$ are low.

8. The I/O state remains at high impedance after $\overline{CE}$ goes low if the transition occurs at the same time as or after the falling edge of $\overline{WE}$.

9. Use $\overline{WE}$ or $\overline{OE}$ or both signals to disable the output before input data is applied during a write cycle when the input is not the same.

10. Data input must be set to floating state, before I/O becomes low impedance, by $\overline{WE}$ or $\overline{OE}$ or both.

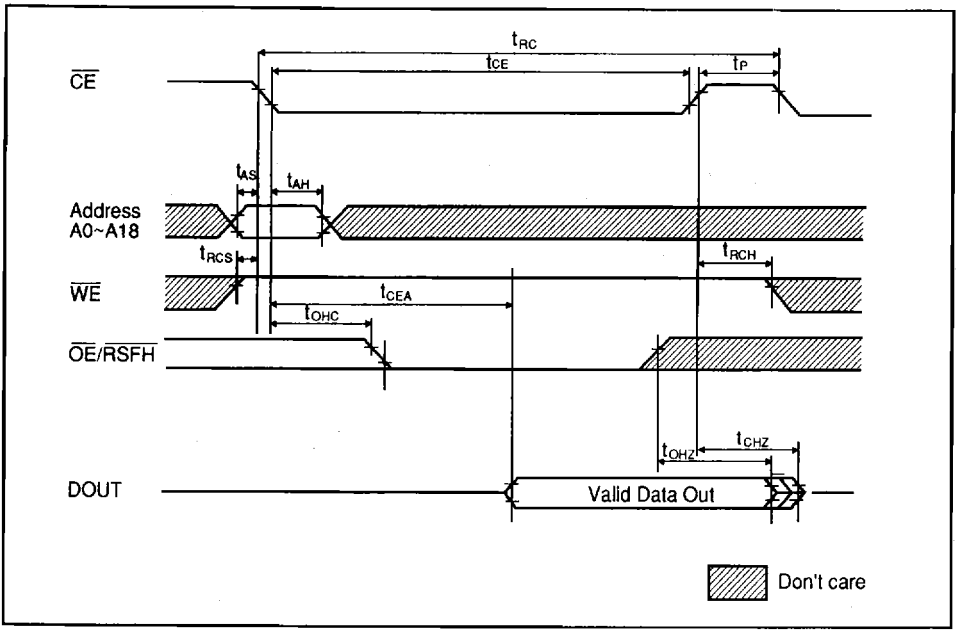
11. VIH (min.) and VIL (max.) are input timing reference levels for measurement. The transition time is measured between VIL and VIH.

12. 2048 cycles of refresh must be applied within 15 µs after the end of self refreshing to satisfy 2048 cycles/32ms.

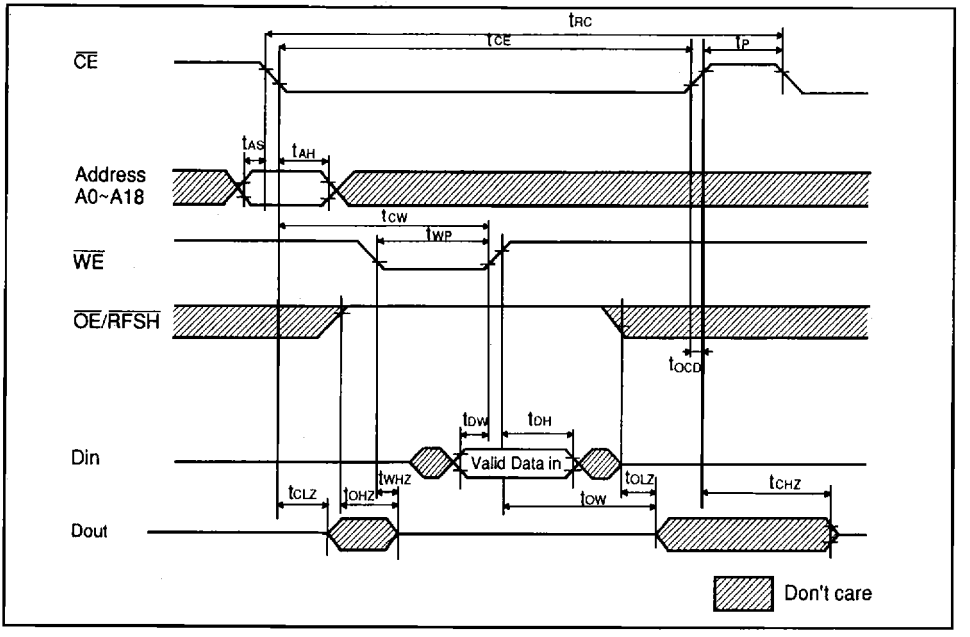
13. tFAS and tRFS are not applied in the -D version.

TIMING WAVEFORMS

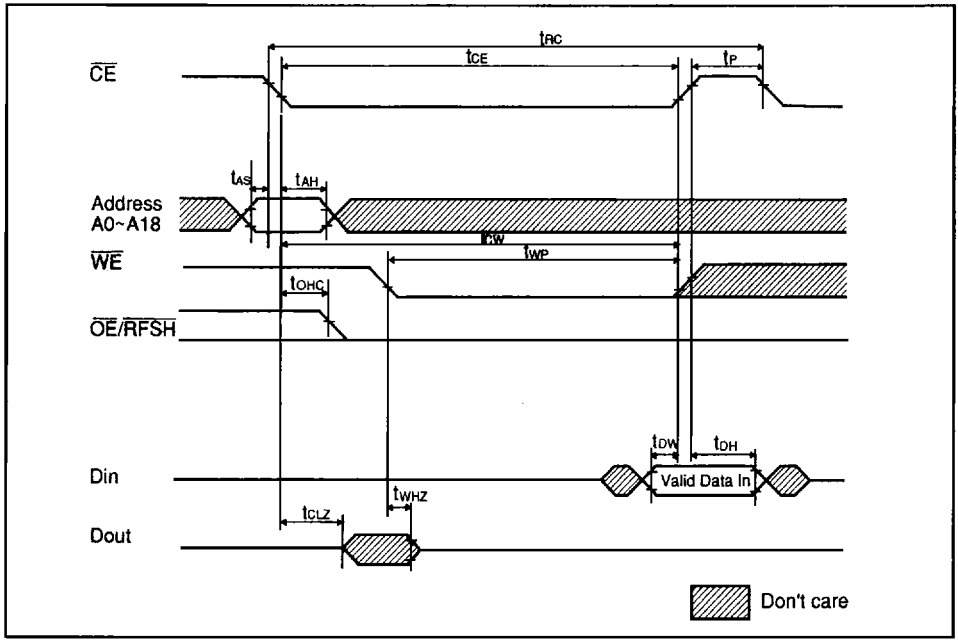
READ CYCLE



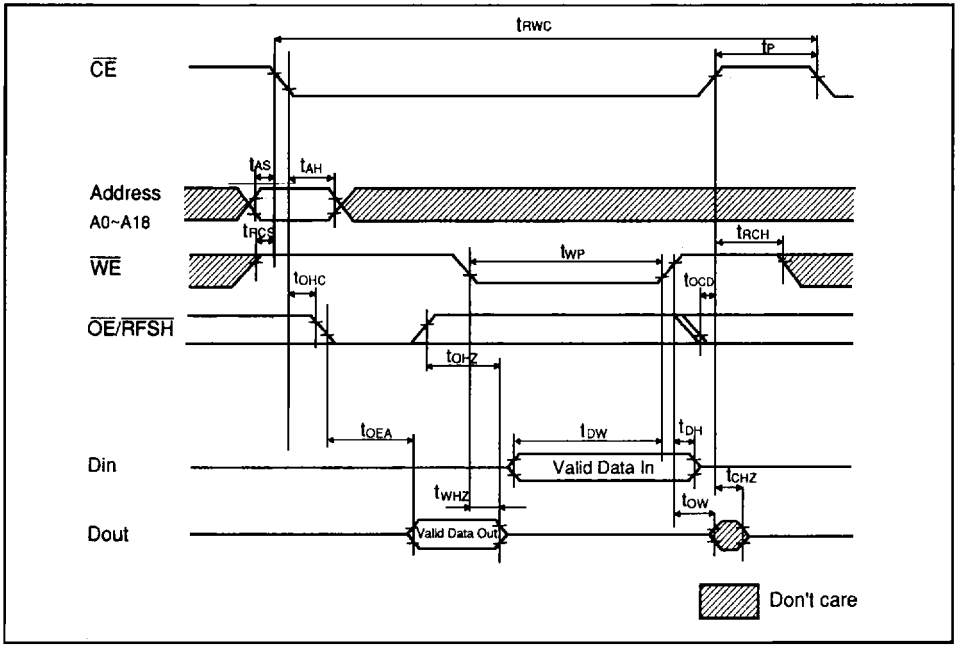
WRITE CYCLE 1 (OE High)



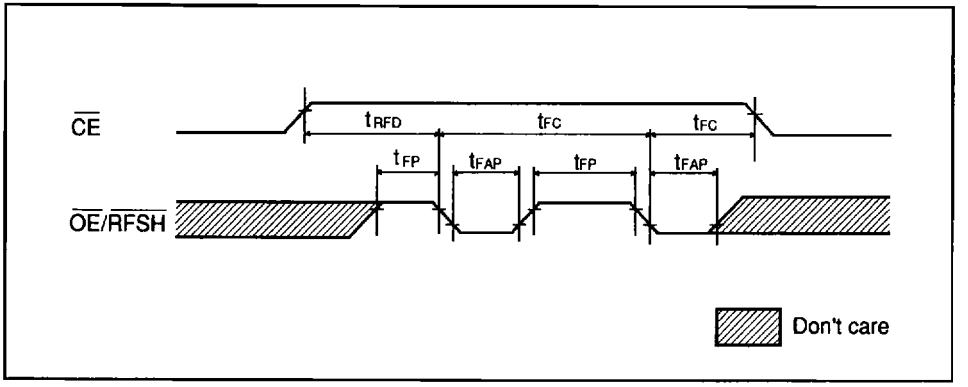
WRITE CYCLE 2 ($\overline{OE}$ Low)



READ MODIFY WRITE



AUTO-REFRESH CYCLE



SELF REFRESH (L VERSION ONLY)