



Programmable System Frequency Generator for PII/III™

Recommended Application:

810/810E and Solano (815) type chipset

Output Features:

- 2 - CPUs @ 2.5V
- 13 - SDRAM @ 3.3V
- 3 - 3V66 @ 3.3V
- 8 - PCI @3.3V
- 1 - 24/48MHz@ 3.3V
- 1 - 48MHz @ 3.3V fixed
- 1 - REF @3.3V, 14.318MHz

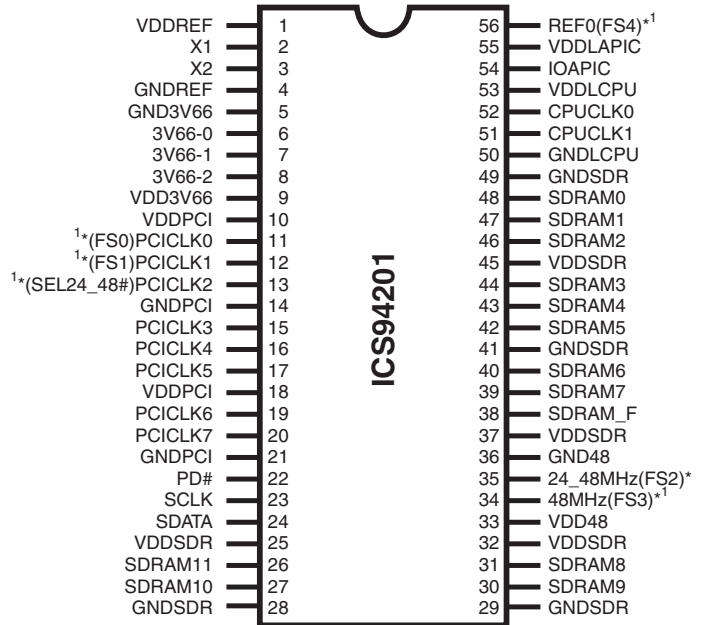
Features:

- Programmable output frequency.
- Programmable output rise/fall time for PCI and SDRAM clocks.
- Programmable 3V66 to PCI skew.
- Spread spectrum for EMI control with programmable spread percentage.
- Watchdog timer technology to reset system if over-clocking causes malfunction.
- Support power management through PD#.
- Uses external 14.318MHz crystal.
- FS pins for frequency select

Key Specifications:

- CPU Output Jitter: <250ps
- IOAPIC Output Jitter: <500ps
- 48MHz, 3V66, PCI Output Jitter: <500ps
- CPU Output Skew: <175ps
- PCI Output Skew: <500ps
- 3V66 Output Skew <175ps
- For group skew timing, please refer to the Group Timing Relationship Table.

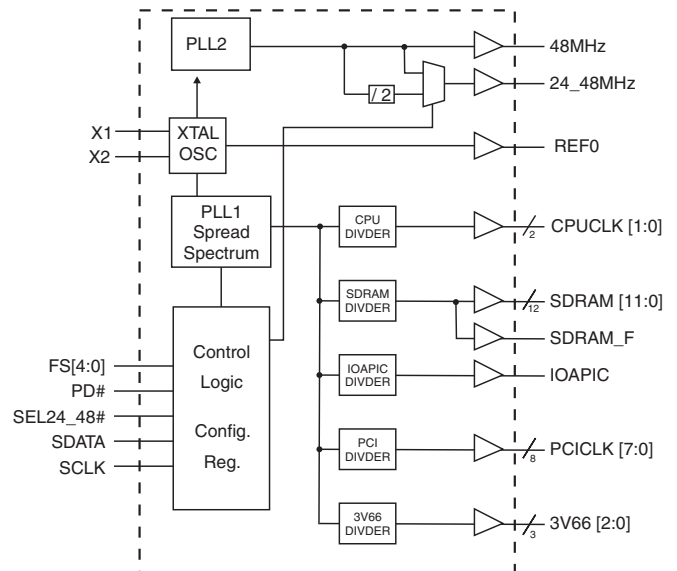
Pin Configuration



56-Pin 300 mil SSOP

1. These pins will have 1.5 to 2X drive strength.
- * 120K ohm pull-up to VDD on indicated inputs.

Block Diagram



ICS94201



General Description

The **ICS94201** is a single chip clock solution for desktop designs using the 810/810E and Solano style chipset. It provides all necessary clock signals for such a system.

The **ICS94201** belongs to ICS new generation of programmable system clock generators. It employs serial programming I²C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking.

Spread spectrum typically reduces system EMI by 7dB to 8dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding.

Pin Configuration

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|--|----------------------|------|---|
| 1, 9, 10, 18, 25, 32, 33, 37, 45 | VDD | PWR | 3.3V power supply |
| 2 | X1 | IN | Crystal input, has internal load cap (33pF) and feedback resistor from X2 |
| 3 | X2 | OUT | Crystal output, nominally 14.318MHz. Has internal load cap (33pF) |
| 4, 5, 14, 21, 28, 29, 36, 41, 49 | GND | PWR | Ground pins for 3.3V supply |
| 8, 7, 6 | 3V66 [2:0] | OUT | 3.3V Fixed 66MHz clock outputs for HUB |
| 11 | PCICLK0 ¹ | OUT | 3.3V PCI clock output, with Synchronous CPUCLKs |
| | FS0 | IN | Logic input frequency select bit. Input latched at power on. |
| 12 | PCICLK1 ¹ | OUT | 3.3V PCI clock output, with Synchronous CPUCLKs |
| | FS1 | IN | Logic input frequency select bit. Input latched at power on. |
| 13 | SEL_24_48# | IN | Logic input to select output. |
| | PCICLK2 ¹ | OUT | 3.3V PCI clock output, with Synchronous CPUCLKs |
| 20, 19, 17, 16, 15 | PCICLK [7:3] | OUT | 3.3V PCI clock outputs, with Synchronous CPUCLKs |
| 22 | PD# | IN | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. |
| 23 | SCLK | IN | Clock input of I ² C input |
| 24 | SDATA | OUT | Data input for I ² C serial input. |
| 34 | FS3 | IN | Logic input frequency select bit. Input latched at power on. |
| | 48MHz | OUT | 3.3V Fixed 48MHz clock output for USB |
| 35 | FS2 | IN | Logic input frequency select bit. Input latched at power on. |
| | 24_48MHz | OUT | 3.3V 24_48MHz output, selectable through pin 13, default is 24MHz. |
| 38 | SDRAM_F | OUT | 3.3V SDRAM output can be turned off through I ² C |
| 48, 47, 46, 44, 43, 42, 40, 39, 31, 30, 27, 26 | SDRAM [11:0] | OUT | 3.3V output. All SDRAM outputs can be turned off through I ² C |
| 50 | GNDL | PWR | Ground for 2.5V power supply for CPU & APIC |
| 51, 52 | CPUCLK [1:0] | OUT | 2.5V Host bus clock output. Output frequency derived from FS pins. |
| 53, 55 | VDDL | PWR | 2.5V power supply for CPU, IOAPIC |
| 54 | IOAPIC | OUT | 2.5V clock outputs running at 16.67MHz. |
| 56 | FS4 | IN | Logic input frequency select bit. Input latched at power on. |
| | REF0 ¹ | OUT | 3.3V, 14.318MHz reference clock output. |



General I²C serial interface information for the ICS94201

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte 0 through Byte 28** (see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| How to Write: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D2 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Byte 6 | |
| | ACK |
| ○ | |
| ○ | ○ |
| ○ | ○ |
| | ○ |
| Byte 26 | |
| | ACK |
| Byte 27 | |
| | ACK |
| Byte 28 | |
| | ACK |
| Stop Bit | |

*See notes on the following page.

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends **Byte 0 through byte 6 (default)**
- ICS clock sends **Byte 0 through byte X (if X_(H) was written to byte 6)**.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read: | |
|---|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D3 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| | Byte 6 |
| ACK | |
| If 7 _H has been written to B6 | Byte 7 |
| ACK | |
| ○ | ○ |
| ○ | ○ |
| ○ | ○ |
| | |
| If 1A _H has been written to B6 | Byte26 |
| ACK | |
| If 1B _H has been written to B6 | Byte 27 |
| ACK | |
| If 1C _H has been written to B6 | Byte 28 |
| ACK | |
| Stop Bit | |



Brief I²C registers description for ICS94201 Programmable System Frequency Generator

| Register Name | Byte | Description | Pwd Default |
|--|------------|---|---|
| Functionality & Frequency Select Register | 0 | Output frequency, hardware / I ² C frequency select, spread spectrum & output enable control register. | See individual byte description |
| Output Control Registers | 1-5 | Active / inactive output control registers. | See individual byte description |
| Byte Count Read Back Register | 6 | Writing to this register will configure byte count and how many byte will be read back. Do not write 00 _H to this byte. | 06 _H |
| Latched Inputs Read Back Register | 7 | The inverse of the latched inputs level could be read back from this register. | See individual byte description |
| Watchdog Control Registers | 8 Bit[6:0] | Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register. | 000,0000 |
| VCO Control Selection Bit | 8 Bit[7] | This bit selects whether the output frequency is controlled by hardware/byte 0 configurations or byte 14&15 programming. | 0 |
| Watchdog Timer Count Register | 9 | Writing to this register will configure the number of seconds for the watchdog timer to reset. | FF _H |
| ICS Reserved Register | 10 | This is an unused register. Writing to this register will not affect device functionality. | 00 _H |
| Device ID, Vendor ID & Revision ID Registers | 11-12 | Byte 11 bit[3:0] is ICS vendor id - 0001. Other bits in these 2 registers designate device revision ID of this part. | See individual byte description |
| ICS Reserved Register | 13 | Don't write into this register, writing 1's will cause malfunction. | 00 _H |
| VCO Frequency Control Registers | 14-15 | These registers control the dividers ratio into the phase detector and thus control the VCO output frequency. | Depend on hardware/byte 0 configuration |
| Spread Spectrum Control Registers | 16-17 | These registers control the spread percentage amount. | Depend on hardware/byte 0 configuration |
| Output Dividers Control Registers | 18-20 | Changing bits in these registers result in frequency divider ratio changes. Incorrect configuration of group output divider ratio can cause system malfunction. | Depend on hardware/byte 0 configuration |
| Group Skews Control Registers | 21-23 | Increment or decrement the group skew amount as compared to the initial skew. | See individual byte description |
| Output Rise/Fall Time Select Registers | 24 | These registers will control the group rise and fall time. | See individual byte description |

Notes:

- The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to read back is defined by writing to byte 6.**
- When writing to bytes 14 - 15, bytes 16 - 17 and bytes 18 - 20, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
- The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
- The input is operating at 3.3V logic levels.
- The data byte format is 8-bit bytes.
- To simplify the clock generator I²C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
- At power-on, all registers are set to a default condition, as shown.



Byte 0: Functionality and frequency select register (Default=0)

| Bit | Description | | | | | | | | | | | | | PWD |
|-------------|---|------|------|------|------|---------|--------|------|--------|--------|--------|--------|--------|--------|
| Bit | Bit2 | Bit7 | Bit6 | Bit5 | Bit4 | VCO/REF | VCO | VCO/ | CPUCLK | SDRAM | 3V66 | PCICLK | IOAPIC | PWD |
| | FS4 | FS3 | FS2 | FS1 | FS0 | Divider | MHz | CPU | MHz | MHz | MHz | MHz | MHz | |
| Bit (2,7:4) | 0 | 0 | 0 | 0 | 0 | 501/18 | 398.52 | 6 | 66.43 | 99.65 | 66.43 | 33.21 | 16.61 | Note 1 |
| | 0 | 0 | 0 | 0 | 1 | 352/14 | 360.00 | 6 | 60.00 | 90.00 | 60.00 | 30.00 | 15.00 | |
| | 0 | 0 | 0 | 1 | 0 | 504/18 | 400.91 | 6 | 66.80 | 100.20 | 66.80 | 33.40 | 16.70 | |
| | 0 | 0 | 0 | 1 | 1 | 315/11 | 410.02 | 6 | 68.33 | 102.50 | 68.33 | 34.17 | 17.08 | |
| | 0 | 0 | 1 | 0 | 0 | 440/15 | 420.00 | 6 | 70.00 | 105.00 | 70.00 | 35.00 | 17.50 | |
| | 0 | 0 | 1 | 0 | 1 | 440/14 | 450.00 | 6 | 75.00 | 112.50 | 75.00 | 37.50 | 18.75 | |
| | 0 | 0 | 1 | 1 | 0 | 503/15 | 480.14 | 6 | 80.00 | 120.00 | 80.00 | 40.00 | 20.00 | |
| | 0 | 0 | 1 | 1 | 1 | 313/9 | 497.95 | 6 | 83.00 | 124.50 | 83.00 | 41.50 | 20.75 | |
| | 0 | 1 | 0 | 0 | 0 | 515/37 | 199.29 | 2 | 99.65 | 99.65 | 66.43 | 33.21 | 16.61 | |
| | 0 | 1 | 0 | 0 | 1 | 440/35 | 180.29 | 2 | 90.00 | 90.00 | 60.00 | 30.00 | 15.00 | |
| | 0 | 1 | 0 | 1 | 0 | 518/37 | 200.45 | 2 | 100.23 | 100.23 | 66.84 | 33.41 | 16.70 | |
| | 0 | 1 | 0 | 1 | 1 | 446/31 | 206.00 | 2 | 103.00 | 103.00 | 68.67 | 34.33 | 17.17 | |
| | 0 | 1 | 1 | 0 | 0 | 484/33 | 210.00 | 2 | 105.00 | 105.00 | 70.00 | 35.00 | 17.50 | |
| | 0 | 1 | 1 | 0 | 1 | 507/33 | 219.98 | 2 | 110.00 | 110.00 | 73.33 | 36.67 | 18.33 | |
| | 0 | 1 | 1 | 1 | 0 | 514/32 | 229.99 | 2 | 115.00 | 115.00 | 76.67 | 38.33 | 19.17 | |
| | 0 | 1 | 1 | 1 | 1 | 447/16 | 400.01 | 2 | 200.00 | 200.00 | 133.33 | 66.66 | 33.33 | |
| | 1 | 0 | 0 | 0 | 0 | 501/18 | 398.52 | 3 | 132.86 | 132.86 | 66.43 | 33.21 | 16.61 | |
| | 1 | 0 | 0 | 0 | 1 | 454/13 | 500.03 | 3 | 166.67 | 166.67 | 83.34 | 41.67 | 20.83 | |
| | 1 | 0 | 0 | 1 | 0 | 504/18 | 400.91 | 3 | 133.64 | 133.64 | 66.82 | 33.41 | 16.70 | |
| | 1 | 0 | 0 | 1 | 1 | 488/17 | 411.02 | 3 | 137.00 | 137.00 | 68.50 | 34.25 | 17.13 | |
| | 1 | 0 | 1 | 0 | 0 | 440/15 | 420.00 | 3 | 140.00 | 140.00 | 70.00 | 35.00 | 17.50 | |
| | 1 | 0 | 1 | 0 | 1 | 395/13 | 435.05 | 3 | 145.00 | 145.00 | 72.50 | 36.25 | 18.13 | |
| | 1 | 0 | 1 | 1 | 0 | 440/14 | 450.00 | 3 | 150.00 | 150.00 | 75.00 | 37.50 | 18.75 | |
| | 1 | 0 | 1 | 1 | 1 | 503/15 | 480.14 | 3 | 160.00 | 160.00 | 80.00 | 40.00 | 20.00 | |
| | 1 | 1 | 0 | 0 | 0 | 501/18 | 398.52 | 3 | 132.86 | 99.65 | 66.93 | 33.21 | 16.61 | |
| | 1 | 1 | 0 | 0 | 1 | 454/13 | 500.03 | 3 | 166.67 | 125.00 | 83.34 | 41.67 | 20.83 | |
| | 1 | 1 | 0 | 1 | 0 | 504/18 | 400.91 | 3 | 133.64 | 100.23 | 66.82 | 33.41 | 16.7 | |
| | 1 | 1 | 0 | 1 | 1 | 488/17 | 411.02 | 3 | 137.00 | 102.75 | 68.50 | 34.25 | 17.13 | |
| | 1 | 1 | 1 | 0 | 0 | 440/15 | 420.00 | 3 | 140.00 | 105.00 | 70.00 | 35.00 | 17.50 | |
| | 1 | 1 | 1 | 0 | 1 | 395/13 | 435.05 | 3 | 145.00 | 108.75 | 72.50 | 36.25 | 18.13 | |
| | 1 | 1 | 1 | 1 | 0 | 440/14 | 450.00 | 3 | 150.00 | 112.50 | 75.00 | 37.50 | 18.75 | |
| | 1 | 1 | 1 | 1 | 1 | 503/15 | 480.14 | 3 | 160.00 | 120.00 | 80.00 | 40.00 | 20.00 | |
| Bit 3 | 0-Frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 2,7:4 | | | | | | | | | | | | | 0 |
| Bit 1 | 0- Normal 1- Spread spectrum enable ± 0.35% Center Spread | | | | | | | | | | | | | 1 |
| Bit 0 | 0- Running 1- Tristate all outputs | | | | | | | | | | | | | 0 |

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

ICS94201



Byte 1: Output Control Register (1 = enable, 0 = disable)

| Bit | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | - | X | FS3# |
| Bit 6 | - | X | FS0# |
| Bit 5 | - | X | FS2# |
| Bit 4 | 35 | 1 | 24MHz |
| Bit 3 | - | 1 | (Reserved) |
| Bit 2 | 34 | 1 | 48MHz |
| Bit 1 | - | 1 | (Reserved) |
| Bit 0 | 38 | 1 | SDRAM_F |

Byte 2: Output Control Register (1 = enable, 0 = disable)

| Bit | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | 39 | 1 | SDRAM7 |
| Bit 6 | 40 | 1 | SDRAM6 |
| Bit 5 | 42 | 1 | SDRAM5 |
| Bit 4 | 43 | 1 | SDRAM4 |
| Bit 3 | 44 | 1 | SDRAM3 |
| Bit 2 | 46 | 1 | SDRAM2 |
| Bit 1 | 47 | 1 | SDRAM1 |
| Bit 0 | 48 | 1 | SDRAM0 |

Byte 3: Output Control Register (1 = enable, 0 = disable)

| Bit | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | 20 | 1 | PCICLK7 |
| Bit 6 | 19 | 1 | PCICLK6 |
| Bit 5 | 17 | 1 | PCICLK5 |
| Bit 4 | 16 | 1 | PCICLK4 |
| Bit 3 | 15 | 1 | PCICLK3 |
| Bit 2 | 13 | 1 | PCICLK2 |
| Bit 1 | 12 | 1 | PCICLK1 |
| Bit 0 | 11 | 1 | PCICLK0 |

Byte 4: Output Control Register (1 = enable, 0 = disable)

| Bit | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | 8 | 1 | 3V66_2 |
| Bit 6 | 6 | 1 | 3V66_0 |
| Bit 5 | 7 | 1 | 3V66_1 |
| Bit 4 | - | X | FS4# |
| Bit 3 | 54 | 1 | IOAPIC |
| Bit 2 | - | X | FS1# |
| Bit 1 | 51 | 1 | CPUCLK1 |
| Bit 0 | 52 | 1 | CPUCLK0 |

Byte 5: Output Control Register (1 = enable, 0 = disable)

| Bit | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | - | 1 | (Reserved) |
| Bit 3 | 26 | 1 | SDRAM11 |
| Bit 2 | 27 | 1 | SDRAM10 |
| Bit 1 | 30 | 1 | SDRAM9 |
| Bit 0 | 31 | 1 | SDRAM8 |

Byte 6: Byte Count Read Back Register

| Bit | Pin# | PWD | Description |
|-------|------|-----|-----------------|
| Bit 7 | - | 0 | Reserved (Note) |
| Bit 6 | - | 0 | Reserved (Note) |
| Bit 5 | - | 0 | Reserved (Note) |
| Bit 4 | - | 0 | Reserved (Note) |
| Bit 3 | - | 0 | Reserved (Note) |
| Bit 2 | - | 1 | Reserved (Note) |
| Bit 1 | - | 1 | Reserved (Note) |
| Bit 0 | - | 0 | Reserved (Note) |

Note: Writing to this register will configure byte count and how many bytes will be read back, default is 6 bytes.

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default



Byte 7: Latch Inputs Readback Register

| Bit | PWD | Description |
|-------|-----|-------------|
| Bit 7 | 0 | (Reserved) |
| Bit 6 | 0 | (Reserved) |
| Bit 5 | 0 | (Reserved) |
| Bit 4 | X | FS4# |
| Bit 3 | X | FS3# |
| Bit 2 | X | FS2# |
| Bit 1 | X | FS1# |
| Bit 0 | X | FS0# |

Byte 8: VCO Control Selection Bit & Watchdog Timer Control Register

| Bit | PWD | Description |
|-------|-----|--------------------------------|
| Bit 7 | 0 | 0=Hw/B0 freq / 1=B14&15 freq |
| Bit 6 | 0 | WD Enable 0=disable / 1=enable |
| Bit 5 | 0 | WD Status 0=normal / 1=alarm |
| Bit 4 | 0 | WD Safe Frequency, FS4 |
| Bit 3 | 0 | WD Safe Frequency, FS3 |
| Bit 2 | 0 | WD Safe Frequency, FS2 |
| Bit 1 | 0 | WD Safe Frequency, FS1 |
| Bit 0 | 0 | WD Safe Frequency, FS0 |

Note: FS values in bit [0:4] will correspond to Byte 0 FS values. Default safe frequency is same as 00000 entry in byte0.

Byte 9: Watchdog Timer Count Register

| Bit | PWD | Description |
|-------|-----|--|
| Bit 7 | 1 | The decimal representation of these 8 bits correspond to 580ms or 2ms (selectable by byte 13 bit 4) the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 256X 580ms = 148 seconds |
| Bit 6 | 1 | |
| Bit 5 | 1 | |
| Bit 4 | 1 | |
| Bit 3 | 1 | |
| Bit 2 | 1 | |
| Bit 1 | 1 | |
| Bit 0 | 1 | |

Byte 10: ICS Reserved Register

| Bit | PWD | Description |
|-------|-----|-------------|
| Bit 7 | 0 | (Reserved) |
| Bit 6 | 0 | (Reserved) |
| Bit 5 | 0 | (Reserved) |
| Bit 4 | 0 | (Reserved) |
| Bit 3 | 0 | (Reserved) |
| Bit 2 | 0 | (Reserved) |
| Bit 1 | 0 | (Reserved) |
| Bit 0 | 0 | (Reserved) |

Note: This is an unused register. Writing to this register will not affect device performance or functionality.

Byte 11: Vender ID & Device ID Register

| Bit | PWD | Description |
|-------|-----|-------------|
| Bit 7 | X | Device ID |
| Bit 6 | X | Device ID |
| Bit 5 | X | Device ID |
| Bit 4 | X | Device ID |
| Bit 3 | 0 | Vendor ID |
| Bit 2 | 0 | Vendor ID |
| Bit 1 | 0 | Vendor ID |
| Bit 0 | 1 | Vendor ID |

Note: ICS Vendor ID is 0001 as in Number 1 in frequency generation.

Byte 12: Revision ID Register

| Bit | PWD | Description |
|-------|-----|-------------|
| Bit 7 | X | Revision ID |
| Bit 6 | X | Revision ID |
| Bit 5 | X | Revision ID |
| Bit 4 | X | Revision ID |
| Bit 3 | X | Device ID |
| Bit 2 | X | Device ID |
| Bit 1 | X | Device ID |
| Bit 0 | X | Device ID |

Note: Device ID and Revision ID values will be based on individual device and its revision.

Notes:

1. PWD = Power on Default



Byte 13: ICS Reserved Register

| Bit | PWD | Description |
|-------|-----|--|
| Bit 7 | 0 | (Reserved) |
| Bit 6 | 0 | (Reserved) |
| Bit 5 | 0 | (Reserved) |
| Bit 4 | 0 | W0 timer base select 0=580ms 1=2ms |
| Bit 3 | 0 | (Reserved) |
| Bit 2 | 0 | (Reserved) |
| Bit 1 | 0 | (Reserved) |
| Bit 0 | 0 | (Reserved) |

Note: DON'T write a '1' into this register, it will cause malfunction.

Byte 14: VCO Frequency Control Register

| Bit | PWD | Description |
|-------|-----|------------------|
| Bit 7 | X | VCO Divider Bit0 |
| Bit 6 | X | REF Divider Bit6 |
| Bit 5 | X | REF Divider Bit5 |
| Bit 4 | X | REF Divider Bit4 |
| Bit 3 | X | REF Divider Bit3 |
| Bit 2 | X | REF Divider Bit2 |
| Bit 1 | X | REF Divider Bit1 |
| Bit 0 | X | REF Divider Bit0 |

Note: The decimal representation of these 7 bits (Byte 14 [6:0]) + 2 is equal to the REF divider value .

Byte 15: VCO Frequency Control Register

| Bit | PWD | Description |
|-------|-----|------------------|
| Bit 7 | X | VCO Divider Bit8 |
| Bit 6 | X | VCO Divider Bit7 |
| Bit 5 | X | VCO Divider Bit6 |
| Bit 4 | X | VCO Divider Bit5 |
| Bit 3 | X | VCO Divider Bit4 |
| Bit 2 | X | VCO Divider Bit3 |
| Bit 1 | X | VCO Divider Bit2 |
| Bit 0 | X | VCO Divider Bit1 |

Note: The decimal representation of these 9 bits (Byte 15 bit [7:0] & Byte 14 bit [7]) + 8 is equal to the VCO divider value. For example if VCO divider value of 36 is desired, user need to program $36 - 8 = 28$, namely, 0, 00011100 into byte 15 bit & byte 14 bit 7.

VCO Programming Constrains

VCO Frequency 150MHz to 500MHz

VCO Divider Range 8 to 519

REF Divider Range 2 to 129

Phase Detector Stability 0.3536 to 1.4142

Useful Formula

VCO Frequency = $14.31818 \times \text{VCO/REF divider value}$

Phase Detector Stabiliy = $14.038 \times (\text{VCO divider value})^{-0.5}$

To program the VCO frequency for over-clocking.

0. Before trying to program our clock manually, consider using ICS provided software utilities for easy programming.
1. Select the frequency you want to over-clock from with the desired gear ratio (i.e. CPU:SDRAM:3V66:PCI ratio) by writing to byte 0, or using initial hardware power up frequency.
2. Write 0001, 1001 (19H) to byte 6 for readback of 25 bytes (byte 0-24).
3. Read back byte 16-24 and copy values in these registers.
4. Re-initialize the write sequence.
5. Write a '1' to byte 8 bit 7 indicating you want to use byte 14 and 15 to control the VCO frequency.
6. Write to byte 14 & 15 with the desired VCO & REF divider values.
7. Write to byte 16 to 24 with the values you copy from step 3. This maintains the output divider mux controls the same gear ratio.
8. The above procedure is only needed when changing the VCO for the 1st pass. If VCO frequency needs to be changed again, user only needs to write to byte 14 and 15 unless the system is to reboot.



Note:

1. User needs to ensure step 3 & 7 is carried out. Systems with the wrong spread percentage and/or group to group divider ratio programmed into bytes 16-20 could be unstable. Step 3 & 7 assure the correct spread and gear ratio.
2. If VCO, REF divider values or phase detector stability are out of range, the device may fail to function correctly.
3. Follow min and max VCO frequency range provided. Internal PLL could be unstable if VCO frequency is too fast or too slow. Use $14.31818\text{MHz} \times \text{VCO/REF divider values}$ to calculate the VCO frequency (MHz).
4. Users can also utilize software utility provided to program the VCO frequency from ICS Application Engineering.
5. Spread percent needs to be calculated based on VCO frequency, spread modulation frequency and spread amount desired. See Application note for software support.

Byte 16: Spread Sectrum Control Register

| Bit | PWD | Description |
|-------|-----|----------------------|
| Bit 7 | X | Spread Spectrum Bit7 |
| Bit 6 | X | Spread Spectrum Bit6 |
| Bit 5 | X | Spread Spectrum Bit5 |
| Bit 4 | X | Spread Spectrum Bit4 |
| Bit 3 | X | Spread Spectrum Bit3 |
| Bit 2 | X | Spread Spectrum Bit2 |
| Bit 1 | X | Spread Spectrum Bit1 |
| Bit 0 | X | Spread Spectrum Bit0 |

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 17: Spread Spectrum Control Register

| Bit | PWD | Description |
|-------|-----|-----------------------|
| Bit 7 | X | Divider control Bit26 |
| Bit 6 | 0 | Divider control Bit25 |
| Bit 5 | X | Divider control Bit24 |
| Bit 4 | X | Spread Spectrum Bit12 |
| Bit 3 | X | Spread Spectrum Bit11 |
| Bit 2 | X | Spread Spectrum Bit10 |
| Bit 1 | X | Spread Spectrum Bit9 |
| Bit 0 | X | Spread Spectrum Bit8 |

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 18: Output Dividers Control Register

| Bit | PWD | Description |
|-------|-----|---------------------------------|
| Bit 7 | X | Output Divider MUX Control Bit7 |
| Bit 6 | X | Output Divider MUX Control Bit6 |
| Bit 5 | X | Output Divider MUX Control Bit5 |
| Bit 4 | X | Output Divider MUX Control Bit4 |
| Bit 3 | X | Output Divider MUX Control Bit3 |
| Bit 2 | X | Output Divider MUX Control Bit2 |
| Bit 1 | X | Output Divider MUX Control Bit1 |
| Bit 0 | X | Output Divider MUX Control Bit0 |

Note: Changing bits in these registers results in frequency divider ratio changes. Incorrect configuration of group gear ratio can cause system malfunction.

Byte 19: Output Dividers Control Register

| Bit | PWD | Description |
|-------|-----|----------------------------------|
| Bit 7 | X | Output Divider MUX Control Bit15 |
| Bit 6 | X | Output Divider MUX Control Bit14 |
| Bit 5 | X | Output Divider MUX Control Bit13 |
| Bit 4 | X | Output Divider MUX Control Bit12 |
| Bit 3 | X | Output Divider MUX Control Bit11 |
| Bit 2 | X | Output Divider MUX Control Bit10 |
| Bit 1 | X | Output Divider MUX Control Bit9 |
| Bit 0 | X | Output Divider MUX Control Bit8 |

Note: Changing bits in these registers results in frequency divider ratio changes. Incorrect configuration of group gear ratio can cause system malfunction.

Notes:

1. PWD = Power on Default
2. The power on default for byte 16-20 depends on the hardware (latch inputs FS[0:4]) or IIC (Byte 0 bit [1:7]) setting. Be sure to read back and re-write the values of these 5 registers when VCO frequency change is desired for the first pass.



Byte 20: Output Dividers Control Register

| Bit | PWD | Description |
|-------|-----|----------------------------------|
| Bit 7 | X | Output Divider MUX Control Bit23 |
| Bit 6 | X | Output Divider MUX Control Bit22 |
| Bit 5 | X | Output Divider MUX Control Bit21 |
| Bit 4 | X | Output Divider MUX Control Bit20 |
| Bit 3 | X | Output Divider MUX Control Bit19 |
| Bit 2 | X | Output Divider MUX Control Bit18 |
| Bit 1 | X | Output Divider MUX Control Bit17 |
| Bit 0 | X | Output Divider MUX Control Bit16 |

Note: Changing bits in these registers results in frequency divider ratio changes. Incorrect configuration of group gear ratio can cause system malfunction.

Byte 22: Group Skew Control Register

| Bit | PWD | Description |
|-------|-----|-----------------------|
| Bit 7 | 1 | 3V66 to PCI Skew Bit3 |
| Bit 6 | 0 | 3V66 to PCI Skew Bit2 |
| Bit 5 | 0 | 3V66 to PCI Skew Bit1 |
| Bit 4 | 1 | 3V66 to PCI Skew Bit0 |
| Bit 3 | 0 | (Reserved) |
| Bit 2 | 0 | (Reserved) |
| Bit 1 | 0 | (Reserved) |
| Bit 0 | 0 | (Reserved) |

Note: Default 3V66 to PCI skew is 2.5ns bit [7:4]=1001. Each increment or decrement of bit 4 to 7 will introduce 100ps delay or advance on all PCI clocks.

Byte 24: Output Rise/Fall Time Select Register

| Bit | PWD | Description |
|-------|-----|---------------------------|
| Bit 7 | 0 | (Reserved) |
| Bit 6 | 0 | REF 0=Normal, 1=Weak |
| Bit 5 | 0 | 24,48Mhz 0=Normal, 1=Weak |
| Bit 4 | 0 | (Reserved) |
| Bit 3 | 0 | PCI 0=Normal, 1=Weak |
| Bit 2 | 0 | 3V66 0=Normal, 1=Weak |
| Bit 1 | 0 | SDRAM 0=Normal, 1=Weak |
| Bit 0 | 0 | (Reserved) |

Byte 21: ICS Reserved Register

| Bit | PWD | Description |
|-------|-----|-------------|
| Bit 7 | 0 | (Reserved) |
| Bit 6 | 0 | (Reserved) |
| Bit 5 | 0 | (Reserved) |
| Bit 4 | 0 | (Reserved) |
| Bit 3 | 0 | (Reserved) |
| Bit 2 | 0 | (Reserved) |
| Bit 1 | 0 | (Reserved) |
| Bit 0 | 0 | (Reserved) |

Note: This is an unused register. Writing to this register will not affect device performance or functionality.

Byte 23: Group Skew Control Register

| Bit | PWD | Description |
|-------|-----|---------------------------|
| Bit 7 | 0 | (Reserved) |
| Bit 6 | 0 | (Reserved) |
| Bit 5 | 0 | (Reserved) |
| Bit 4 | 0 | (Reserved) |
| Bit 3 | 0 | 3V66 to IOAPIC Skew Bit 3 |
| Bit 2 | 1 | 3V66 to IOAPIC Skew Bit 2 |
| Bit 1 | 1 | 3V66 to IOAPIC Skew Bit 1 |
| Bit 0 | 1 | 3V66 to IOAPIC Skew Bit 0 |

Note: Default 3V66 to IOAPIC skew is 2.5ns bit [3:0]=0111. Each increment or decrement of bit 4 to 7 will introduce 100ps delay or advance on all IOAPIC clocks.

Notes:

1. PWD = Power on Default
2. The power on default for byte 16-20 depends on the hardware (latch inputs FS[0:4]) or I²C (Byte 0 bit [1:7]) setting. Be sure to read back and re-write the values of these 5 registers when VCO frequency change is desired for the first pass.
3. If Byte 8 bit 7 is driven to "1" meaning programming is intended, Byte 21-24 will lose their default power up value.



Absolute Maximum Ratings

| | |
|-------------------------------------|--------------------------------------|
| Core Supply Voltage | 4.6 V |
| I/O Supply Voltage | 3.6V |
| Logic Inputs | GND -0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |
| Case Temperature | 115°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Timing Relationship Table¹

| Group | CPU 66 MHz | | CPU 100 MHz | | CPU 133 MHz | | CPU 133 MHz | |
|---------------|---------------|-----------|---------------|-----------|---------------|-----------|---------------|-----------|
| | SDRAM 100 MHz | | SDRAM 100 MHz | | SDRAM 100 MHz | | SDRAM 133 MHz | |
| | Offset | Tolerance | Offset | Tolerance | Offset | Tolerance | Offset | Tolerance |
| CPU to SDRAM | 2.5 ns | 500 ps | 5.0 ns | 500 ps | 0.0 ns | 500 ps | 3.75 ns | 500 ps |
| CPU to 3V66 | 7.5 ns | 500 ps | 5.0 ns | 500 ps | 0.0 ns | 500 ps | 0.0 ns | 500 ps |
| SDRAM to 3V66 | 0.0 ns | 500 ps | 0.0 ns | 500 ps | 0.0 ns | 500 ps | 3.75 ns | 500 ps |
| 3V66 to PCI | 1.5-3.5ns | 500 ps | 1.5-3.5ns | 500 ps | 1.5-3.5ns | 500 ps | 1.5-3.5ns | 500 ps |
| PCI to IOAPIC | 0.0 ns | 1.0 ns | 0.0 ns | 1.0 ns | 0.0 ns | 1.0 ns | 0.0 ns | 1.0 ns |
| USB & DOT | Asynch | N/A | Asynch | N/A | Asynch | N/A | Asynch | N/A |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-----------------------|--|----------------------|--------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | -5 | | 5 | μA |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | | | μA |
| | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | | | |
| Operating Supply Current | I _{DD3.3OP} | C _L = max cap loads; CPU=66-133 MHz, SDRAM=100 MHz | | 334 | 350 | mA |
| | | CPU=133 MHz, SDRAM=133 MHz | | 465 | 500 | |
| | I _{DD2.5OP} | C _L = max cap loads; | | 20 | 70 | |
| Powerdown Current | I _{DD3.3PD} | C _L = 0 pF; Input address to VDD or GND | | 280 | 600 | μA |
| Input Frequency | F _i | V _{DD} = 3.3 V | | 14.318 | | MHz |
| Pin Inductance | L _{pin} | | | | 7 | nH |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{OUT} | Output pin capacitance | | | 6 | pF |
| | C _{INX} | X1 & X2 pins | 27 | | 45 | pF |
| Transition time ¹ | T _{trans} | To 1st crossing of target frequency | | | 3 | ms |
| Settling time ¹ | T _s | From 1st crossing to 1% target frequency | | | 3 | ms |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target frequency | | | 3 | ms |
| Delay ¹ | t _{PZH,tPZL} | Output enable delay (all outputs) | 1 | | 10 | ns |
| | t _{PHZ,tPLZ} | Output disable delay (all outputs) | 1 | | 10 | ns |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - CPU

$T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 2.5 \text{ V} \pm 5\%$; $C_L = 10 - 20 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-----------------|---|------|------|-----|----------|
| Output Impedance ¹ | R_{DSP2B} | $V_O = V_{DD} * (0.5)$ | 13.5 | 15 | 45 | Ω |
| Output Impedance ¹ | R_{DSN2B} | $V_O = V_{DD} * (0.5)$ | 13.5 | 16.5 | 45 | Ω |
| Output High Voltage | V_{OH2B} | $I_{OH} = -1 \text{ mA}$ | 2 | 2.48 | | V |
| Output Low Voltage | V_{OL2B} | $I_{OL} = 1 \text{ mA}$ | | 0.04 | 0.4 | V |
| Output High Current | I_{OH2B} | $V_{OH@MIN} = 1 \text{ V}$ | | -60 | -27 | mA |
| | | $V_{OH@MAX} = 2.375 \text{ V}$ | -27 | -7 | | |
| Output Low Current | I_{OL2B} | $V_{OL@MIN} = 1.2 \text{ V}$ | 27 | 63 | | mA |
| | | $V_{OL@MAX} = 0.3 \text{ V}$ | | 20 | 30 | |
| Rise Time ¹ | t_{r2B} | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.0 \text{ V}$ | 0.4 | 1 | 1.6 | ns |
| Fall Time ¹ | t_{f2B} | $V_{OH} = 2.0 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | 0.4 | 1 | 1.6 | ns |
| Duty Cycle ¹ | d_{t2B} | $V_T = 1.25 \text{ V}$ | 45 | 50 | 55 | % |
| Skew ¹ | t_{sk2B} | $V_T = 1.25 \text{ V}$ | | 30 | 175 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{jyc-cyc2B}$ | $V_T = 1.25 \text{ V}$, CPU 66, SDRAM 100 | | 300 | 350 | ps |
| | | CPU 100, SDRAM 100 | | 240 | 250 | |
| | | CPU 133, SDRAM 100 | | 400 | 500 | |
| | | CPU 133, SDRAM 133 | | 300 | 350 | |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

$T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 10 - 30 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|---|-----|-----|------|----------|
| Output Impedance ¹ | R_{DSP1} | $V_O = V_{DD} * (0.5)$ | 12 | | 55 | Ω |
| Output Impedance ¹ | R_{DSN1} | $V_O = V_{DD} * (0.5)$ | 12 | | 55 | Ω |
| Output High Voltage | V_{OH1} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 1 \text{ mA}$ | | | 0.55 | V |
| Output High Current | I_{OH1} | $V_{OH@MIN} = 1.0 \text{ V}$ | | | -33 | mA |
| | | $V_{OH@MAX} = 3.135 \text{ V}$ | -33 | | | |
| Output Low Current | I_{OL1} | $V_{OL@MIN} = 1.95 \text{ V}$ | 30 | | | mA |
| | | $V_{OL@MAX} = 0.4 \text{ V}$ | | | 38 | |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$ | 0.4 | 1 | 1.6 | ns |
| Fall Time ¹ | t_{f1} | $V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | 0.4 | 0.9 | 1.6 | ns |
| Duty Cycle ¹ | d_{t1} | $V_T = 1.5 \text{ V}$ | 45 | 49 | 55 | % |
| Skew ¹ | t_{sk1} | $V_T = 1.5 \text{ V}$ | | 35 | 175 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{jyc-cyc1}$ | $V_T = 1.5 \text{ V}$ | | 220 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - IOAPIC

T_A = 0 - 70° C; V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|------------------------|--|-----|-----|-----|-------|
| Output Impedance ¹ | R _{DSP4B} | V _O =V _{DD} *(0.5) | 9 | | 3 | Ω |
| Output Impedance ¹ | R _{DSN4B} | V _O =V _{DD} *(0.5) | 9 | | 30 | Ω |
| Output High Voltage | V _{OH4B} | I _{OH} = -5.5 mA | 2 | | | V |
| Output Low Voltage | V _{OL4B} | I _{OL} = 9 mA | | | 0.4 | V |
| Output High Current | I _{OH4B} | V _{OH@MIN} = 1.4 V | | | -21 | mA |
| | | V _{OH@MAX} = 2.5V | -36 | | | |
| Output Low Current | I _{OL4B} | V _{OL@MIN} = 1.0 V | 36 | | | mA |
| | | V _{OL@MAX} =0.2V | | | 31 | |
| Rise Time ¹ | t _{r4B} | V _{OL} = 0.4 V, V _{OH} = 2.0 V | 0.4 | 1.2 | 1.6 | ns |
| Fall Time ¹ | t _{f4B} | V _{OH} = 2.0 V, V _{OL} = 0.4 V | 0.4 | 1.1 | 1.6 | ns |
| Duty Cycle ¹ | d _{t4B} | V _T = 1.25 V | 45 | 50 | 55 | % |
| Jitter, Cycle-to-cycle ¹ | t _{jyc-cyc4B} | V _T = 1.25 V | | 240 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%; C_L = 20 - 30 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-----------------------|--|-----|-----|-----|-------|
| Output Impedance ¹ | R _{DSP3} | V _O =V _{DD} *(0.5) | 10 | | 24 | Ω |
| Output Impedance ¹ | R _{DSN3} | V _O =V _{DD} *(0.5) | 10 | | 24 | Ω |
| Output High Voltage | V _{OH3} | I _{OH} = -1 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL3} | I _{OL} = 1 mA | | | 0.4 | V |
| Output High Current | I _{OH3} | V _{OH@MIN} = 2 V | | | -46 | mA |
| | | V _{OH@MAX} = 3.135V | -54 | | | |
| Output Low Current | I _{OL3} | V _{OL@MIN} = 1 V | 54 | | | mA |
| | | V _{OL@MAX} =0.4V | | | 53 | |
| Rise Time ¹ | t _{r3} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 0.4 | 0.9 | 1.6 | ns |
| Fall Time ¹ | t _{f3} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 0.4 | 0.8 | 1.6 | ns |
| Duty Cycle ¹ | d ₃ | V _T = 1.5 V | 45 | 49 | 55 | % |
| Skew ¹ | t _{sk3} | V _T = 1.5 V | | 100 | 250 | ps |
| Jitter, cycle-to-cycle ¹ | t _{jyc-cyc3} | V _T = 1.5 V | | 350 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $C_L = 40\text{ pF}$ for PCI0-1, $C_L = 10 - 30\text{ pF}$ for other PCIs (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|--|-----|-----|------|----------|
| Output Impedance ¹ | R_{DSP1} | $V_O = V_{DD} * (0.5)$ | 12 | | 55 | Ω |
| Output Impedance ¹ | R_{DSN1} | $V_O = V_{DD} * (0.5)$ | 12 | | 55 | Ω |
| Output High Voltage | V_{OH1} | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 1\text{ mA}$ | | | 0.55 | V |
| Output High Current | I_{OH1} | $V_{OH@MIN} = 1\text{ V}$ | | | -33 | mA |
| | | $V_{OH@MAX} = 3.135\text{ V}$ | -33 | | | |
| Output Low Current | I_{OL1} | $V_{OL@MIN} = 1.95\text{ V}$ | 30 | | | mA |
| | | $V_{OL@MAX} = 0.4\text{ V}$ | | | 38 | |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.4\text{ V}, V_{OH} = 2.4\text{ V}, \text{ PCI0-3}$ | 0.5 | 1.8 | 2 | ns |
| | | PCI3-7 | | 2.2 | 2.5 | |
| Fall Time ¹ | t_{f1} | $V_{OL} = 2.4\text{ V}, V_{OH} = 0.4\text{ V}, \text{ PCI0-3}$ | 0.5 | 1.8 | 2 | ns |
| | | PCI3-7 | | 2.3 | 2.5 | |
| Duty Cycle ¹ | d_{11} | $V_T = 1.5\text{ V}$ | 45 | 51 | 55 | % |
| Skew ¹ | t_{sk1} | $V_T = 1.5\text{ V}$ | | 150 | 500 | ps |
| Jitter, cycle-to-cycle ¹ | $t_{jyc-cyc1}$ | $V_T = 1.5\text{ V}$ | | 200 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 24_48MHz, 48MHz

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 10-20\text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|--|-----|------|------|----------|
| Output Impedance ¹ | R_{DSP5} | $V_O = V_{DD} * (0.5)$ | 20 | | 60 | Ω |
| Output Impedance ¹ | R_{DSN5} | $V_O = V_{DD} * (0.5)$ | 20 | | 60 | Ω |
| Output High Voltage | V_{OH5} | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 1\text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH@MIN} = 1.0\text{ V}$ | | | -23 | mA |
| | | $V_{OH@MAX} = 3.135\text{ V}$ | -29 | | | |
| Output Low Current | I_{OL5} | $V_{OL@MIN} = 1.95\text{ V}$ | 29 | | | mA |
| | | $V_{OL@MAX} = 0.4\text{ V}$ | | | 27 | |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4\text{ V}, V_{OH} = 2.4\text{ V}$ | 0.4 | 2 | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4\text{ V}, V_{OL} = 0.4\text{ V}$ | 0.4 | 2 | 4 | ns |
| Duty Cycle ¹ | d_{i5} | $V_T = 1.5\text{ V}$ | 45 | 53 | 55 | % |
| Jitter, cycle-to-cycle ¹ | $t_{jyc-cyc5}$ | $V_T = 1.5\text{ V}, \text{ Fixed clocks}$ | | 200 | 500 | ps |
| | | $V_T = 1.5\text{ V}, \text{ Ref clocks}$ | | 2300 | 3000 | |

¹Guaranteed by design, not 100% tested in production.



Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS94201 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

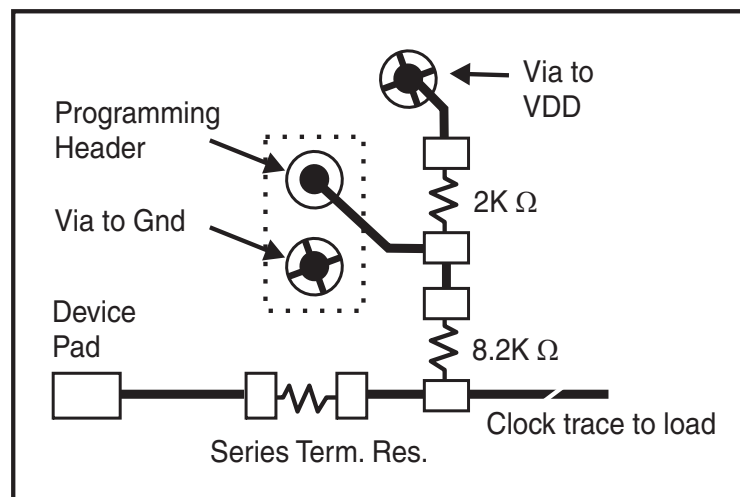
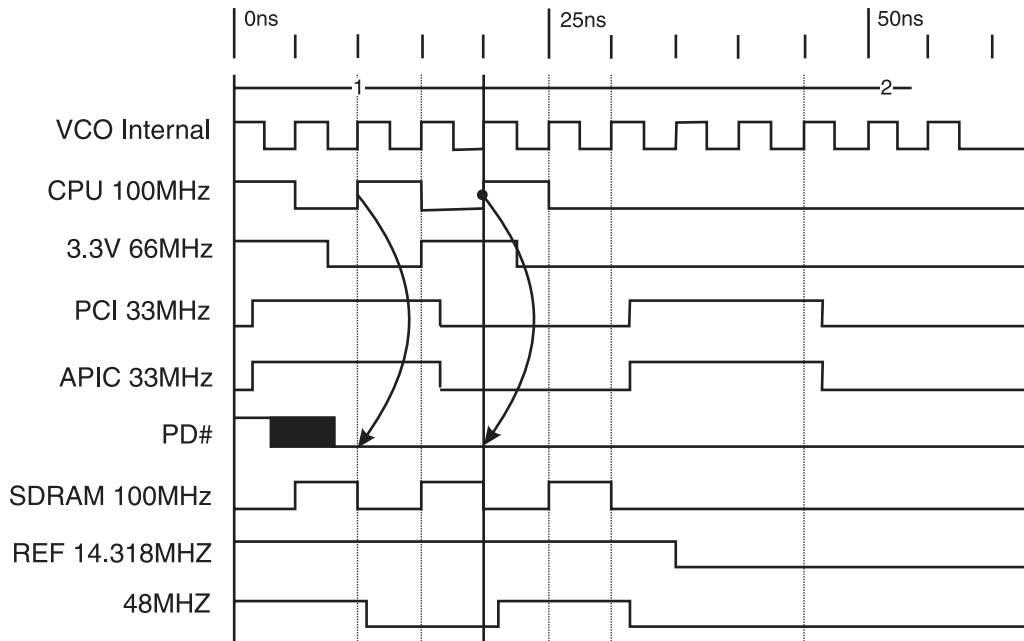


Fig. 1

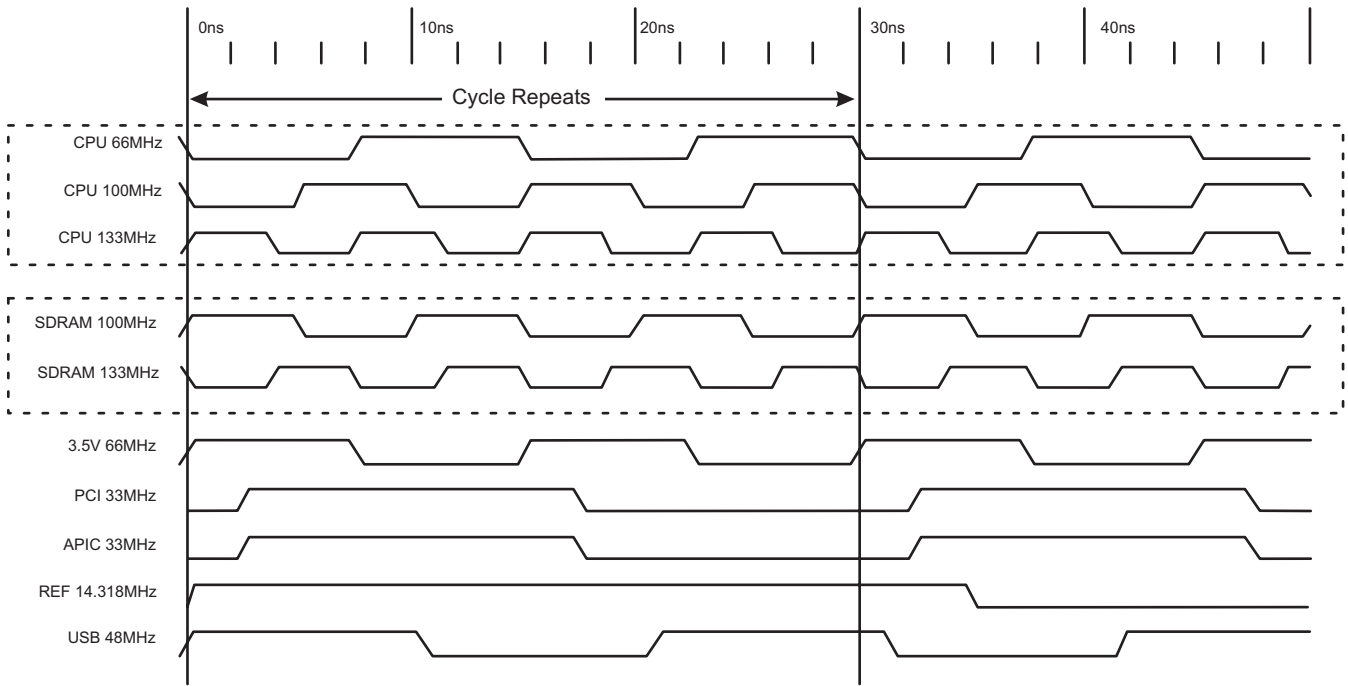


Power Down Waveform

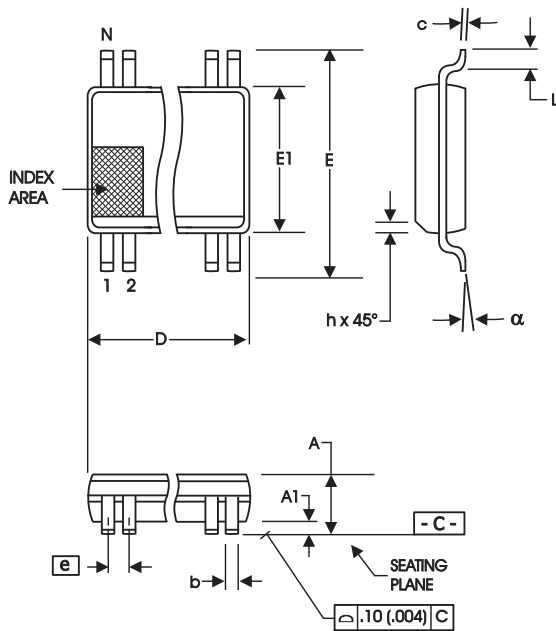


Note

1. After PD# is sampled active (Low) for 2 consecutive rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low transition.
2. Power-up latency <3ms.
3. Waveform shown for 100MHz



Group Offset Waveforms



300 mil SSOP Package

| SYMBOL | In Millimeters | | In Inches | |
|----------|----------------|-------|----------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 56 | 18.31 | 18.55 | .720 | .730 |

Reference Doc.: JEDEC Publication 95, MO-118

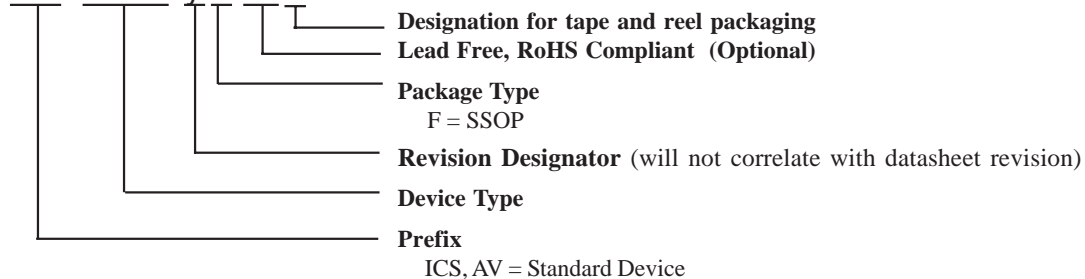
10-0034

Ordering Information

ICS94201yFLFT

Example:

ICS XXXX y FLFT





Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|-------------------------------|--------|
| B | 11/28/2005 | Added LF Ordering Information | 18 |
| | | | |
| | | | |
| | | | |

[Home](#) > [Products](#) > [Timing Solutions](#) > [PC-Notebook-Server Clocks](#) > [Clock Synthesizer by Chipset Vendor](#) > [Desktop Chipsets](#) > 94201

[Add to myIDT \[?\]](#)

You may also like...

94201 (Desktop Chipsets)

Description

810/810E and Solano (815) type chipset

Market Group

PC CLOCK

Additional Info

The ICS94201 belongs to ICS new generation of programmable system clock generators. It employs serial programming I2C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking. • 2 - CPUs @ 2.5V • 13 - SDRAM @ 3.3V • 3 - 3V66 @ 3.3V • 8 - PCI @3.3V • 1 - 24/48MHz@ 3.3V • 1 - 48MHz @ 3.3V fixed • 1 - REF @3.3V, 14.318MHz



Related Orderable Parts

| Attributes | 94201DF | 94201DFLF | 94201DFLFT | 94201DFT |
|--------------------------------|--------------|---------------|---------------|--------------|
| Voltage | 3.3 V (PV56) | 3.3 V (PVG56) | 3.3 V (PVG56) | 3.3 V (PV56) |
| Package | SSOP 56 | SSOP 56 | SSOP 56 | SSOP 56 |
| Speed | NA | NA | NA | NA |
| Temperature | C | C | C | C |
| Status | Active | Active | Active | Active |
| Sample | Yes | Yes | No | No |
| Minimum Order Quantity | 78 | 78 | 1000 | 1000 |
| Factory Order Increment | 26 | 26 | 1000 | 1000 |

Related Documents

| Type | Title | Size | Revision Date |
|-----------|-----------------|--------|---------------|
| Datasheet | 94201 Datasheet | 191 KB | 11/08/2006 |

