Am2925

Clock Generator and Microcycle Length Controller

DISTINCTIVE CHARACTERISTICS

- **Crystal controlled oscillator**
  Stable operation from 1MHz to over 31MHz
- **Four microcode controlled clock outputs**
  Allows clock cycle length control for 15–30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length
- **System controls for $\overline{\text{Run}}/\overline{\text{Halt}}$ and Single Step**
  Switch debounced inputs provide flexible halt controls
- **Slim 0.3" 24-pin package**
  LSI complexity in minimum board area

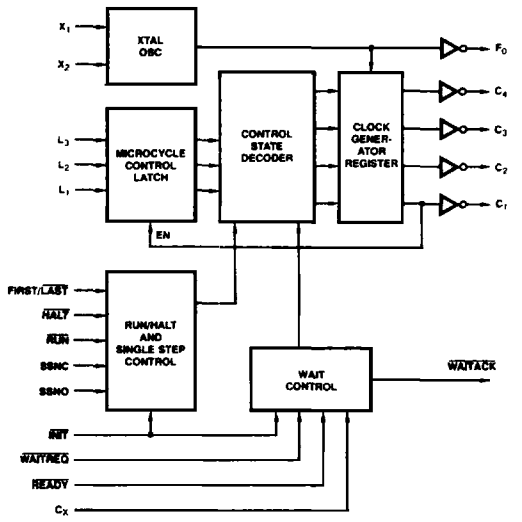
GENERAL DESCRIPTION

The Am2925 is a single-chip general purpose clock generator/driver. It is crystal controlled, and has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meet a variety of system speed requirements. The Am2925 generates four different simultaneous clock output waveforms tailored to meet the needs of Am2900 and other bipolar and MOS microprocessor based systems. One-of-eight cycle lengths may be generated under microprogram control using the Cycle Length inputs L_1, L_2, and L_3.

The Am2925 oscillator runs at frequencies to over 31MHz. A buffered oscillator output, F_0, is provided for external system timing in addition to the four microcode controlled clock outputs C_1, C_2, C_3 and C_4.

System control functions include Run, Halt, Single-Step, Initialize and Ready/Wait controls. In addition, the FIRST/$\overline{\text{LAST}}$ input determines where a halt occurs and the C_X input determines the end point timing of wait cycles. $\overline{\text{WAITACK}}$ indicates that the Am2925 is in a wait state.

BLOCK DIAGRAM



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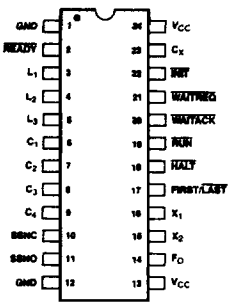
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-24-Slim



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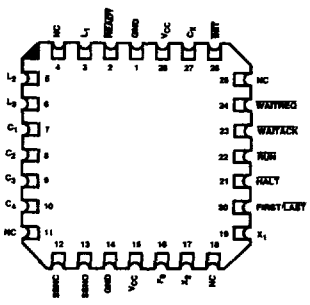
L-28-1



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Note: Pin 1 is marked for orientation

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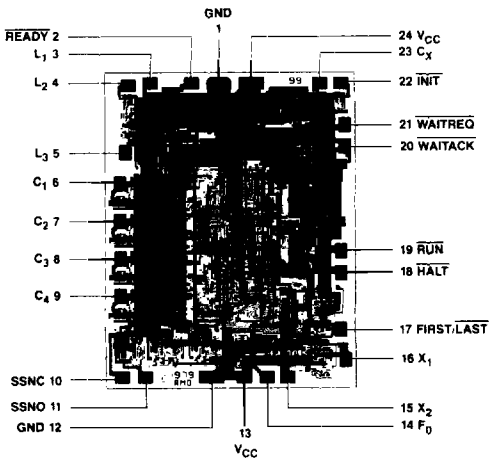
METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.097" x .122"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2925 **D** **C** **B**

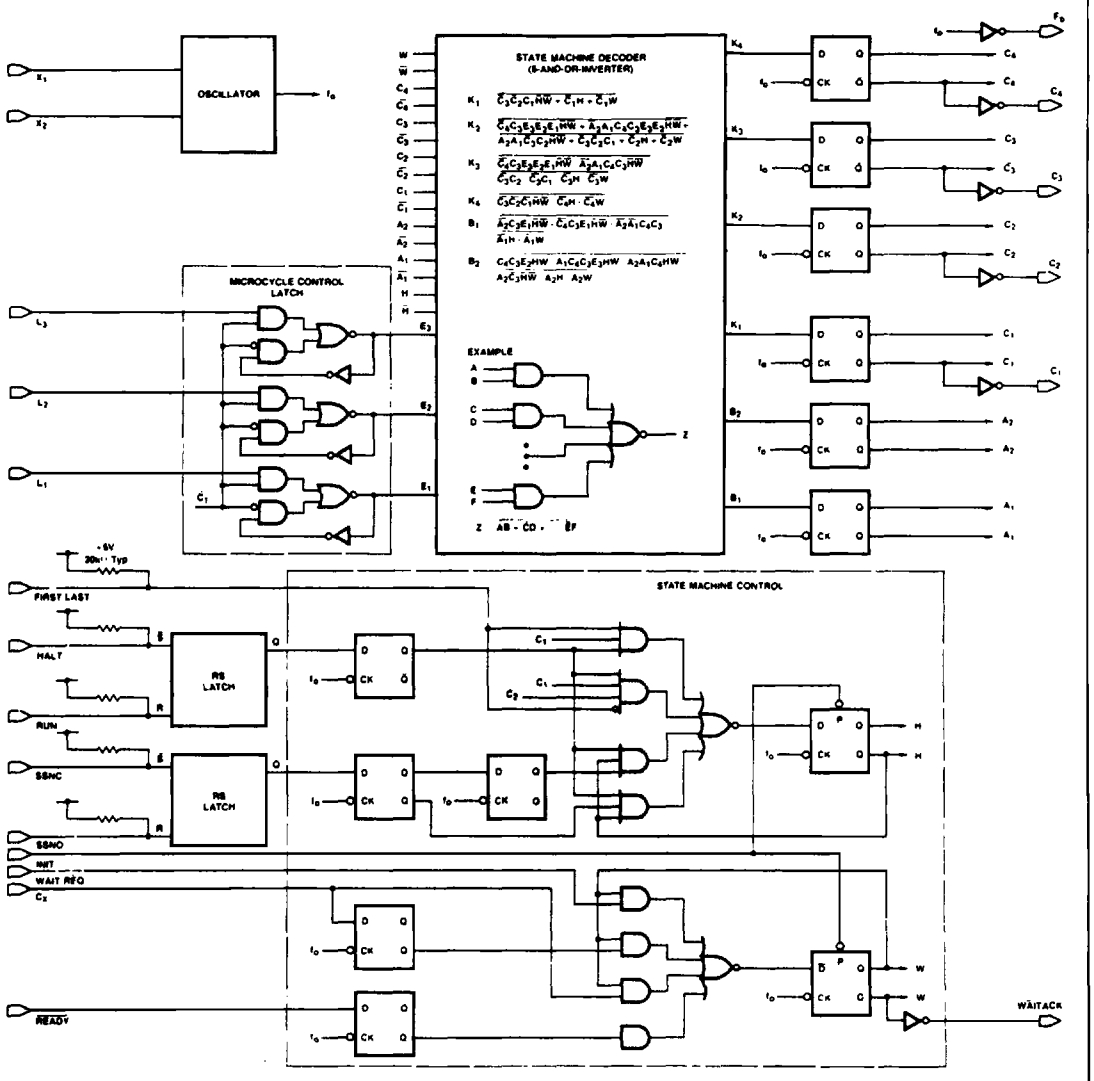
- **B** — Screening Option: Blank – Standard processing; B – Burn-in
- **C** — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- **D** — Package: D – 24-pin SLIMDIP; L – 28-pin leadless chip carrier; X – Dice
- **Am2925** — Device type: Clock Generator

Valid Combinations	
Am2925	DC, DCB, DMB LC, LCB, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

LOGIC DIAGRAM



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PIN DESCRIPTION

Pin No.	Name	I/O	Description
6, 7, 8, 9	C_1, C_2 C_3, C_4	O	System clock outputs. These outputs are all active during every system clock cycle. Their timing is determined by clock cycle length controls, L_1, L_2, and L_3.
3, 4, 5	L_1, L_2, L_3	I	Clock cycle length control inputs. These inputs receive the microcode bits that select the microcycle lengths. They form a control word which selects one of the eight microcycle waveform patterns F_3 through F_{10}.
14	F_0	O	The buffered oscillator output. F_0 internally generates all of the timing edges for outputs C_1, C_2, C_3, C_4 and $\overline{WAITACK}$. F_0 rises just prior to all of the C_1, C_2, C_3, C_4 transitions.
18, 19	$\overline{HALT}$ and $\overline{RUN}$	I	Debounced inputs to provide $\overline{HALT}$ control. These inputs determine whether the output clocks run or not. A LOW input on $\overline{HALT}$ ($\overline{RUN}$ = HIGH) will stop all clock outputs.
17	FIRST/$\overline{LAST}$	I	$\overline{HALT}$ time control input. A HIGH input in conjunction with a $\overline{HALT}$ command will cause a halt to occur when C_4 = LOW and C_1 = C_2 = C_3 = HIGH (see clock waveforms). A LOW input causes a $\overline{HALT}$ to occur when C_1 = C_2 = C_3 = LOW and C_4 = HIGH.
11, 10	SSNO and SSNC	I	Single Step control inputs. These debounced inputs allow system clock cycle single stepping while $\overline{HALT}$ is activated LOW.
21	$\overline{WAITREQ}$	I	The Wait Request active LOW input. When LOW this input will cause the outputs to halt during the next oscillator cycle after the C_X input goes LOW.
23	C_X	I	Wait cycle control input. The clock outputs respond to a wait request one oscillator clock cycle after C_X goes LOW. C_X is normally tied to any one of C_1, C_2, C_3 or C_4.
20	$\overline{WAITACK}$	O	The Wait Acknowledge active LOW output. When LOW, this output indicates that all clock outputs are in the "WAIT" state.
2	$\overline{READY}$	I	The $\overline{READY}$ active LOW input is used to continue normal clock output patterns after a wait stage.
22	$\overline{INIT}$	I	The Initialize active LOW input. This input is intended for use during power up initialization of the system. When LOW all clock outputs free run regardless of the state of the Halt, Single Step, Wait Request and Ready inputs.
16, 15	X_1, X_2	I, O	External crystal connections. X_1 can also be driven by a TTL frequency source.

DETAILED DESCRIPTION

The Am2925 is a dynamically programmable general-purpose clock generator/driver. It can be logically separated into three parts. There is an oscillator, a state machine decoder and a state machine control section.

The oscillator is a linear inverting amplifier which may be configured with a minimum of external parts as a 1st harmonic* crystal oscillator, 3rd harmonic* crystal oscillator, L-C oscillator or used to buffer an external clock. The buffered, inverted output of this oscillator is available as F_0.

The state machine takes microcode information from the Microcycle Length "L" inputs L_1, L_2 and L_3 and counts the fundamental frequency of the internal oscillator, F_0, to create the clock outputs, C_1, C_2, C_3 and C_4.

The clock outputs have a characteristic wave shape relationship for each microcycle length. For example, C_1 is always LOW only on the last F_0 clock period of a microcycle and C_4 is always LOW on the first. C_3 has an approximately 50% duty cycle, and C_2 is HIGH for all but the last two periods.

The current state of the machine is contained in a register, part of which is the Clock Generator Register. C_1, C_2, C_3 and C_4 are the outputs of this register. These outputs and the outputs of the Microcycle Control Latch are fed into a set of combinatorial logic to generate the next state. On each falling edge of the internal clock the next state is entered into the current state register. The Microcycle Control Latch is latched when C_1 is HIGH. This means that it will be loaded during the last state of each microcycle (C_1 = C_2 = C_3 = LOW, C_4 = HIGH). This internal latch selects one of eight possible microcycle lengths, F_3 to F_{10}.

The state machine control logic, which determines the mode of operation of the state machine, is intended to be connected to a front panel. There are four basic modes of operation of the Am2925 comprised of Run, Halt, Wait and Single Step.

SYSTEM TIMING

In the typical computer, the time required to execute different instructions varies. However, the time allotted to each instruction is the time that it takes to execute the longest instruction. The Am2925 allows the user to dynamically vary the time allotted for each instruction, thereby allowing the user to realize a higher throughput.

This application section will cover several aspects of the Am2925. The first topic to be covered is the oscillator section which is responsible for providing the basis of all system timing. Second will be how to operate the Am2925; last will be an example of an Am2925 in a 16-bit microprogrammed machine.

*It is understood that the terms "fundamental mode" and "3rd overtone" are generally regarded as more technically correct, but "1st harmonic" and "3rd harmonic" are used here because of their more generally accepted usage.

OSCILLATOR

The Am2925 contains an inverting, linear amplifier which is intended to form the basis of a crystal oscillator. In designing this oscillator it is necessary to consider several factors related to the application.

The first consideration is the desired frequency accuracy. This may be subdivided into several areas. An oscillator is considered stable if it is insensitive to variations in temperature and supply voltage, and if it is unaffected by individual component changes and aging. The design of the Am2925 is such that the degree to which these goals are met is determined primarily by the choice of external components. Various types of crystals are available and the manufacturers' literature should be consulted to determine the appropriate type. For good temperature stability, zero temperature coefficient capacitors should be used (Type NPO). For extreme temperature stability, an oven must be used or some other form of temperature compensation applied.

Absolute frequency accuracy must also be considered. The resonant frequency varies with load capacitance. It is therefore important to match the load specified by the crystal manufacturer for a standard crystal (usually 32pF), or to specify the load when ordering a special crystal. It should then be possible to determine from the crystal characteristics the load tolerance to maintain a given accuracy. If the "set-on" error due to load tolerance is unacceptable, a trimmer capacitor should be incorporated for fine adjustment.

The mechanism by which a crystal resonates is electromechanical. This resonance occurs at a fundamental frequency (1st harmonic) and at all odd harmonics of this frequency (even harmonic resonance is not mechanically possible). Unless otherwise constrained crystal oscillators operate at their fundamental frequency. However, crystals are not generally available with fundamental frequencies above 20-25MHz. At higher frequencies, an overtone oscillator must be used. In this case, the crystal is designed to oscillate efficiently at one of its odd harmonic frequencies and additional components are included in the oscillator circuit to prevent it oscillating at lower harmonics.

Where a high degree of accuracy or stability is not required, the amplifier may be configured as an L-C oscillator. It may also be driven from an external clock source if operation is required in synchronism with that source.

1st Harmonic (Fundamental) Oscillator

The circuit of a typical 1st harmonic oscillator is shown in Figure 1. The crystal load is comprised of the two 68pF capacitors in series. This 34pF approximates the standard 32pF crystal load. If a closer match is required then one of the capacitors should be replaced with a parallel combination of a fixed capacitor and a trimmer. The nominal value of the combination should be 60pF to provide proper crystal loading.

A typical crystal specification for use in this circuit is:

Frequency Range: 5–20MHz
Resonance: Parallel Mode
Load: 32pF
Stability: .01% or to match systems requirements
Case: H-17—for smaller size
Temp Range: −30 to +70°C
Note: Frequency will change over temp

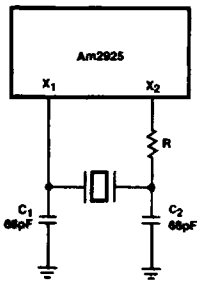

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Figure 1. Connections for 5–20 MHz.

It is good practice to ground the case of the crystal to eliminate stray pick-up and keep all connections as short as possible.

Note: At fundamental frequencies below 5MHz it is possible for the oscillator to operate at the 3rd harmonic. To prevent this a resistor should be added in series with the X_2 pin as shown in the circuit diagram.

The resistor value should match the impedance of C_2:

$$R = X_{C_2} = \frac{1}{2\pi f C_2}$$

3rd Harmonic Oscillator

At frequencies greater than 20MHz the crystal can be operated at its 3rd harmonic. A typical circuit is shown in Figure 2. Two additional components are included; an inductor, L_1, and a capacitor, C_3. The purpose of the capacitor is to block the d.c. path through the inductor and thereby maintain the correct amplifier bias. C_3 should be large ($\geq$ 1000pF).

The inductor forms a parallel tuned circuit with C_1. This circuit has its resonance set between the 1st and 3rd harmonics of the crystal and is used to prevent the oscillator operating at the 1st harmonic. In the 1st harmonic oscillator (Figure 1), the crystal appears as an inductor and forms a π-network with the two capacitors, thus providing the necessary phase shift for oscillation. In the 3rd harmonic oscillator, L_1 and C_1 are chosen such that at the 3rd harmonic the impedance of circuit is equivalent to that of the capacitor C_2 in the 1st harmonic oscillator (Figure 3b). Thus, the same π-network is formed (Figure 3c) and oscillation is possible. At the 1st harmonic the tuned circuit appears as an inductor (Figure 3a), the π-network is not formed and oscillation is not possible.

The following specification is typical for a crystal to be used in a 3rd harmonic oscillator.

Frequency Range: Above 20MHz
Resonance: Parallel Mode
Load: 32pF
Stability: .01% or to match systems requirements
Case: H-17 — for smaller size
Temp Range: −30 to +70°C
Note: Frequency will change temp

Again it is good practice to ground the crystal case and keep connections short.

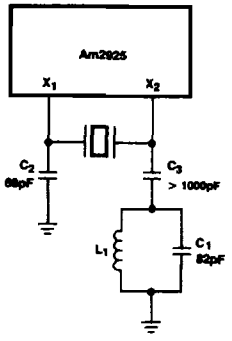

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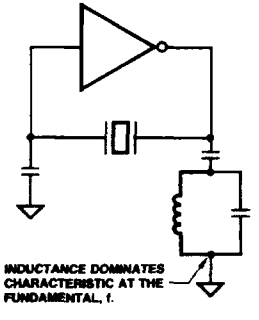
Figure 2. Connections for Frequencies above 20MHz.



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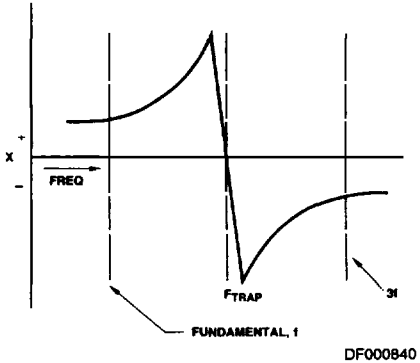
a) Fundamental Equivalent



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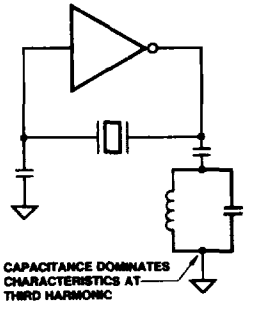
b) Trap Impedance



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c) 3rd Harmonic Equivalent

Figure 3. Forcing Third Harmonic Oscillation.

Design Procedure

(1) Assume C_1 = 82pF and C_2 = 68pF (this gives a sensible inductor value). L_1 is calculated according to the formula:

$$L_1 = \frac{1151}{f_o^2} \qquad f_o = \text{Operating frefquency in MHz}, \; L_1 \text{ in } \mu H$$

This sets the resonant frequency of the L-C combination at 0.52 f_o.

(2) Select the closest standard value inductor for L_1. Using this value calculate C_1 such that the resulting crystal load at the 3rd harmonic is 32pF.

$$C_1 = 60 + \frac{25330}{L_1 \cdot f_o^2} \qquad C_1 \text{ in pF.}$$

Choose the closest standard capacitor value to this.

Using standard values both the resonant frequency of the L-C circuit (f_r) and the crystal load are non-optimal. This will cause a slight error in the oscillating frequency. If this is not permissible C_1 may be a fixed capacitor in parallel with a trimmer such that the range of adjustment includes the calculated value for C_1. This is then set to give the desired frequency. In either case the approximate inductor value will cause the resonant frequency to the L-C circuit to change. This frequency, f_r, may be computed and should remain approximately midway between the 1st and 3rd harmonic.

$$f_r = \frac{159}{\sqrt{L_1 C_1}} \qquad f_r \text{ in MHZ}, \; L_1 \text{ in } \mu H, \; C_1 \text{ in pF}$$

L-C Oscillator

The Am2925 can be operated as an L-C tuned oscillator (Figure 4) and will perform as a stable oscillator within the restrictions of the chosen frequency determining components (i.e., inductor and capacitors). The circuit chosen is a classical π-network with DC loop isolation. The Am2925 oscillator is a DC biased linear amplifier. This DC bias is necessary and therefore C_3 is included to block the DC path through the inductor. If a variable slug tuned inductor is used a moderate range of frequency adjustment tuneability (approximately 2:1) can be achieved. The range can be enhanced by switching the two resonant capacitors (C_1, C_2) to larger or smaller values. The specific frequency of operation can be determined by the formula:

$$f = \frac{1}{2\pi\sqrt{LC}} \quad \text{(where C is } C_1 \text{ and } C_2 \text{ in series).}$$

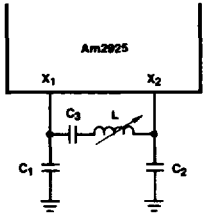

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Figure 4. L-C Tuned Oscillator.

External Clock Drive

The Am2925 can be driven from an external clock source at a signal level of 1.0V P-P or greater. This is accomplished by reducing the gain of the amplifier and AC coupling the input signal (Figure 5). The gain is reduced by feeding the amplifier output back to the input through a 4.7kΩ resistor. AC coupling is provided by a 0.01μF capacitor. The controlled gain minimizes ringing caused by the fast rising edges of the driver. The AC coupling maintains oscillator output symmetry by preserving oscillator DC bias levels.

X_1 can be driven directly by TTL levels meeting the DC input requirements.

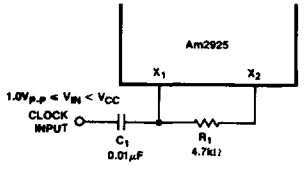

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Figure 5. External Clock Drive.

Am2925 Control Inputs

The control inputs fall into two categories, microcycle length control and clock control. Microcycle length control is provided via the "L" inputs which are intended to be connected to the microprogram memory. The "L" inputs are used to select one of eight cycle lengths ranging from three oscillator cycles for pattern F_3 to ten oscillator cycles for pattern F_{10}. This information is always loaded at the end of the microcycle into the Microcycle Control Latch. The Microcycle Latch performs the function of a pipeline register for the microcycle length microcode bits. Therefore, the cycle length goes in the same microword as the instruction that it is associated with.

The clock control inputs are used to synchronize the microprogram machine with the external world and I/O devices. Inputs like $\overline{\text{RUN}}$, $\overline{\text{HALT}}$, SSNO and SSNC, which start and stop execution, are meant to be connected to switches on the front panel of the microprogrammed machine (see Figure 6). These inputs have internal pull-up resistors and are connected to an R-S flip-flop in order to provide switch debouncing. The FIRST/$\overline{\text{LAST}}$ input is used to determine at what point of the microcycle the Am2925 will halt when $\overline{\text{HALT}}$ or a SINGLE STEP is initiated. In most applications the user wires this input HIGH or LOW depending on his design.

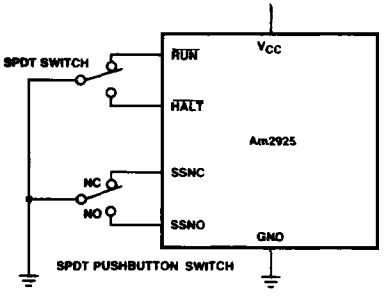

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Figure 6. Switch Connection for $\overline{\text{RUN}}$/$\overline{\text{HALT}}$ and Single Step.

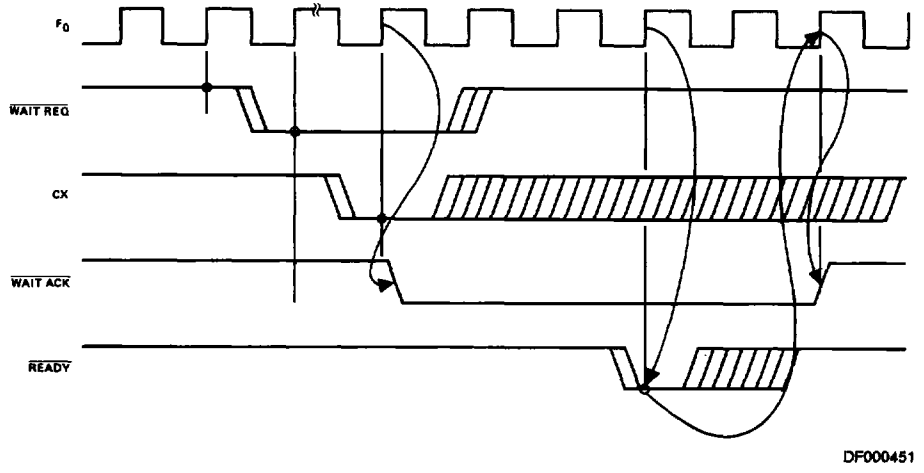


Figure 7. Am2925 WAIT/READY Timing.

When HALT is held low (RUN = HIGH) the state machine will start the halt mode on the last (C_1 = LOW) or the first (C_4 = LOW) state of the microcycle as determined by the FIRST/LAST input. When RUN goes low (HALT = HIGH) the state machine will resume the run mode.

The WAITREQ, C_X, READY and WAITACK signals are used to synchronize other parts of a computer system (memory, I/O devices) to the CPU by dynamically stretching the microcycle. For example, the CPU may access a slow peripheral that requires the data remain on the data bus for several microseconds in which case the peripheral pulls the WAITREQ line LOW. The C_X input lets the designer specify when the WAITREQ line is sampled in the microcycle. This has a direct impact on how much time the peripheral has to respond in order to request a wait cycle (see Figure 7). The READY line is used by the peripheral to signal when it is ready to resume execution of the rest of the microcycle. The WAITACK line goes LOW on the next oscillator cycle after the C_X input goes LOW and remains LOW until the second oscillator cycle after READY goes LOW.

The SSNO and SSNC inputs are used to initiate the SINGLE STEP mode. These debounced inputs allow a single microcycle to occur while in the halt mode. SSNO (normally open) and SSNC (normally closed) are intended to be connected to a momentary SPDT switch. After SSNO has been low for one clock edge, the state machine will change to the run mode. The microcycle will end on the first or last state of the microcycle depending on the state of the FIRST/LAST.

AC Timing Signal References

Set-up and hold times in registers and latches are measured relative to the clock signals that drive them. In the Am2925, the crystal oscillator provides a free running clock signal that drives all the registers on the devices. This clock is provided for the user through the buffered output of F_0. Therefore, F_0 is used as the reference for set-up, hold and clock to output times. However for the Microcontrol Latch, the set-up and hold times are referenced to the C_1 output which is the buffered version of the latch enable. This reference is appropriate for the Microcontrol Latch because in a typical application this latch is considered part of the pipeline register which is also driven by one of the "C" outputs.

Clock Outputs

There are four clock outputs provided for the user which have different duty cycles. The user must make a decision as to which one best fits his purposes. For example, in a three address architecture, with the Am2903 (Figure 8), the C_3 clock (approximately 50% duty cycle) could be used to drive the clock input while C_2 (always low last two oscillator cycles) drives Instruction Enable. This guarantees, for microcycle lengths greater than four, that the internal RAM data latches of the Am2903 are closed and the destination address is multiplexed onto the B address bus before the RAM begins the Write cycle (Figure 9).

16-BIT MACHINE WITH Am2925

The block diagram in Figure 10 shows a 16-bit microprogrammed machine which uses an Am2925 to generate system timing. The design decisions include oscillator frequency and clock pattern selections.

Selecting the Crystal

In order to pick the oscillator frequency, a detailed timing analysis of the machine must be done in order to determine the execution length of every operation to be performed. For each operation there will be several delay paths, which usually include the ALU and the microprogram control.

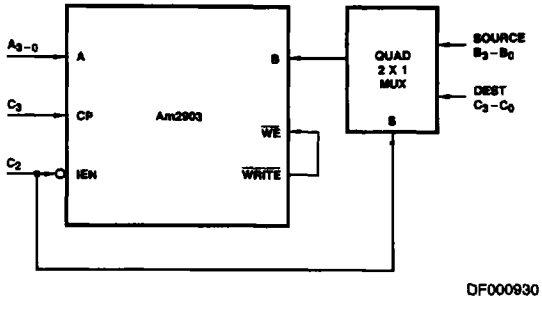


Figure 8. Am2903 Three Address Architecture.

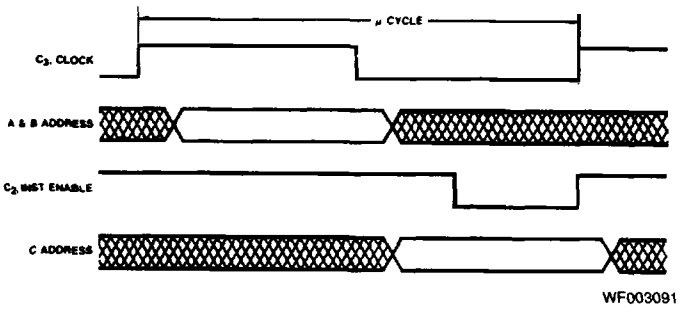


Figure 9. Am2903 Three Address Operation.

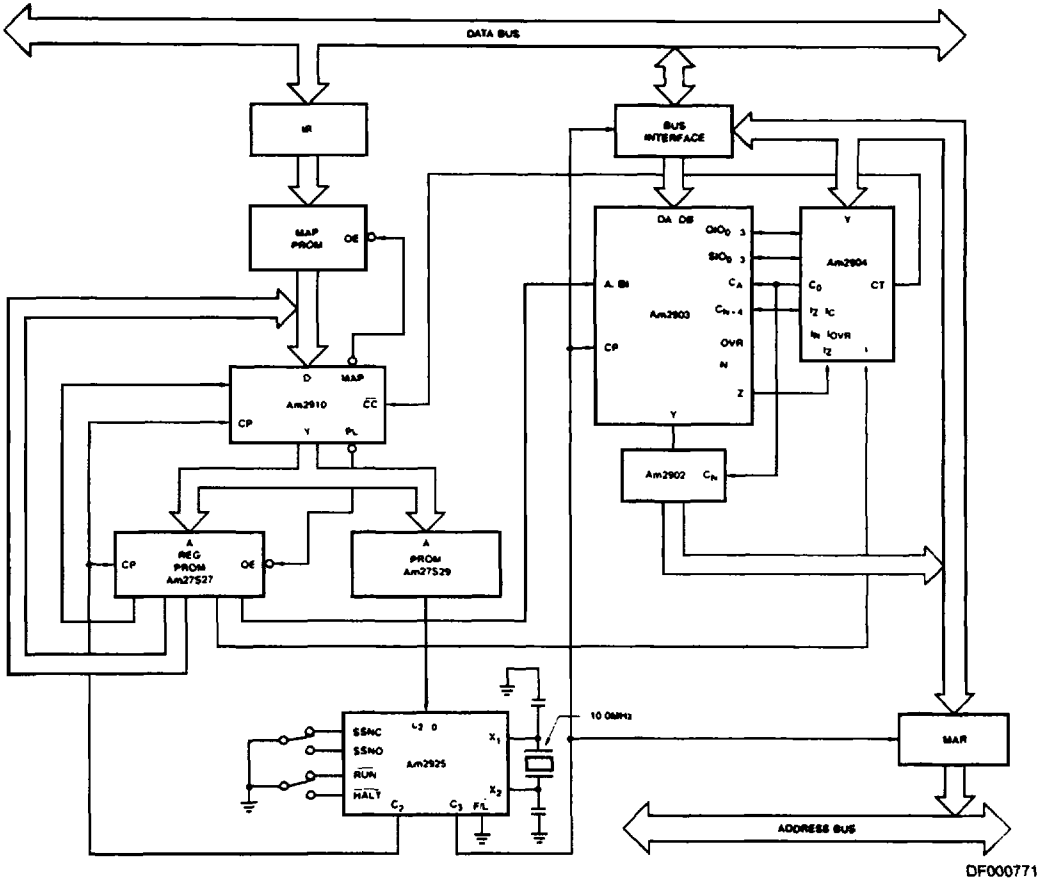


Figure 10. 16-Bit Microprogrammed Machine.

Table 1 is an example of two of these paths. PATH 1 is a path through the Am2910 (Figure 10) for a microprogram Conditional Jump Subroutine. PATH 2 is a data flow path through the Am2903 for an Add instruction. Therefore, if the operation were an Add with a Conditional Jump Subroutine the maximum delay would be 170ns. If there were a Program Control Unit also, then delays through it would have to be considered.

After the execution times all of the instruction types have been calculated, the oscillator frequency can be selected. It is desirable to minimize the difference between the most commonly used instructions and multiples of the oscillator period. In this way the most efficient use can be made of the variable microcycle scheme.

For example, in the hypothetical machine in Figure 10 there are five instruction types (most machines will have more). Table 2 is a table which lists each instruction type, corresponding execution time, and anticipated percentage of the typical instruction stream for each instruction. Several possible frequencies are shown which contain the next highest multiple of the corresponding oscillator period for each instruction. 20MHz is the best choice because it comes closest to matching instructions A and C which compose 90% of the typical instruction stream.

In this example, 20MHz was chosen. AT 20MHz there is a choice between fundamental or overtone crystals. Fundamental frequency crystals are commonly available up to 25MHz and 3rd harmonic crystals are available above 17MHz. A fundamental crystal was selected for the example machine because the component count for the oscillator design is lower than for the overtone design. However, if it had turned out that 30MHz was a better choice then overtone operation would be chosen since fundamental crystals above 25MHz are not generally available.

Fixed Bandwidth Buses

For those designs that require a data bus with fixed bandwidth and fixed time slots for each memory access, the designer should consider using cycle lengths which are a multiple of the shortest cycle length, i.e., cycle lengths 3, 6 and 9 or cycle lengths 4 and 8.

The design could further require that the bus be accessed only during the shortest cycle length. Therefore, by using multiple cycle lengths it can be predicted when the CPU will access the bus and for how long, thereby maintaining the fixed bandwidth.

Performance Comparison

Estimated performance can be calculated directly from Table 2. For a fixed microcycle machine the longest instruction execution time would have to be used for all instructions, yielding an average instruction time of 228ns. With a variable microcycle machine the average instruction time is the sum of the products for each instruction, of the percentage of the instruction stream and the next highest multiple. The average instruction for the example machine with a 20MHz crystal is:

(0.6 x 150 + .08 x 200 + .3 + 200 +
.01 x 200 + .01 + 250) = 170.5ns

This represents a 25% increase in system performance without requiring any other system speed-ups and without requiring faster devices.

Device No.	Device Path	Path 1	Path 2
Am27S27	CP – Q	27	27
Am2904	INST – CT	58	–
Am2903A	I/AB – GP	–	50
Am2910A	CC – Y	30	–
Am2902A	GP – CN + Z	–	7
Am27S27	TS	55	–
Am2903A	CN – Z	–	35
Am2904	TSZ	–	17
Total	ns	170	136

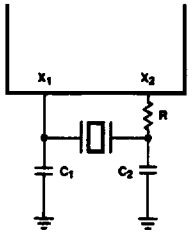
Table 1: Delay Path Totals for an Add and a Condition Jump Subroutine.

Instruction Type	A	B	C	D	E	Unit
Execution Time	143	180	184	200	228	ns
Percentage of Instruction Stream	60%	8%	30%	1%	1%	%
Closest Multiple Oscillator Period						
20MHz P = 50	150 (3P)	200 (4P)	200 (4P)	200 (4P)	250 (5P)	ns
25MHz P = 40	160 (4P)	200 (5P)	200 (5P)	200 (5P)	240 (6P)	ns
30MHz P = 33	167 (5P)	200 (6P)	200 (6P)	200 (6P)	233 (7P)	ns
33MHz P = 30	150 (5P)	180 (6P)	210 (7P)	210 (7P)	240 (8P)	ns

Table 2. Instruction Time Analysis.

Am2925 OSCILLATOR APPLICATIONS

EXTERNAL COMPONENT CALCULATIONS SUMMARY



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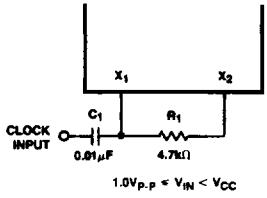
$$R = X_{C_2} = \frac{1}{Tfc_2} \text{ for } 1-6\text{MHz}$$

$R = 0$ for 6 – 20MHz

FUNDAMENTAL OSCILLATOR



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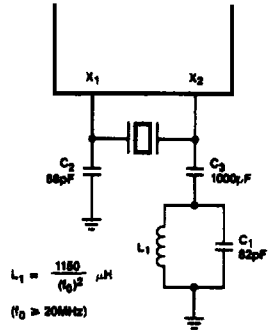
EXTERNAL CLOCK DRIVE



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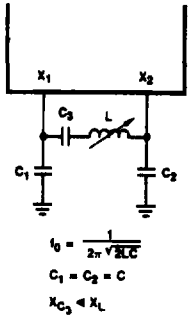
3rd HARMONIC OSCILLATOR



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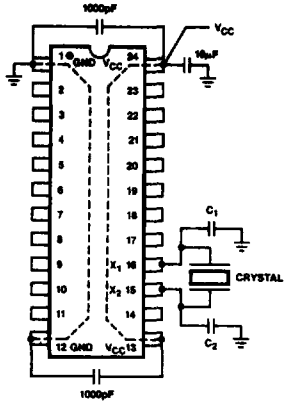
L-C OSCILLATOR

TYPICAL EXTERNAL CONNECTIONS



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DESIGN CONSIDERATIONS

1. Oscillator external connections should be less than 1" long — wirewrap is not recommended.
2. V_{CC} and GND connections should be less than ½" long to power plane.
3. Supply decoupling includes both high frequency and bulk storage elements.
4. The same considerations apply for 3rd overtone configurations.

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Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.0mA	2.5			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	$\overline{WAITACK}$, C_i	I_{OL} = 4.0mA			0.4	Volts
				I_{OL} = 8.0mA			0.45	
				I_{OL} = 12mA			0.5	
			F_0	I_{OL} = 16mA			0.5	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Note 3)	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3			−0.4	mA
				$\overline{WAITREQ}$, X_1 (See Figure 11)			−0.8	mA
				SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$			−1.0	mA
				C_X			−1.2	mA
				FIRST/$\overline{LAST}$			−1.5	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3			20	μA
				$\overline{WAITREQ}$			50	μA
				SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$			−500	μA
				C_X			70	μA
				FIRST/$\overline{LAST}$			−750	μA
				X_1 (See Figure 11)			500	μA
I_I	Input HIGH Current	V_{CC} = MAX	V_{IN} = 5.5V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3			100	μA
			V_{IN} = V_{CC}	SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$			100	μA
			V_{IN} = 5.5V	$\overline{WAITREQ}$, C_X			1.0	mA
			V_{IN} = V_{CC}	FIRST/$\overline{LAST}$			1.0	mA
			V_{IN} = 4.0V	X_1 (See Figure 11)			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX				85	120	mA

Notes: 1. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX use the appropriate value specified under Operating Ranges for the applicable device type.
3. Does not apply to X_1 and X_2.
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} varies with temperature and oscillation frequency as shown in Figure 12. The parameters specified (worst case) applies to f_0 = 0, +25°C, C_1 = C_2 = C_3 = LOW, C_4 = HIGH, X_1 = 2.4V, X_2 = open and F_0 = LOW. The variations shown in Figure 12 apply to typical values.

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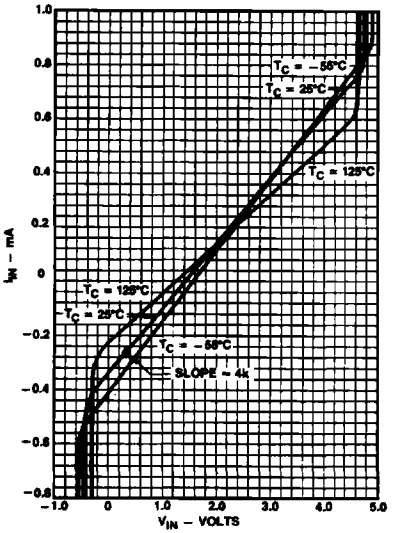
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

	Parameters	Description	Test Conditions	Min	Typ	Max	Units
1	f_{MAX1}	F_0 Frequency (C_X Connected) (Note 6)	C_L = 15pF, R_L = 280Ω	31			MHz
2	f_{MAX2}	F_0 Frequency (C_X = HIGH)			42		
3	t_{OFFSET}	F_0(↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)	C_L = 50pF, R_L = 2.0kΩ	0	5.0	7.5	ns
4	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)		3	11.5	16	ns
5	t_{SKEW}	C_1 (↓) to C_2 (↓)		0	0.5	2	ns
6	t_{SKEW}	C_1 (↓) to C_3 (↓)		0	0.5	2	ns
7	t_{SKEW}	C_1 (↓) to C_4 (↓) Opposite Transition		4	7	10	ns
8	t_S	L_1, L_2, L_3 to C_1 (↓)		5			ns
9	t_H	L_1, L_2, L_3 to C_1 (↓)		9			ns
10	t_S	C_X to F_0 (↓) (Note 7)		20	17		ns
11	t_H	C_X to F_0 (↓) (Note 7)		0	−10		ns
12	t_S	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)		20	17		ns
13	t_H	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)		0	−10		ns
14	t_S	$\overline{READY}$ to F_0 (↓) (Note 8)		20	17		ns
15	t_H	$\overline{READY}$ to F_0 (↓) (Note 8)		0	−10		ns
16	t_S	$\overline{RUN}$, $\overline{HALT}$ (↓) to F_0 (↓) (Notes 8, 9)		20	14		ns
17	t_S	SSNC, SSNO to F_0 (↓) (Notes 8, 9)		20	14		ns
18	t_S	FIRST/$\overline{LAST}$ to F_0 (↓) (Note 10)		25	17		ns
19	t_S	$\overline{INIT}$ (↓) to F_0 (↓) (Note 8)		30			ns
20	t_{PWL}	$\overline{INIT}$ LOW Pulse Width		15	10		ns
21	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$			16	23	ns
22	t_{PLH}	Propagation Delay (Note 11) X_1 to F_0	C_L = 15pF, R_L = 280Ω		13	16	ns
23	t_{PHL}				14	17	ns

Notes: 6. The frequency guarantees apply with C_X connected to C_1, C_2, C_3, C_4 or HIGH. The C_X input load must be considered part of the 50pF/2.0kΩ clock output loading
7. These set-up and hold times apply to the F_0 LOW-to-HIGH transition of the period in which C_X goes LOW
8. These inputs are synchronized internally. Failure to meet t_S may cause a $1/F_0$ delay but will not cause incorrect operation.
9. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
10. FIRST/LAST normally wired HIGH or LOW.
11. Reference point of T offset has been moved forward which has increased T offsets.



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X_1 is not a TTL input. It is a crystal connection to an inverting linear oscillator amplifier, and is specified primarily for test convenience.

Figure 11. Am2925 X_1 Input Characteristics (Typical, V_{CC} = 5.0V).

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

	Parameters	Description	Test Conditions	COMMERCIAL Am2925 Min	COMMERCIAL Am2925 Max	MILITARY Am2925 Min	MILITARY Am2925 Max	Units
1	f_{MAX1}	F_0 Frequency (C_X Connected) (Note 6)	C_L = 15pF, R_L = 280Ω	31		31		MHz
2	f_{MAX2}	F_0 Frequency (C_X = HIGH)						
3	t_{OFFSET}	F_0(↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)	C_L = 50pF, R_L = 2.0kΩ		8.5		8.5	ns
4	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)			17.0		18.0	ns
5	t_{SKEW}	C_1 (↓) to C_2 (↓)			2		2	ns
6	t_{SKEW}	C_1 (↓) to C_3 (↓)			2		2	ns
7	t_{SKEW}	C_1 (↓) to C_4 (↓) Opposite Transition			11		11	ns
8	t_S	L_1, L_2, L_3 to C_1 (↓)		6		7		ns
9	t_H	L_1, L_2, L_3 to C_1 (↓)		11		11		ns
10	t_S	C_X to F_0 (↓) (Note 7)		25		25		ns
11	t_H	C_X to F_0 (↓) (Note 7)		0		0		ns
12	t_S	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)		25		25		ns
13	t_H	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)		0		0		ns
14	t_S	$\overline{READY}$ to F_0 (↓) (Note 8)		25		25		ns
15	t_H	$\overline{READY}$ to F_0 (↓) (Note 8)		0		0		ns
16	t_S	$\overline{RUN}$, $\overline{HALT}$ (↓) to F_0 (↓) (Notes 8, 9)		25		25		ns
17	t_S	SSNC, SSNO to F_0 (↓) (Notes 8, 9)		25		25		ns
18	t_S	FIRST/$\overline{LAST}$ to F_0 (↓) (Note 10)		30		35		ns
19	t_S	$\overline{INIT}$ (↓) to F_0 (↓) (Note 8)		33		35		ns
20	t_{PWL}	$\overline{INIT}$ LOW Pulse Width		20		25		ns
21	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$			25		27	ns
22	t_{PLH}	Propagation Delay (Note 11)	C_L = 15pF, R_L = 280Ω		23		26	ns
23	t_{PHL}	X_1 to F_0			21		23	ns

Notes:
6. The frequency guarantees apply with C_X connected to C_1, C_2, C_3, C_4 or HIGH. The C_X input load must be considered part of the 50pF/2.0kΩ clock output loading
7. These set-up and hold times apply to the F_0 LOW-to-HIGH transition of the period in which C_X goes LOW
8. These inputs are synchronized internally. Failure to meet t_S may cause a $1/F_0$ delay but will not cause incorrect operation.
9. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
10. FIRST/LAST normally wired HIGH or LOW.
11. Reference point of T offset has been moved forward which has increased T offsets.

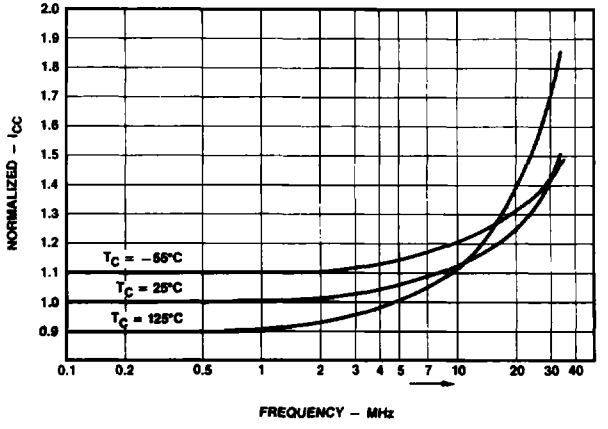

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Figure 12. Am2925 I_{CC} Normalized vs Frequency (V_{CC} = 5.5V).

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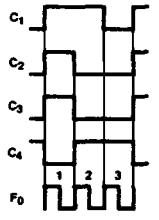
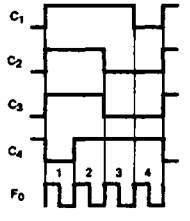
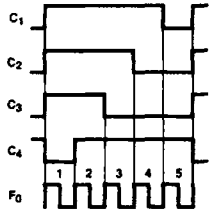
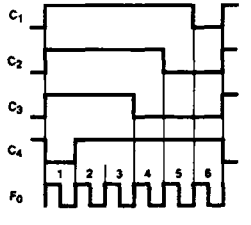
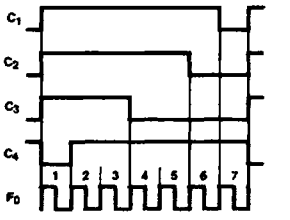
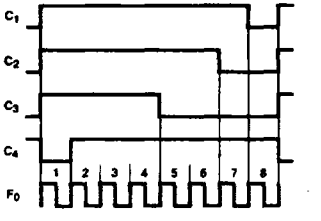
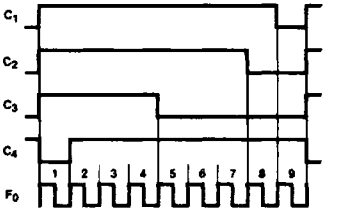
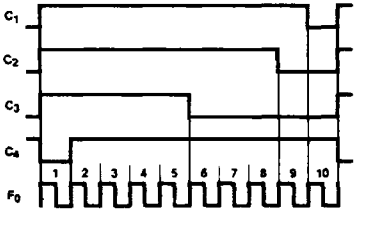
Refer to Page 13-1 for Essential Information on Military Devices

AM2925 CLOCK WAVEFORMS

PATTERN INPUT CODE L_3 L_2 L_1	WAVEFORMS AND TIMING
F_3 LLL	
F_4 LLH	
F_5 HLH	
F_6 HHH	

PATTERN INPUT CODE L_3 L_2 L_1	WAVEFORMS AND TIMING
F_7 LHH	
F_8 LHL	
F_9 HHL	
F_{10} HLL	

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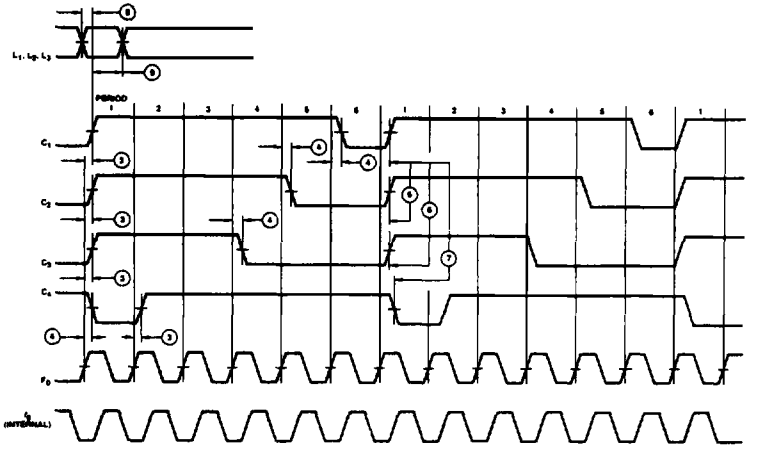
SWITCHING WAVEFORMS



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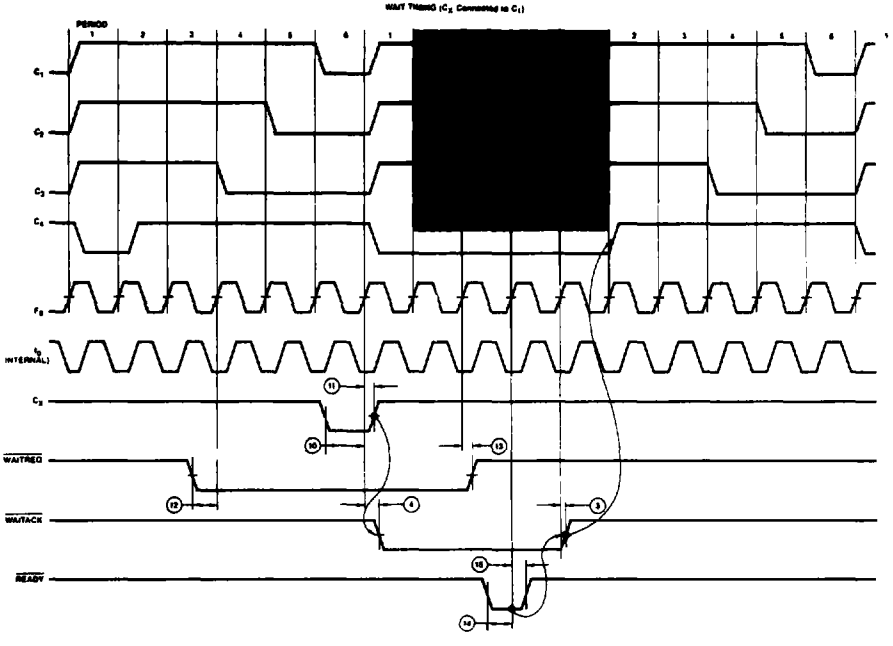
NORMAL CYCLE WITHOUT WAIT STATES (Pattern F_6 Shown)



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WAIT TIMING (C_X Connected to C_1)