54AC/74AC378 • 54ACT/74ACT378

Parallel D Register With Enable

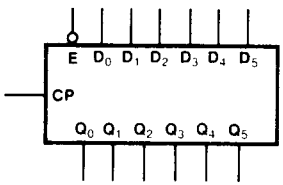
Description

The 'AC/'ACT378 is a 6-bit register with a buffered common Enable. This device is similar to the 'AC/'ACT174, but with common Enable rather than common Master Reset.

- **6-Bit High-Speed Parallel Register**
- **Positive Edge-Triggered D-Type Inputs**
- **Fully Buffered Common Clock and Enable Inputs**
- **Outputs Source/Sink 24 mA**
- **'ACT378 has TTL-Compatible Inputs**

Ordering Code: See Section 6

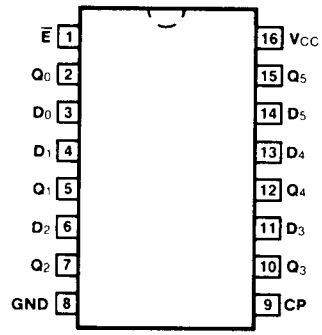
Logic Symbol



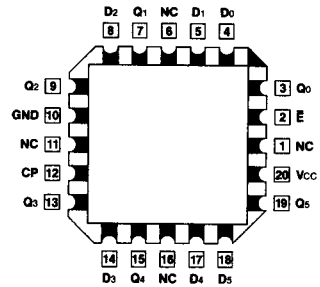
Pin Names

$\overline{E}$	Enable Input
D_0 - D_5	Data Inputs
CP	Clock Pulse Input
Q_0 - Q_5	Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC/'ACT378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

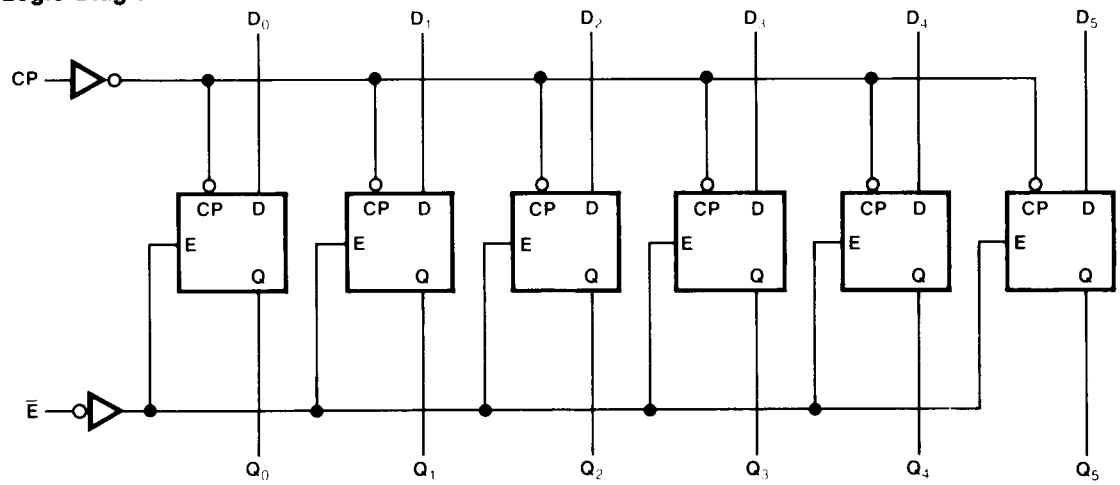
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input.

Truth Table

Inputs			Outputs
$\overline{E}$	CP	D_n	Q_n
H	⌐	X	No Change
L	⌐	H	H
L	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°$
I_{CCT}	Maximum Additional Icc/Input ('ACT378)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		74 100						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0		8.5 6.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0		7.5 5.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF	54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	1.5 1.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	−1.5 −1.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	0 0			ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	8.5 6.0			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		100						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	5.0		6.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	5.0		5.5						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	3.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	5.0	−1.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	5.0	0				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	5.0	6.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V