



MULTIPOINT-LVDS LINE DRIVER AND RECEIVER

FEATURES

- Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates⁽¹⁾ Up to 200 Mbps
- Type-1 Receivers Incorporate 25 mV of Hysteresis
- Type-2 Receivers Provide an Offset (100 mV) Threshold to Detect Open-Circuit and Idle-Bus Conditions
- Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange
- Controlled Driver Output Voltage Transition Times for Improved Signal Quality
- -1 V to 3.4 V Common-Mode Voltage Range Allows Data Transfer With 2 V of Ground Noise
- Bus Pins High Impedance When Disabled or $V_{CC} \leq 1.5$ V
- 100-Mbps Devices Available (SN65MLVD200A, 202A, 204A, 205A)
- M-LVDS Bus Power Up/Down Glitch Free

The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

APPLICATIONS

- Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485
- Backplane or Cabled Multipoint Data and Clock Transmission
- Cellular Base Stations
- Central-Office Switches
- Network Switches and Routers

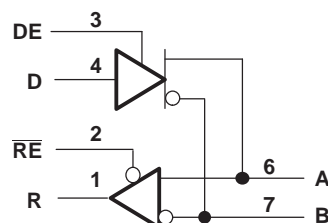
DESCRIPTION

The SN65MLVD201, 203, 206, and 207 are multipoint-low-voltage differential (M-LVDS) line drivers and receivers, which are optimized to operate at signaling rates up to 200 Mbps. All parts comply with the multipoint low-voltage differential signaling (M-LVDS) standard TIA/EIA-899. These circuits are similar to their TIA/EIA-644 standard compliant LVDS counterparts, with added features to address multipoint applications. The driver output has been designed to support multipoint buses presenting loads as low as 30 Ω, and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

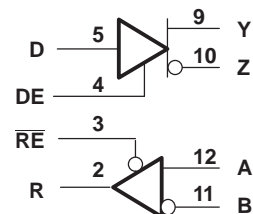
These devices have Type-1 and Type-2 receivers that detect the bus state with as little as 50 mV of differential input voltage over a common-mode voltage range of -1 V to 3.4 V. The Type-1 receivers exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input. Type-2 receivers include an offset threshold to provide a known output state under open-circuit, idle-bus, and other faults conditions. The devices are characterized for operation from -40°C to 85°C.

LOGIC DIAGRAM (POSITIVE LOGIC)

SN65MLVD201, SN65MLVD206



SN65MLVD203, SN65MLVD207



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER ⁽¹⁾	FOOTPRINT	RECEIVER TYPE	PACKAGE MARKING
SN65MLVD201D	SN75176	Type 1	MF201
SM65MLVD203D	SN75ALS180	Type 1	MLVD203
SN65MLVD206D	SN75176	Type 2	MF206
SM65MLVD207D	SN75ALS180	Type 2	MLVD207

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PACKAGE DISSIPATION RATINGS

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING
D(8)	725 mW	5.8 mW/°C	377 mW
D(14)	950 mW	7.6 mW/°C	494 mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE / UNIT	
Supply voltage range ⁽²⁾ , V _{CC}		−0.5 V to 4 V	
Input voltage range	D, DE, RE	−0.5 V to 4 V	
	A, B (201, 206)	−1.8 V to 4 V	
	A, B (203, 207)	−4 V to 6 V	
Output voltage range	R	−0.3 V to 4 V	
	Y, Z, A, or B	−1.8 V to 4 V	
Electrostatic discharge	Human Body Model ⁽³⁾	A, B, Y, and Z	±8 kV
		All pins	±2 kV
	Charged-Device Model ⁽⁴⁾	All pins	±1500 V
Continuous power dissipation		See Dissipation Rating Table	
Storage temperature range		−65°C to 150°C	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	3	3.3	3.6	V
V _{IH}	High-level input voltage	2		V _{CC}	V
V _{IL}	Low-level input voltage	GND		0.8	V
	Voltage at any bus terminal V _A , V _B , V _Y or V _Z	−1.4		3.8	V
V _{ID}	Magnitude of differential input voltage	0.05		V _{CC}	V
T _A	Operating free-air temperature	−40		85	°C

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I _{CC}	Supply current	Driver only		13	22	mA
		Both disabled		1	4	
		Both enabled		16	24	
		Receiver only		4	13	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT
V _{AB} or V _{YZ}	Differential output voltage magnitude	See Figure 2	480		650	mV
Δ V _{AB} or Δ V _{YZ}	Change in differential output voltage magnitude between logic states		-50		50	mV
V _{OS(SS)}	Steady-state common-mode output voltage	See Figure 3	0.8		1.2	V
ΔV _{OS(SS)}	Change in steady-state common-mode output voltage between logic states		-50		50	mV
V _{OS(PP)}	Peak-to-peak common-mode output voltage				150	mV
V _{Y(OC)} or V _{A(OC)}	Maximum steady-state open-circuit output voltage	See Figure 7	0		2.4	V
V _{Z(OC)} or V _{B(OC)}	Maximum steady-state open-circuit output voltage		0		2.4	V
V _{P(H)}	Voltage overshoot, low-to-high level output	See Figure 5			1.2 V _{SS}	V
V _{P(L)}	Voltage overshoot, high-to-low level output		-0.2 V _{SS}			V
I _{IH}	High-level input current (D, DE)	V _{IH} = 2 V	0		10	μA
I _{IL}	Low-level input current (D, DE)	V _{IL} = 0.8 V	0		10	μA
J _{I_{OS}J}	Differential short-circuit output current magnitude	See Figure 4			24	mA
I _{OZ}	High-impedance state output current (driver only)	-1.4 V ≤ V _Y or V _Z ≤ 3.8 V, Other output = 1.2 V	-15		10	μA
I _{O(OFF)}	Power-off output current	-1.4 V ≤ V _Y or V _Z ≤ 3.8 V, Other output = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	-10		10	μA
C _Y or C _Z	Output capacitance	V _I = 0.4 sin(30E6πt) + 0.5 V, ⁽³⁾ Other input at 1.2 V, Driver disabled		3		pF
C _{YZ}	Differential output capacitance	V _{AB} = 0.4 sin(30E6πt) V, ⁽³⁾ Driver disabled			2.5	pF
C _{Y/Z}	Output capacitance balance, (C _Y /C _Z)		0.99		1.01	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) All typical values are at 25°C and with a 3.3-V supply voltage.

(3) HP4194A impedance analyzer (or equivalent)

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going differential input voltage threshold	Type 1			50	mV
		Type 2			150	
V _{IT-}	Negative-going differential input voltage threshold	Type 1	See Figure 9 and Table 1 and Table 2		-50	mV
		Type 2			50	
V _{HYS}	Differential input voltage hysteresis, (V _{IT+} - V _{IT-})	Type 1			25	mV
		Type 2			0	
V _{OH}	High-level output voltage	I _{OH} = -8 mA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8 mA			0.4	V
I _{IH}	High-level input current (\overline{RE})	V _{IH} = 2 V	-10		0	μA
I _{IL}	Low-level input current (\overline{RE})	V _{IL} = 0.8 V	-10		0	μA
I _{OZ}	High-impedance output current	V _O = 0 V or 3.6 V	-10		15	μA
C _A or C _B	Input capacitance	V _I = 0.4 sin(30E6πt) + 0.5 V, ⁽²⁾ Other input at 1.2 V		3		pF
C _{AB}	Differential input capacitance	V _{AB} = 0.4 sin(30E6πt) V ⁽²⁾			2.5	pF
C _{A/B}	Input capacitance balance, (C _A /C _B)		0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

BUS INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I _A	Receiver or transceiver with driver disabled input current	V _A = 3.8 V, V _B = 1.2 V,	0		32	μA
		V _A = 0 V or 2.4 V, V _B = 1.2 V	-20		20	
		V _A = -1.4 V, V _B = 1.2 V	-32		0	
I _B	Receiver or transceiver with driver disabled input current	V _B = 3.8 V, V _A = 1.2 V	0		32	μA
		V _B = 0 V or 2.4 V, V _A = 1.2 V	-20		20	
		V _B = -1.4 V, V _A = 1.2 V	-32		0	
I _{AB}	Receiver or transceiver with driver disabled differential input current (I _A - I _B)	V _A = V _B , 1.4 ≤ V _A ≤ 3.8 V	-4		4	μA
I _{A(OFF)}	Receiver or transceiver power-off input current	V _A = 3.8 V, V _B = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	0		32	μA
		V _A = 0 V or 2.4 V, V _B = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	-20		20	
		V _A = -1.4 V, V _B = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	-32		0	
I _{B(OFF)}	Receiver or transceiver power-off input current	V _B = 3.8 V, V _A = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	0		32	μA
		V _B = 0 V or 2.4 V, V _A = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	-20		20	
		V _B = -1.4 V, V _A = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	-32		0	
I _{AB(OFF)}	Receiver input or transceiver power-off differential input current (I _A - I _B)	V _A = V _B , 0 V ≤ V _{CC} ≤ 1.5 V, -1.4 ≤ V _A ≤ 3.8 V	-4		4	μA
C _A	Transceiver with driver disabled input capacitance	V _A = 0.4 sin(30E6πt) + 0.5V ⁽²⁾ , V _B = 1.2 V		5		pF
C _B	Transceiver with driver disabled input capacitance	V _B = 0.4 sin(30E6πt) + 0.5 V ⁽²⁾ , V _A = 1.2 V		5		pF
C _{AB}	Transceiver with driver disabled differential input capacitance	V _{AB} = 0.4 sin(30E6πt)V ⁽²⁾			3	pF
C _{A/B}	Transceiver with driver disabled input capacitance balance, (C _A /C _B)		0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	See Figure 5	1	1.5	2.4	ns
t _{PHL}	Propagation delay time, high-to-low-level output		1	1.5	2.4	ns
t _r	Differential output signal rise time		1		1.6	ns
t _f	Differential output signal fall time		1		1.6	ns
t _{sk(pp)}	Pulse skew (t _{PHL} - t _{PLH})			0	100	ps
t _{sk(pp)}	Part-to-part skew ⁽²⁾				1	ns
t _{jit(per)}	Period jitter, rms (1 standard deviation) ⁽³⁾	100 MHz clock input ⁽⁴⁾		2	3	ps
t _{jit(pp)}	Peak-to-peak jitter ^{(3) (5)}	200 Mbps 2 ¹⁵ -1 PRBS input ⁽⁶⁾		30	130	ps
t _{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 6			7	ns
t _{PLZ}	Disable time, low-level-to-high-impedance output				7	ns
t _{PZH}	Enable time, high-impedance-to-high-level output				7	ns
t _{PZL}	Enable time, high-impedance-to-low-level output				7	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) t_{sk(pp)} is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.

(4) t_r = t_f = 0.5 ns (10% to 90%), measured over 30 k samples.

(5) Peak-to-peak jitter includes jitter due to pulse skew (t_{sk(pp)}).

(6) t_r = t_f = 0.5 ns (10% to 90%), measured over 100 k samples.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
t_{pLH}	Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, See Figure 10	2	4	6	ns	
t_{pHL}	Propagation delay time, high-to-low-level output		2	4	6	ns	
t_r	Output signal rise time		1		2.3	ns	
t_f	Output signal fall time		1		2.3	ns	
$t_{sk(p)}$	Pulse skew ($ t_{pHL} - t_{pLH} $)		Type 1		100	300	ps
			Type 2		300	500	ps
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾				1	ns	
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) ⁽³⁾		100 MHz clock input ⁽⁴⁾		4	7	ps
$t_{jit(pp)}$	Peak-to-peak jitter ⁽³⁾⁽⁵⁾		Type 1		300	700	ps
			Type 2		450	800	ps
t_{pHZ}	Disable time, high-level-to-high-impedance output	See Figure 11			10	ns	
t_{pLZ}	Disable time, low-level-to-high-impedance output				10	ns	
t_{pZH}	Enable time, high-impedance-to-high-level output				15	ns	
t_{pZL}	Enable time, high-impedance-to-low-level output				15	ns	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.

(4) $V_{ID} = 200 \text{ mV}_{pp}$ (LVD201, 203), $V_{ID} = 400 \text{ mV}_{pp}$ (LVD206, 207), $V_{cm} = 1 \text{ V}$, $t_r = t_f = 0.5 \text{ ns}$ (10% to 90%), measured over 30 k samples.

(5) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).

(6) $V_{ID} = 200 \text{ mV}_{pp}$ (LVD201, 203), $V_{ID} = 400 \text{ mV}_{pp}$ (LVD206, 207), $V_{cm} = 1 \text{ V}$, $t_r = t_f = 0.5 \text{ ns}$ (10% to 90%), measured over 100 k samples.

PARAMETER MEASUREMENT INFORMATION

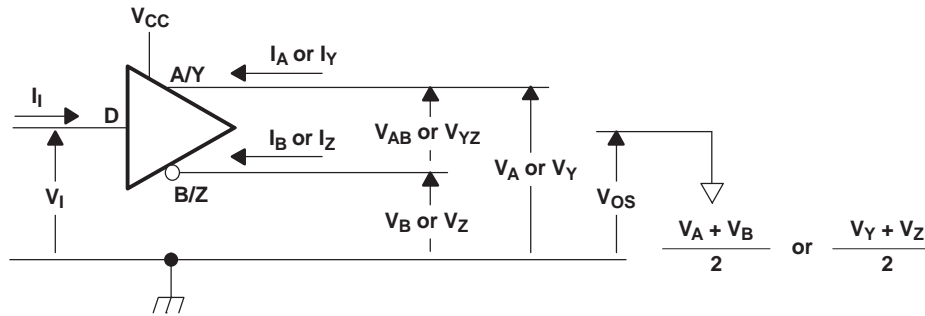
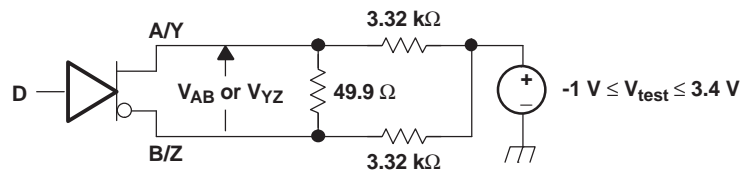
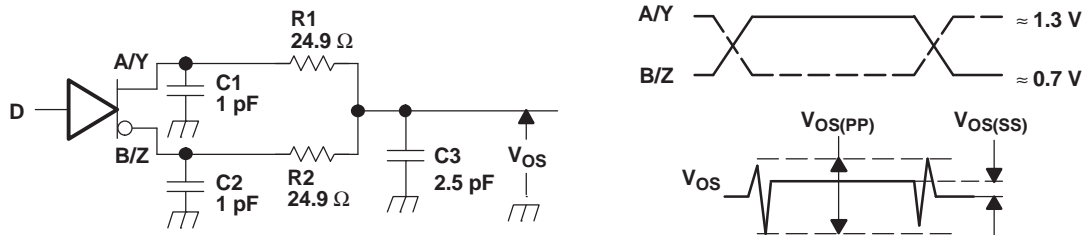


Figure 1. Driver Voltage and Current Definitions



- A. All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse frequency = 500 kHz, duty cycle = $50 \pm 5\%$.
- B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.
- C. R1 and R2 are metal film, surface mount, 1%, and located within 2 cm of the D.U.T.
- D. The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

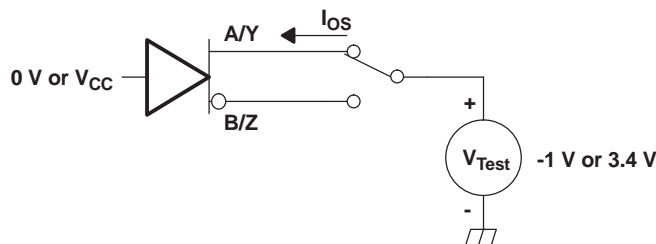
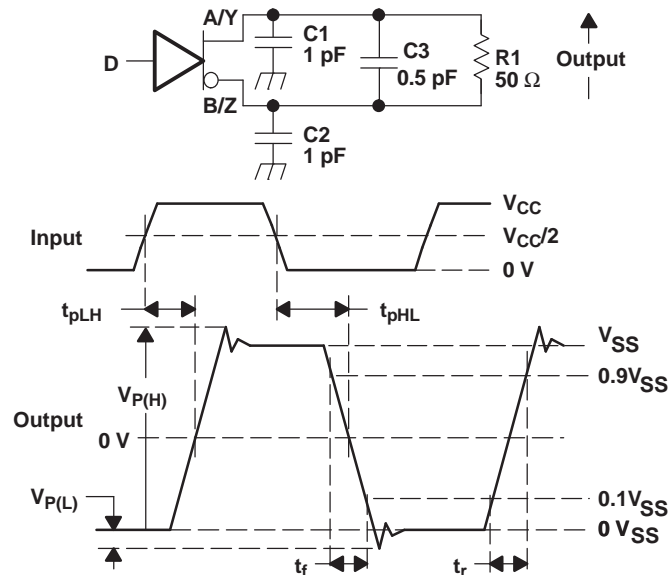


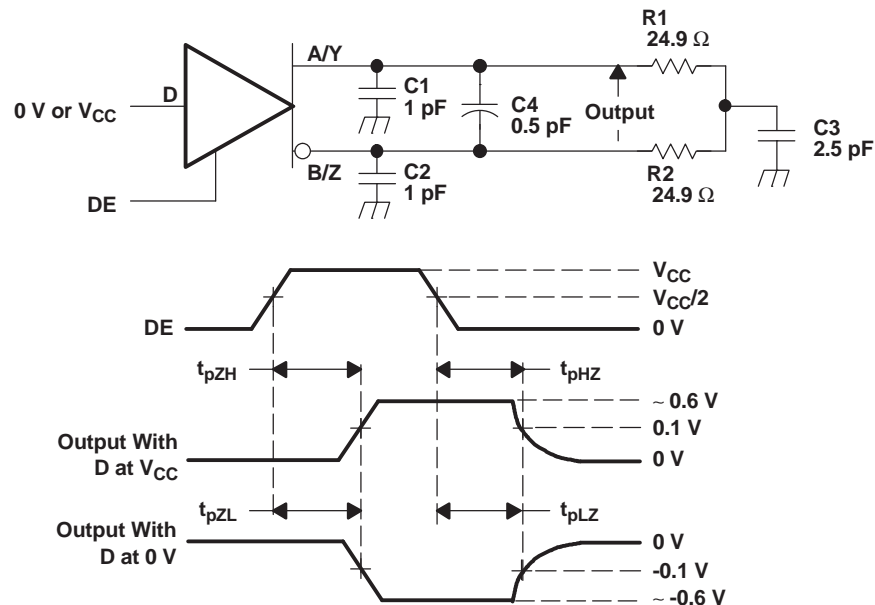
Figure 4. Driver Short-Circuit Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 500 kHz, duty cycle = 50%.
- B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.
- C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 500 kHz, duty cycle = 50%.
- B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.
- C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 6. Driver Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

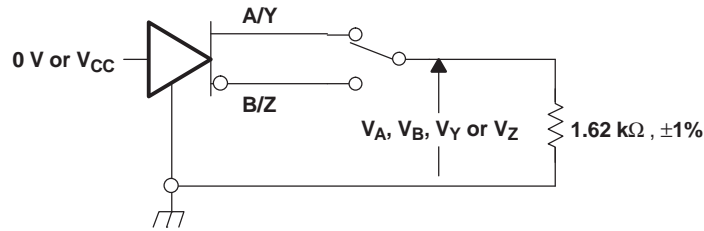
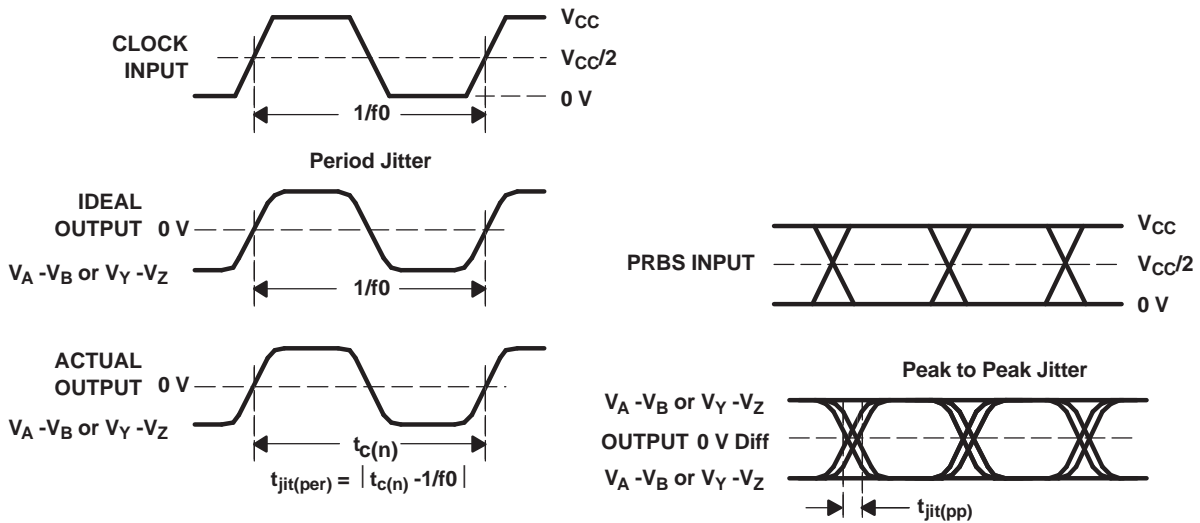


Figure 7. Maximum Steady State Output Voltage



- A. All input pulses are supplied by an Agilent 8304A Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter is measured using a 100 MHz 50% duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 200Mbps $2^{15}-1$ PRBS input.

Figure 8. Driver Jitter Measurement Waveforms

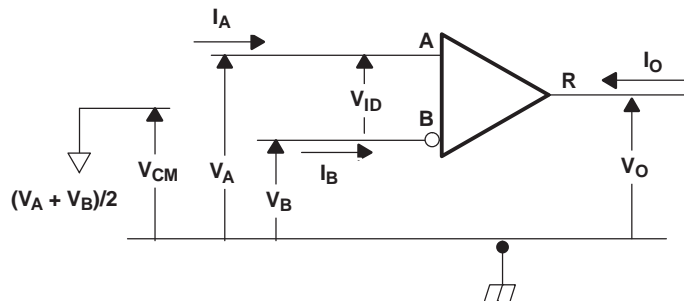


Figure 9. Receiver Voltage and Current Definitions

Table 1. Type-1 Receiver Input Threshold Test Voltages

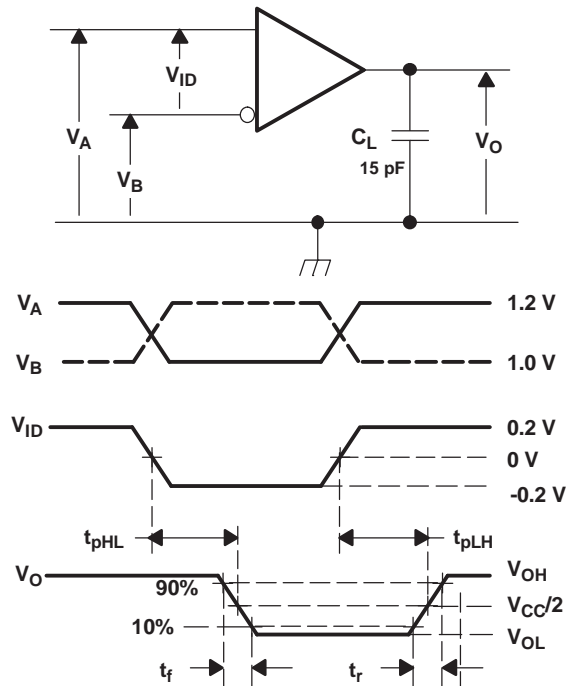
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT ⁽¹⁾
V _{IA}	V _{IB}	V _{ID}	V _{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	-2.400	1.200	L
3.800	3.750	0.050	3.775	H
3.750	3.800	-0.050	3.775	L
-1.350	-1.400	0.050	-1.375	H
-1.400	-1.350	-0.050	-1.375	L

(1) H = high level, L = low level, output state assumes receiver is enabled ($\overline{RE} = L$)

Table 2. Type-2 Receiver Input Threshold Test Voltages

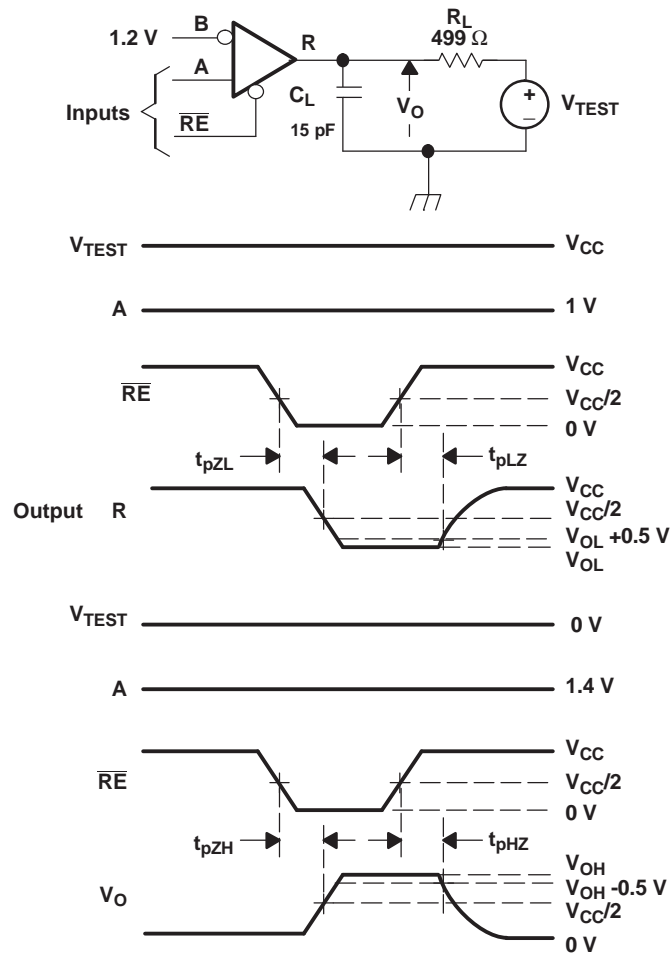
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT ⁽¹⁾
V _{IA}	V _{IB}	V _{ID}	V _{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	-2.400	1.200	L
3.800	3.650	0.150	3.725	H
3.800	3.750	0.050	3.775	L
-1.250	-1.400	0.150	-1.325	H
-1.350	-1.400	0.050	-1.375	L

(1) H = high level, L = low level, output state assumes receiver is enabled ($\overline{RE} = L$)



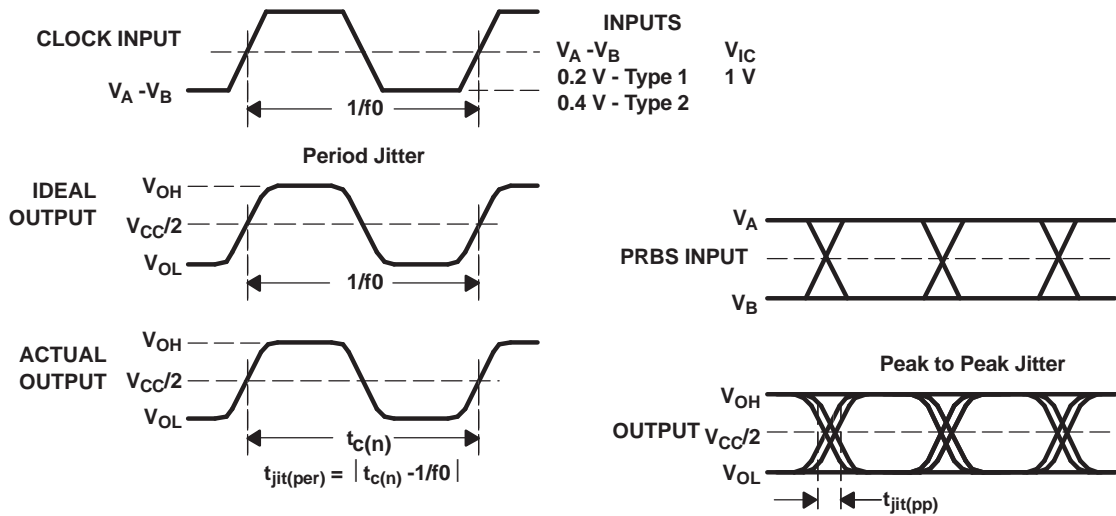
- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 50 MHz, duty cycle = 50%. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.
- B. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 10. Receiver Timing Test Circuit and Waveforms



- All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 500 kHz, duty cycle = 50%.
- R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
- R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
- C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and 20%.

Figure 11. Receiver Enable/Disable Time Test Circuit and Waveforms

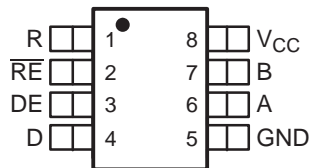


- All input pulses are supplied by an Agilent 8304A Stimulus System.
- The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- Period jitter is measured using a 100 MHz 50% duty cycle clock input.
- Peak-to-peak jitter is measured using a 200 Mbps $2^{15}-1$ PRBS input.

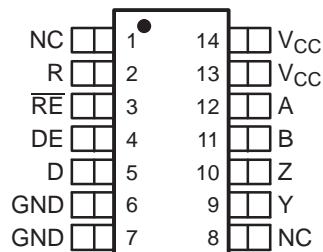
Figure 12. Receiver Jitter Measurement Waveforms

PIN ASSIGNMENTS

SN65MLVD201D (Marked as MF201)
SN65MLVD206D (Marked as MF206)
(TOP VIEW)



SN65MLVD203D (Marked as MLVD203)
SN65MLVD207D (Marked as MLVD207)
(TOP VIEW)



NC - No internal connection

DEVICE FUNCTION TABLES

TYPE-1 RECEIVER (201, 203)			TYPE-2 RECEIVER (206, 207)		
INPUTS		OUTPUT	INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	\overline{RE}	R	$V_{ID} = V_A - V_B$	\overline{RE}	R
$V_{ID} \geq 50 \text{ mV}$	L	H	$V_{ID} \geq 150 \text{ mV}$	L	H
$-50 \text{ mV} < V_{ID} < 50 \text{ mV}$	L	?	$50 \text{ mV} < V_{ID} < 150 \text{ mV}$	L	?
$V_{ID} \leq -50 \text{ mV}$	L	L	$V_{ID} \leq 50 \text{ mV}$	L	L
X	H	Z	X	H	Z
X	Open	Z	X	Open	Z
Open Circuit	L	?	Open Circuit	L	L

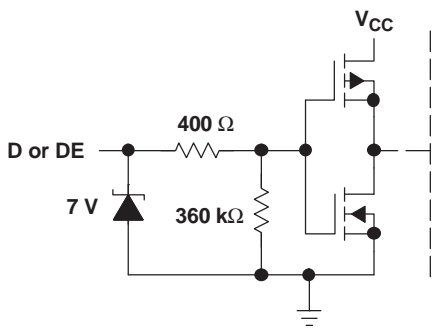
DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	A OR Y	B OR Z
L	H	L	H
H	H	H	L
OPEN	H	L	H
X	OPEN	Z	Z
X	L	Z	Z

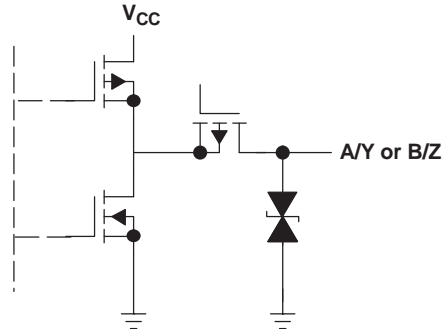
H = high level, L = low level, Z = high impedance, X = Don't care, ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

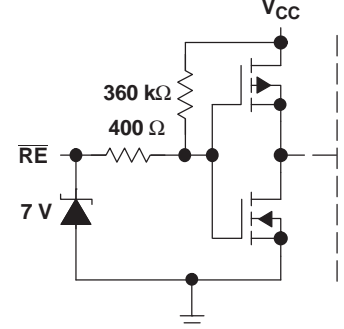
DRIVER INPUT AND DRIVER ENABLE



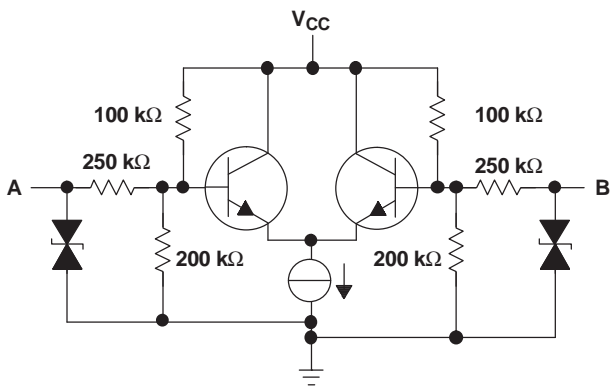
DRIVER OUTPUT



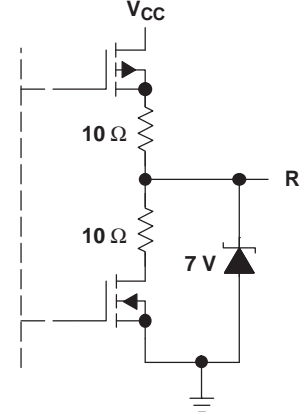
RECEIVER ENABLE



RECEIVER INPUT



RECEIVER OUTPUT



TYPICAL CHARACTERISTICS

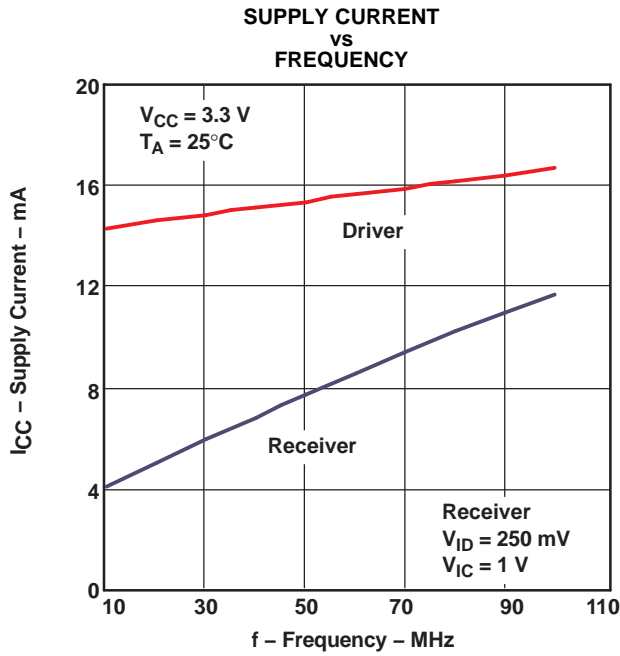


Figure 13.

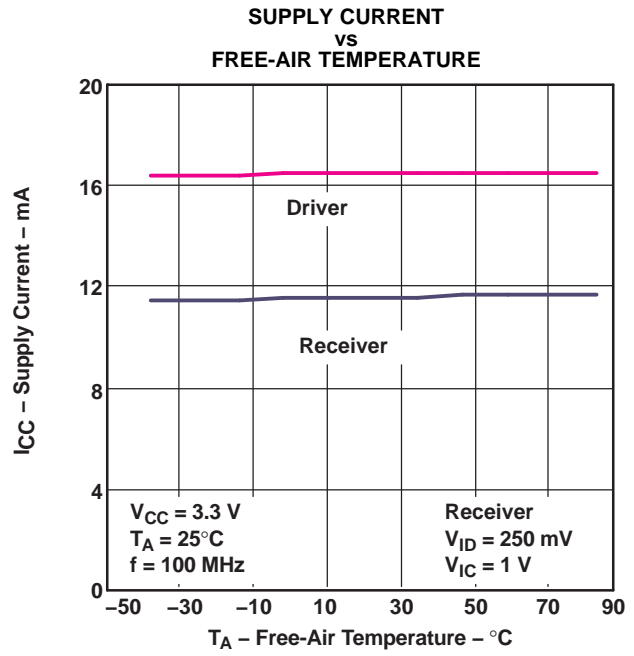


Figure 14.

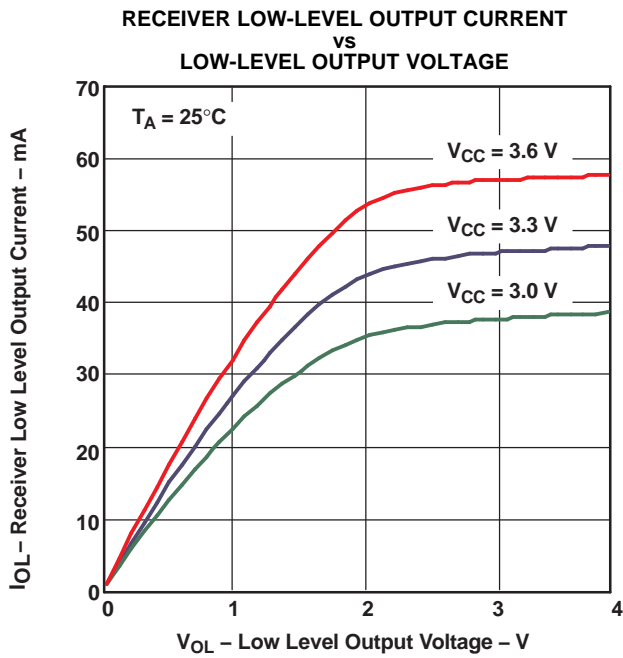


Figure 15.

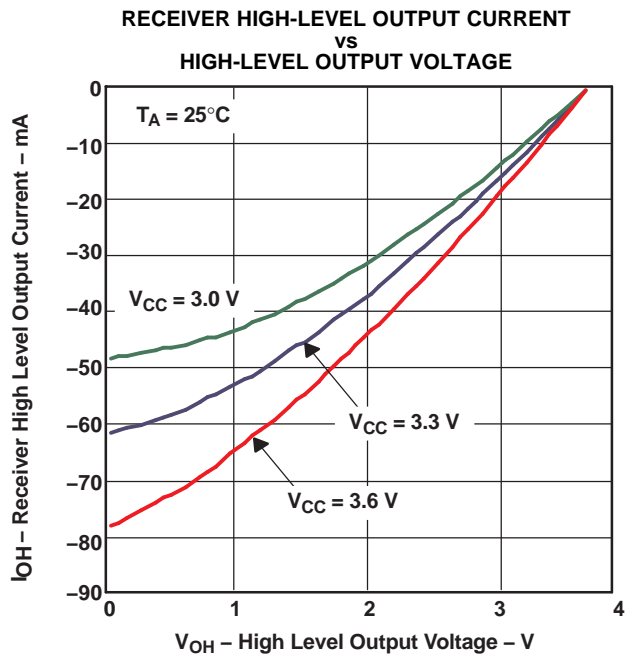
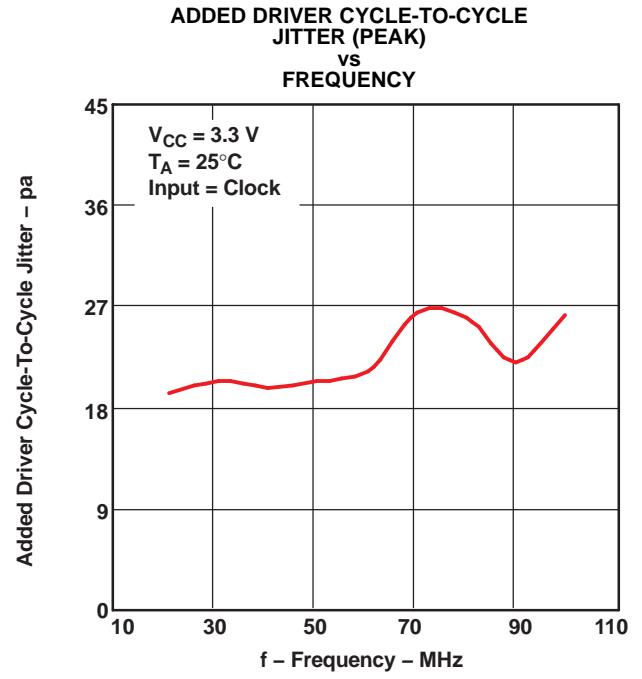
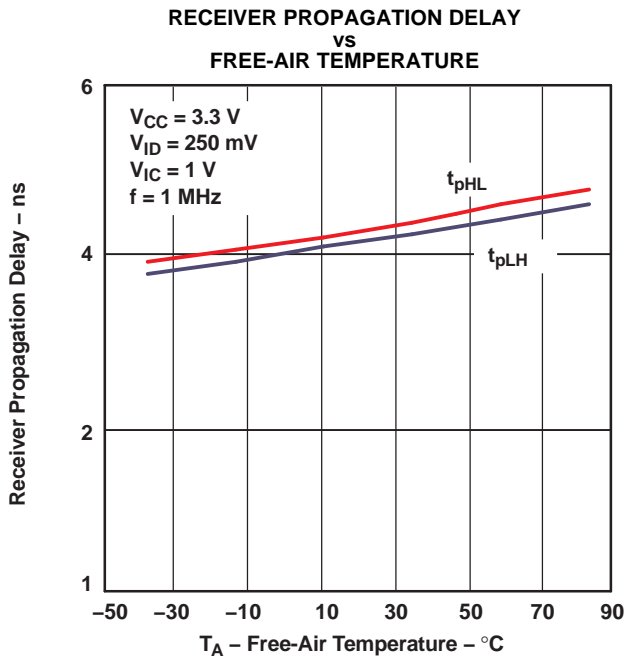
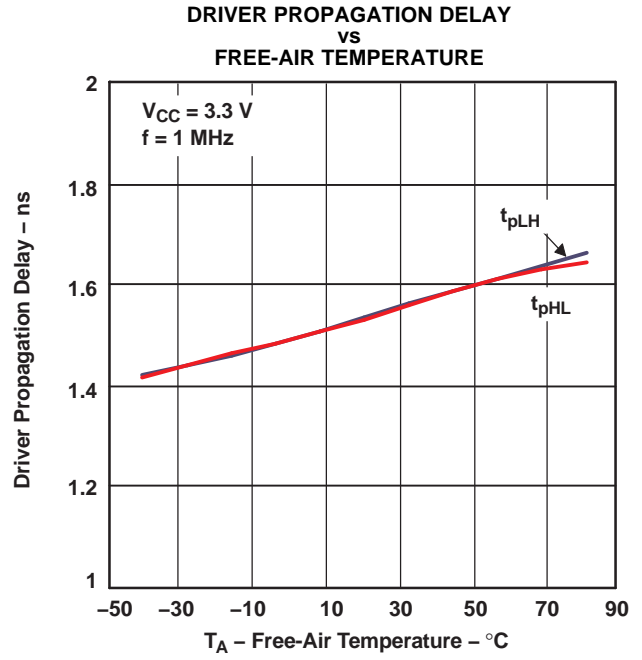
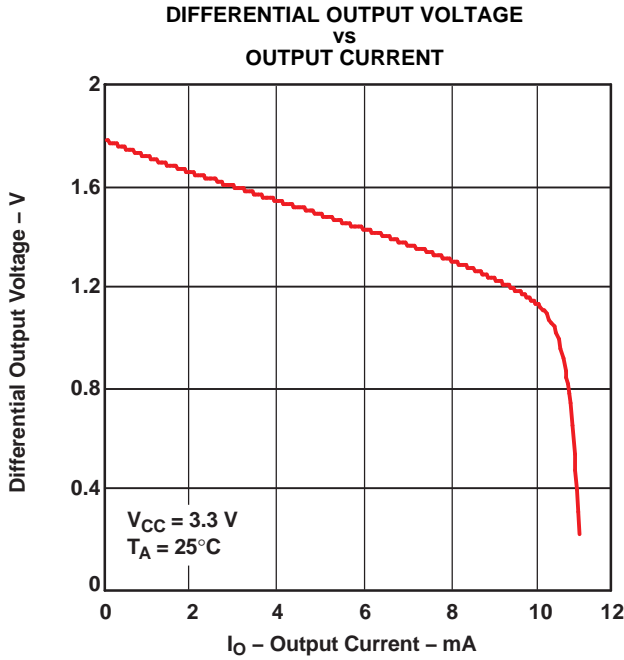


Figure 16.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

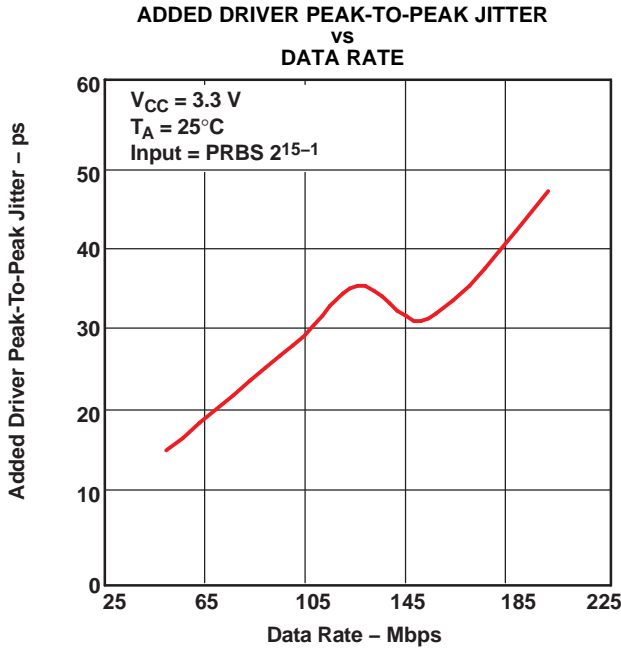


Figure 21.

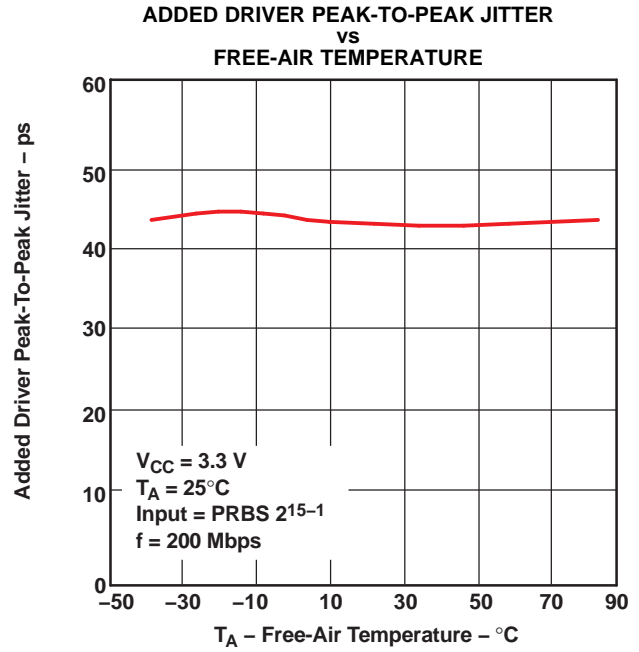


Figure 22.

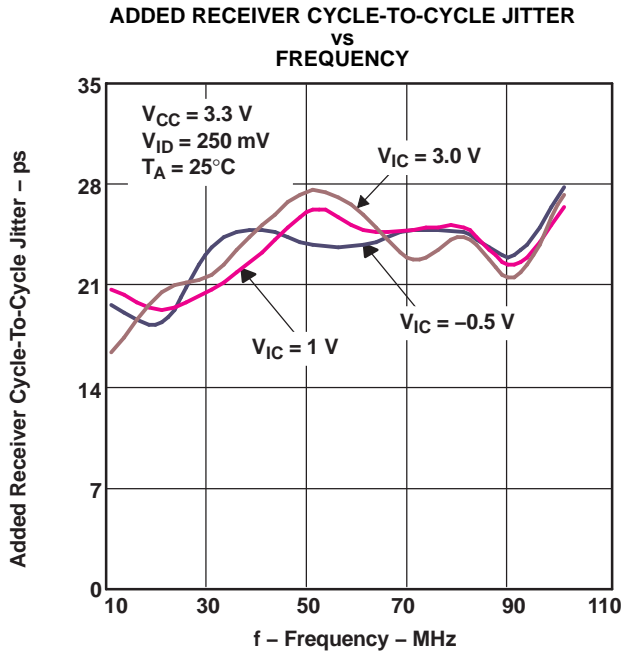


Figure 23.

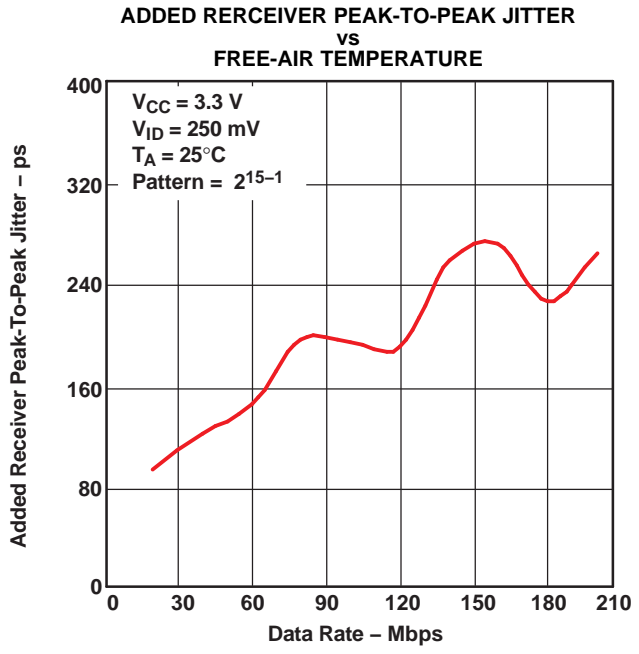


Figure 24.

TYPICAL CHARACTERISTICS (continued)

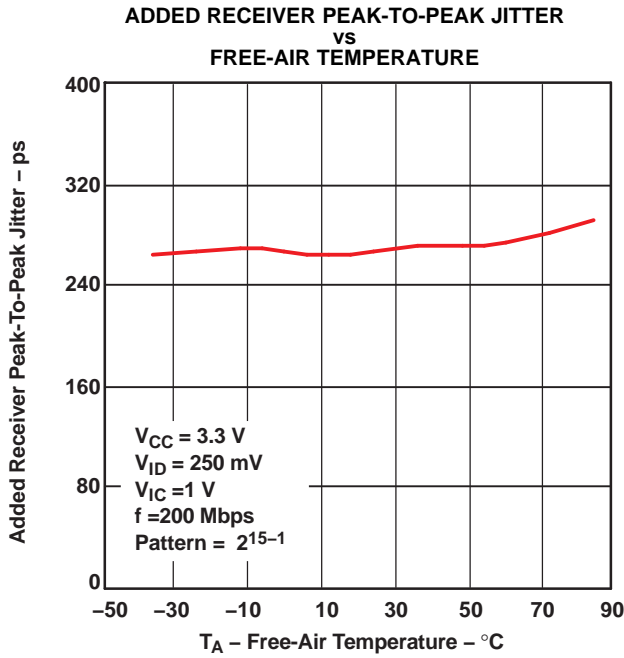


Figure 25.

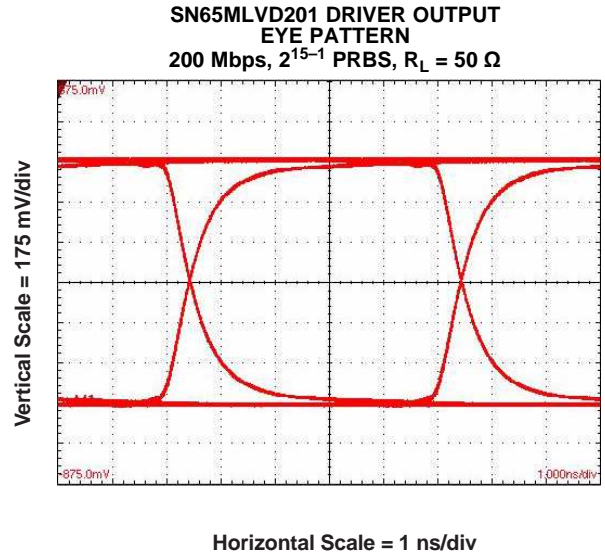


Figure 26.

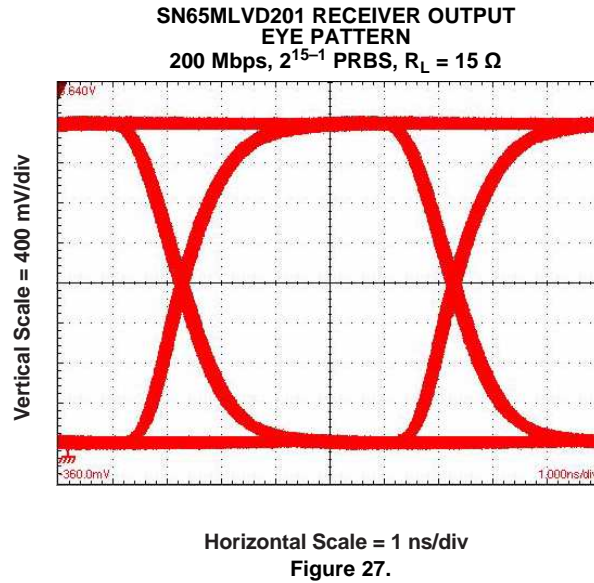


Figure 27.

APPLICATION INFORMATION

Receiver Input Threshold (Failsafe)

The MLVD standard defines a type 1 and type 2 receiver. Type 1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts. Type 2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in [Table 3](#) and [Figure 28](#).

Table 3. Receiver Input Voltage Threshold Requirements

RECEIVER TYPE	OUTPUT LOW	OUTPUT HIGH
Type 1	$-2.4 \text{ V} \leq V_{ID} \leq -0.05 \text{ V}$	$0.05 \text{ V} \leq V_{ID} \leq 2.4 \text{ V}$
Type 2	$-2.4 \text{ V} \leq V_{ID} \leq 0.05 \text{ V}$	$0.15 \text{ V} \leq V_{ID} \leq 2.4 \text{ V}$

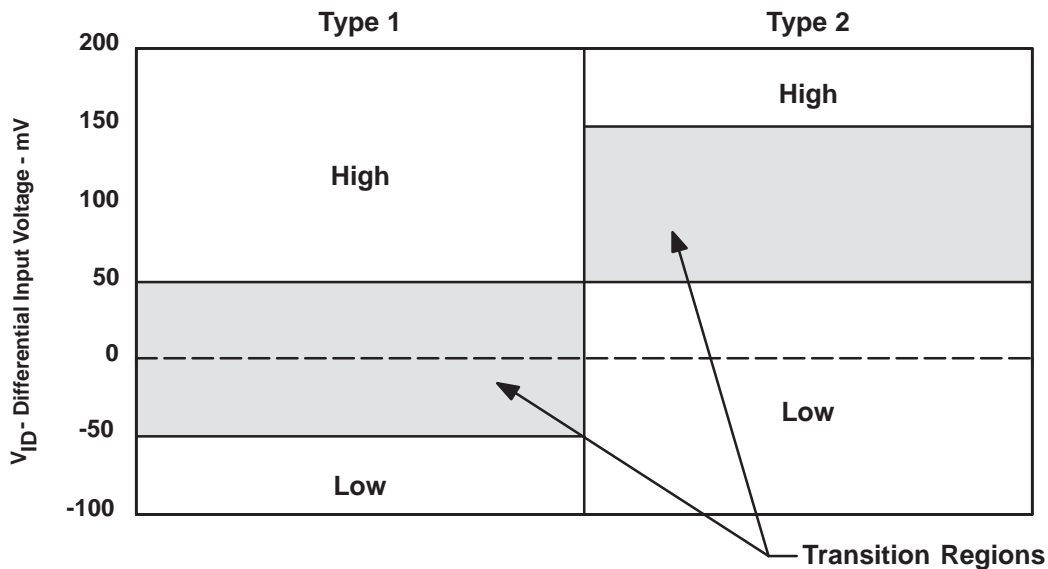


Figure 28. Expanded Graph of Receiver Differential Input Voltage Showing Transition Region

LIVE INSERTION/GLITCH-FREE POWER UP/DOWN

The SN65MLVD201/203/206/207 family of products offered by Texas Instruments provides a glitch-free powerup/down feature that prevents the M-LVDS outputs of the device from turning on during a powerup or powerdown event. This is especially important in live insertion applications, when a device is physically connected to an M-LVDS multipoint bus and VCC is ramping.

While the M-LVDS interface for these devices is glitch free on powerup/down, the receiver output structure is not. [Figure 29](#) shows the performance of the receiver output pin, R (CHANNEL 2), as Vcc (CHANNEL 1) is ramped.

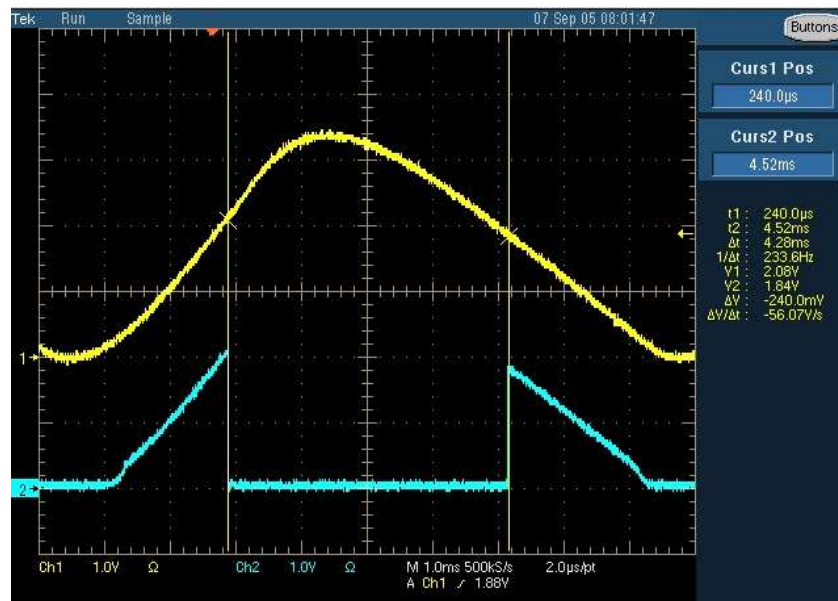


Figure 29. M-LVDS Receiver Output: VCC (CHANNEL 1), R Pin (CHANNEL 2)

The glitch on the R pin is independent of the \overline{RE} voltage. Any complications or issues from this glitch are easily resolved in power sequencing or system requirements that suspend operation until VCC has reached a steady state value.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65MLVD201D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF201	Samples
SN65MLVD201DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF201	Samples
SN65MLVD201DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF201	Samples
SN65MLVD203D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD203	Samples
SN65MLVD203DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD203	Samples
SN65MLVD203DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD203	Samples
SN65MLVD206D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF206	Samples
SN65MLVD206DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF206	Samples
SN65MLVD206DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF206	Samples
SN65MLVD207D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD207	Samples
SN65MLVD207DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD207	Samples
SN65MLVD207DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD207	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD201DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65MLVD203DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65MLVD206DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65MLVD207DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD201DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65MLVD203DR	SOIC	D	14	2500	340.5	336.1	32.0
SN65MLVD206DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65MLVD207DR	SOIC	D	14	2500	340.5	336.1	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65MLVD201D	D	SOIC	8	75	507	8	3940	4.32
SN65MLVD201DG4	D	SOIC	8	75	507	8	3940	4.32
SN65MLVD203D	D	SOIC	14	50	507	8	3940	4.32
SN65MLVD203DG4	D	SOIC	14	50	507	8	3940	4.32
SN65MLVD206D	D	SOIC	8	75	507	8	3940	4.32
SN65MLVD206DG4	D	SOIC	8	75	507	8	3940	4.32
SN65MLVD207D	D	SOIC	14	50	507	8	3940	4.32
SN65MLVD207DG4	D	SOIC	14	50	507	8	3940	4.32

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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