CALMOS™

DECEMBER 1989

CA82C52

CMOS SERIAL CONTROLLER INTERFACE

- Pin and functional compatibility with the industry standard 8252
- TTL input/output compatibility
- Low power CMOS implementation
- High speed - DC to 16 MHz operation
- Single chip UART/BRG
- Crystal or external clock input
- On chip baud rate generator featuring 72 selectable baud rates
- Interrupt mode with mask capability
- Microprocessor bus oriented interface
- Line break generation and detection
- Loopback and echo modes
- Fully static operation

The CA82C52 is a high performance, single chip programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG). The Baud Rate Generator can be programmed for one of 72 different baud rates using a single industry standard crystal or external frequency source. A programmable buffered clock output is available and can be programmed to provide either a buffered oscillator or 16X baud rate clock for general purpose system usage.

The CA82C52 features full TTL/CMOS compatibility, allowing it to be designed into mixed TTL/NMOS/CMOS system environments. Its high speed and high performance make it ideally suited for aerospace and defense applications, while a very low power consumption suits it to portable systems and systems with low power standby modes.

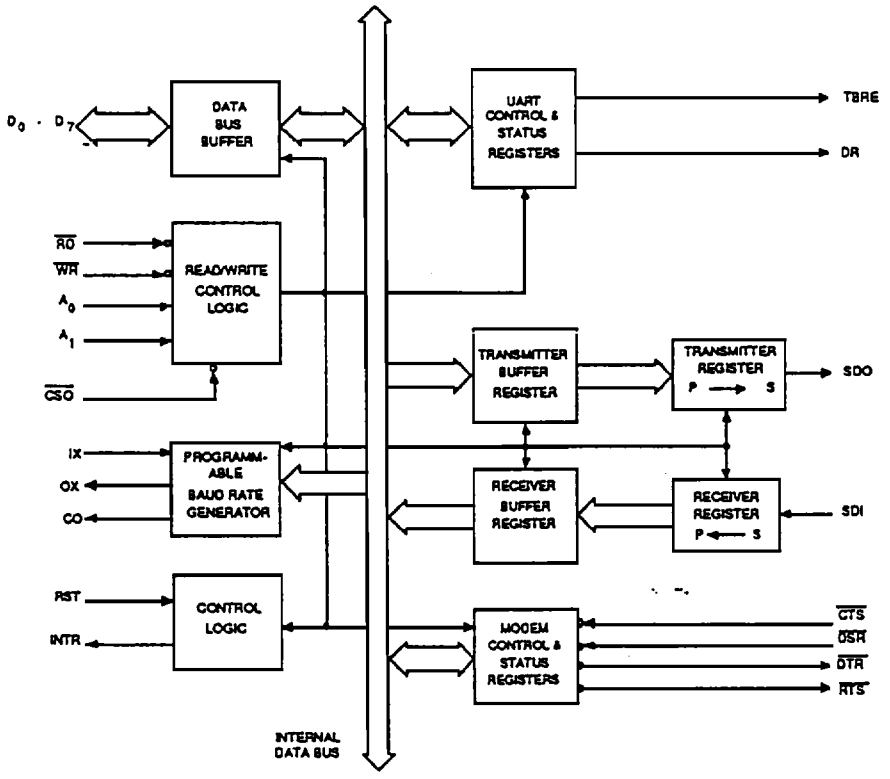


Figure 1 : CA82C52 BLOCK DIAGRAM

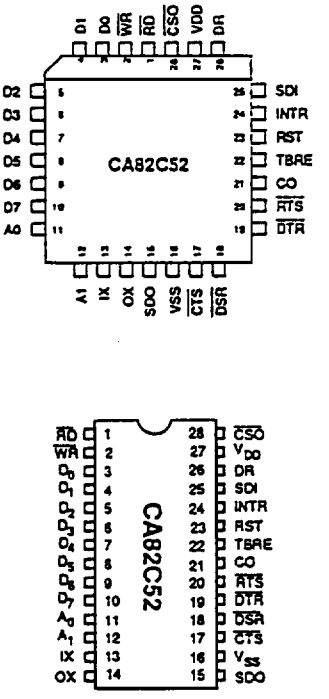


Figure 2 : PLCC and PDIP PIN CONFIGURATIONS

Table 1 : PIN DESCRIPTIONS

Symbol	Pins		Type	Name and Function
	PLCC	PDIP		
A_0, A_1	11, 12	11, 12	I	**Address Inputs:** The address lines select the various internal registers during CPU bus operations.
CO	21	21	O	**Clock Out:** This output is user programmable to provide either a buffered IX output or a buffered Baud Rate Generator (16x) clock output. The buffered IX (Crystal or external clock source) output is provided when the Baud Rate Select Register (BRSR) bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at 16 times the programmed baud rate.
$\overline{CSO}$	28	28	I	**Chip Select:** Chip select acts as an enable signal for the $\overline{RD}$ and $\overline{WR}$ input signals.
$\overline{CTS}$	17	17	I	**Clear to Send:** The logical state of the $\overline{CTS}$ line is reflected in the $\overline{CTS}$ bit of the Modem Status Register. Any change of state in $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SDO output and will hold SDO in the Mark (high) state. If $\overline{CTS}$ goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect Loop Mode operation.
D_0 - D_7	3 - 10	3 - 10	I/O	**Data Bits 0 - 7:** The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the CA82C52 and the CPU. For character formats of less than 8 bits, the corresponding D_7, D_6 and D_5 are considered *don't cares* for data *write* operations and are 0 for data *read* operations. These lines are normally in a high impedance state except during read operations. D_0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
DR	26	26	O	**Data Ready:** A true level indicates that a character has been received, transferred to the RBR and is ready for transfer to the CPU. DR is reset on a data READ of the Receiver Buffer Register (RBR) or when RST is true.
$\overline{DSR}$	18	18	I	**Data Set Ready:** The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of $\overline{DSR}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the CA82C52.
$\overline{DTR}$	19	19	O	**Data Terminal Ready:** The $\overline{DTR}$ signal can be set *low* by writing a logic 1 to the appropriatebit in the Modem Control Register (MCR). This signal is cleared *high* by writing a logic 0 to the $\overline{DTR}$ bit in the MCR or whenever a RST (high) is applied to the CA82C52.
INTR	24	24	O	**Interrupt Request:** The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit selectively enables modem status changes to provide an input to the INTR logic. Figure 15 shows the overall relationship of these interrupt control signals.
IX, OX	13, 14	13, 14	I/O	**Crystal/Clock:** Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
$\overline{RD}$	1	1	I	**Read:** The $\overline{RD}$ input causes the CA82C52 to output data to the data bus (D_0 - D_7). The data output depends upon the state of the address inputs (A_0, A_1). $\overline{CSO}$ enables the $\overline{RD}$ input.
RST	23	23	I	**Reset:** The RST input forces the CA82C52 into an *Idle* mode in which serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits, which are set. The CA82C52 remains in an *Idle* state until programmed to resume serial data activities. The RST input is a Schmitt trigger input.
$\overline{RTS}$	20	20	O	**Request to Send:** The $\overline{RTS}$ signal can be set *low* by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared *high* by writing a logic 0 to the $\overline{RTS}$ bit in the MCR or whenever a reset RST (high) is applied to the CA82C52.
SDI	25	25	I	**Serial Data Input:** Serial data input to the CA82C52 receiver circuits. A Mark (1) is high, and a Space (0) is *low*. Data inputs on SDI are disabled when operating in the loop mode or when RST is true.

Table 1 : PIN DESCRIPTIONS (cont'd)

Symbol	Pins		Type	Name and Function
	PLCC	PDIP		
SDO	15	15	O	**Serial Data Output:** Serial data output from the CA82C52 transmitter circuitry. A Mark (1) is a logic one (*high*) and Space (0) is a logic zero (*low*). SDO is held in the Mark condition when the transmitter is disabled, when CTS is false, RST is true, when the Transmitter Register is empty, or when in the Loop Mode.
TBRE	22	22	O	**Transmitter Buffer Register Empty:** The TBRE output is set *high* whenever the Transmitter Buffer Register (TBR) has transferred its data to the Transmitter Register. Application of a reset (RST) to the CA82C52 will also set the TBRE output. TBRE is cleared *low* whenever data is written to the TBR.
V_{DD}	27	27	-	**Power:** 5V ± 10% DC Supply
V_{SS}	16	16	-	**Ground:** 0 V
$\overline{WR}$	2	2	I	**Write:** The $\overline{WR}$ input causes data from the data bus (D_0 - D_7) to be input to the CA82C52. Addressing and chip select action is the same as for read operations.

FUNCTIONAL DESCRIPTION

The CA82C52 UART contains a programmable baud rate generator that provides clocking for the transmitter and receiver circuits. The clock output, CO, is a buffered version of either the clock input (IX) to the device or a clock rate that is 16 x the actual baud rate generated.

The transmitter is used for sending serial data out through the SDO pin. The Transmitter Buffer Register accepts 5- to 8-bit wide parallel data from the data bus and transfers it to the Transmitter Register which then shifts the data out serially through the SDO pin. This form of double buffering technique allows continuous data flow transmission.

The receiver accepts serial data via the SDI pin and converts it to parallel form for the system CPU to read. Data is received serially into the Receiver Shift Register from the SDI pin, then sent to the Receiver Buffer Register for access by the CPU. The receiver also detects parity errors, overrun errors, frame errors and break characters.

The Modem Control and Status block provides the means for communicating with the modem or data set. The Modem Control Register is used to select one of four modes of communication; normal mode, loop mode, echo mode and transmit break. The Modem Control Register defines which interrupts will be enabled and will also set the modem control output lines, $\overline{RTS}$ and $\overline{DTR}$. The Modem Status Register keeps track of any changes in the modem control input lines, $\overline{CTS}$ and $\overline{DSR}$, as well as allowing the CPU to read their inputs.

The format of the data character being transmitted (eg: number of data bits, parity control and the number of stop bits) is controlled by the UART Control Register. Changes in the status of the device at any given time is reflected in the UART Status Register.

Operating Modes

Normal Mode: Configures the CA82C52 for normal full or half-duplex communications. Data will not be looped back in any form between the serial data input pin and the serial data output pin (see Figure 3a).

Transmit Break: This mode of operation causes the transmitter to transmit break characters only. A break character is composed of all logical zeros for the start, data, parity and stop bits.

Echo Mode: When selected, echo mode causes the CA82C52 to re-transmit data received on the SDI pin out to the SDO pin. In this mode of operation, any data written to the Transmitter Buffer Register will not be sent out on the SDO pin (Figure 3b).

Loop Test Mode: This mode internally re-directs data that would normally be transmitted back to the receiver circuitry. The transmitted data will not appear at the SDO pin. Also, data that is received on the SDI pin will be ignored by the device. This mode of operation is useful for performing self test(s) on the device (Figure 3c).

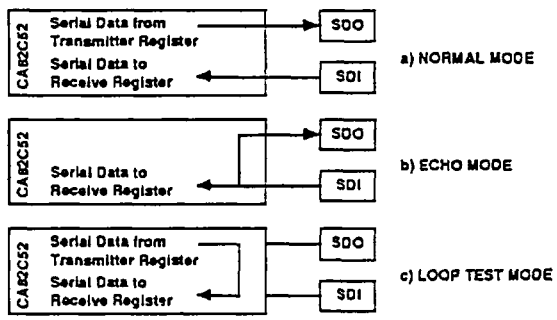


Figure 3 : OPERATING MODES

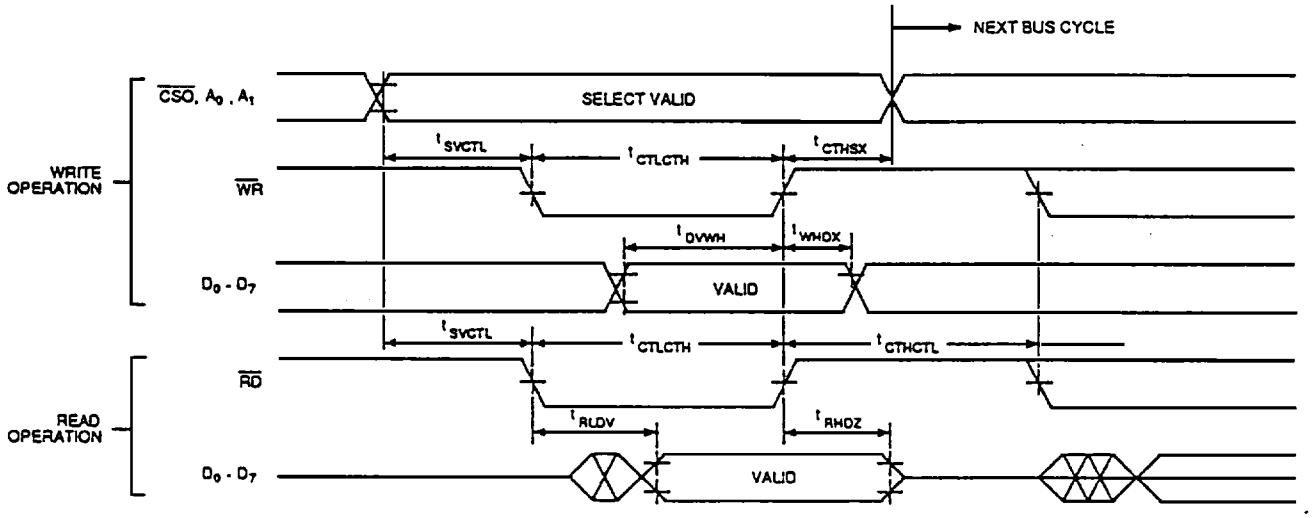
Table 2 : AC CHARACTERISTICS (T_A = –40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

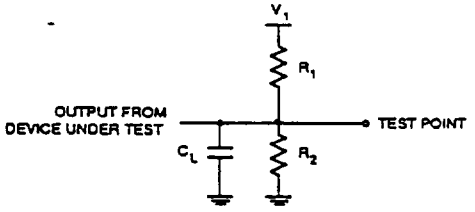
Symbol	Parameter	Test Conditions	Limits (16 MHz)		Units
			Min	Max	
FC	Clock Frequency	t_{CHCL} + t_{CLCH} must be ≥ 62.5 ns	0	16	MHz
t_{CHCL}	Clock High Time		25		ns
t_{CLCH}	Clock Low Time		25		ns
t_{CTHCTL}	Control Disable to Control Enable		190		ns
t_{CTHSX}	Select Hold From Control Trailing Edge		50		ns
t_{CTLCTH}	Control Pulse Width	Control Consists of $\overline{RD}$ or $\overline{WR}$	150		ns
t_{DVWH}	Data Setup Time		50		ns
t_{FCO}	Clock Output Fall Time	C_L = 50 pf		15	ns
t_{RCO}	Clock Output Rise Time	C_L = 50 pf		15	ns
t_{RHDZ}	Read Disable	2	0	60	ns
t_{RLDV}	Read Low to Data Valid	1		120	ns
T_R/T_F	IX Input Rise/Fall Time (External Clock)	tx ≤ $^1/_6$FC or 50 ns, whichever is smaller		tx	ns
t_{SVCTL}	Select Setup to Control Leading Edge		30		ns
t_{WHDX}	Data Hold Time		20		ns

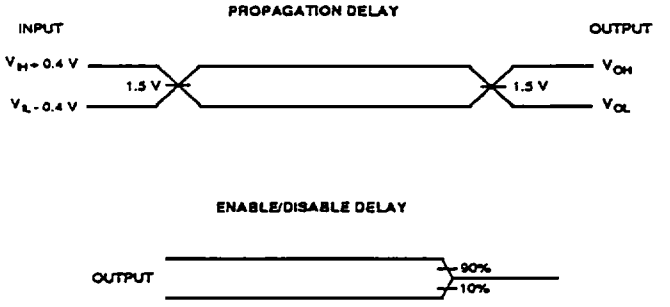
Table 3 : CAPACITANCE (T_A = 25°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits (16 MHz)		Units
			Min	Max	
C_{IN}	Input Capacitance	Freq = 1 MHz		10	pF
$C_{I/O}$	I/O Capacitance	All measurements are		15	pF
C_{OUT}	Output Capacitance	referenced to device V_{SS} (GND)		10	pF

Figure 4 : BUS OPERATION TIMING DIAGRAM







	TEST CONDITION	V_1	R_1	R_2	C_L
1	Propagation Delay	1.7 V	520	∞	100 pF
2	Disable Delay	V_{DD}	5 K	5 K	50 pF

A.C. Testing: All input signals must switch between V_{IL} - 0.4 V and V_{IH} + 0.4 V. TR and TF must be ≤ 15 ns.

Figure 5 : AC TEST CIRCUITS

Figure 6 : AC TESTING I/O WAVEFORM

Table 4 : DC CHARACTERISTICS (T_A = –40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits (16 MHz)		Units
			Min	Max	
FC	Clock Frequency	$t_{CHCL} + t_{CLCH}$ must be ≥ 62.5 ns	0	16	MHz
I_{DD}	Operating Power Supply Current (see Note 1)	External Clock F = 2.45576 MHz V_{DD} = 5.5 V, V_{IN} = V_{DD} or V_{SS} Outputs Open		3	mA
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} on input pins	–1.0	+1.0	µA
I_{OL}	I/O Leakage Current	V_{OUT} = V_{DD} or V_{SS} on 3-state pins	–10.0	+10.0	µA
V_{IH}	Input HIGH Voltage		2.0		V
V_{IH} (CLK)	Input HIGH Voltage Clock	External Clock	V_{DD} – 0.5		V
V_{IL}	Input LOW Voltage			0.8	V
V_{IL} (CLK)	Input LOW Voltage Clock	External Clock		V_{SS} + 0.5	V
V_{OH}	Output HIGH Voltage	I_{OH} = –2.5 mA	3.0		V
		I_{OH} = –100 µA	V_{DD} – 0.4		
V_{OL}	Output LOW Voltage	I_{OL} = +2.5 mA		0.4	V
V_{TH}	Schmitt Trigger Input HIGH Voltage	Reset Input	V_{DD} –0.5		V
V_{TL}	Schmitt Trigger Input LOW Voltage	Reset Input		V_{SS} + 0.5	V

Note 1 : IDD is typically ≤ 1 ma/MHz

Table 5 : RECOMMENDED OPERATING CONDITIONS

Operating Voltage Range		+4.5 V to +5.5 V
Operating Temperature Range	Commercial	0°C to +70°C
	Industrial	–40°C to +85°C
	Military	–55°C to +125°C

Table 6 : ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (V_{DD})	+8.0 V
Input (V_{IN}) or I/O Voltage Applied	V_{SS} – 0.5 V to V_{DD} + 0.5 V
Output (V_{OUT}) Voltage Applied	V_{SS} – 0.5 V to V_{DD} + 0.5 V
Maximum Power Dissipation	1 Watt
Storage Temperature	–65°C to +150°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PROGRAMMING INSTRUCTIONS

Reset

During and after power-up, the CA82C52 Reset input (RST) should be held high for at least two IX clock cycles in order to initialize and drive the CA82C52 circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur:

- Resets the internal Baud Rate Generator (BRG) circuits, clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected.
- Clears the UART Status Register (USR) except for Transmission Complete (TC) and Transmit Buffer Register Empty (TBRE) which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST = low), the CA82C52 remains in the idle mode until programmed to its desired system configuration.

Control Words

The complete functional definition of the CA82C52 is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the CA82C52 to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate etc. Once programmed, the CA82C52 is ready to perform its communication functions.

The control registers can be written to in any order. However, the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the CA82C52 is programmed and operational, these registers can be updated any time the CA82C52 is not immediately transmitting or receiving data.

Table 7 shows the control signals required to access the CA82C52 internal registers.

Table 7 : CONTROL SIGNALS

$\overline{CSO}$	A_1	A_0	$\overline{WR}$	$\overline{RD}$	Operation
0	0	0	0	1	Data Bus →Transmitter Buffer Register (TBR)
0	0	0	1	0	Receiver Buffer Register (RBR) → Data Bus
0	0	1	0	1	Data Bus → UART Control Register (UCR)
0	0	1	1	0	UART Status Register → Data Bus
0	1	0	0	1	Data Bus → Modem Control Register (MCR)
0	1	0	1	0	Modem Control Register (MCR) →Data Bus
0	1	1	0	1	Data Bus → Bit Rate Select Register (BRSR)
0	1	1	1	0	Modem Status Register (MSR) → Data Bus

UART Control Register (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D_7 and D_6 are not used but should always be set to a logic zero (0) in order to ensure software compatibility with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity.

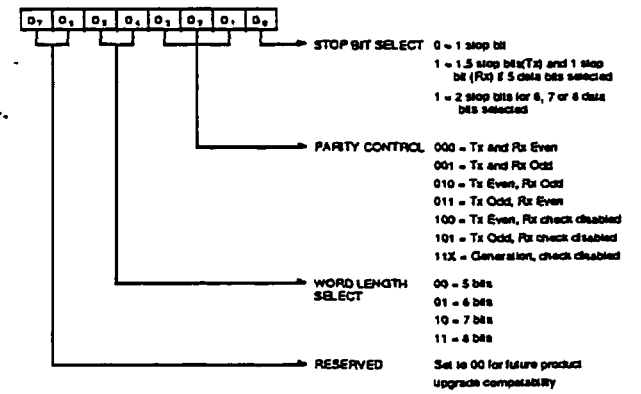


Figure 7 : UCR

Baud Rate Select Register (BRSR)

The CA82C52 is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select the divide ratio (one of 72) for the internal Baud Rate Generator circuitry. The internal circuitry is separated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates: ÷ 1, ÷ 3, ÷ 4 or ÷ 5.

The prescaler design has been optimized to provide standard baud rates using any one of three popular crystals. Using one of these system clock frequencies: 1.8432 MHz, 2.4576 MHz or 3.072 MHz and Prescaler divide ratios of ÷ 3, ÷ 4, or ÷ 5 respectively, the Prescaler output will provide a constant 614.4 KHz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 Baud to 38.4 KBaud can be selected (Table 8). Non-standard baud rates up to 1 Mbaud can be selected using different input frequencies (crystal or external frequency input up to 16 MHz) and/or different Prescaler and Divisor Select ratios.

Regardless of the baud rate, the baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1 Mbaud data rate, a 16 MHz crystal, a Prescale rate of ÷ 1, and a Divisor Select rate of *external is* used. This provides a 16 MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver circuits.

The CO select bit in the BRSR determines if the buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16x baud rate clock) is output on the CO output. The Baud Rate Generator output is always a 50% nominal duty cycle except when *external* is selected and the Prescaler is set to ÷ 3 or ÷ 5.

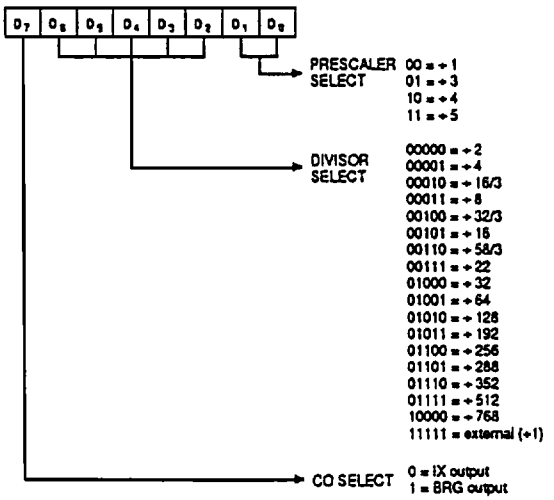


Figure 8 : BRSR

Table 8 : BAUD RATE DIVISORS

Baud Rate	Divisor
38.4 K	External
19.2 K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2400*	58/3
1800	22
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

Note: These baud rates are based upon the following input frequency/Prescale divisor combinations:
1.8432 MHz and Prescale = ÷ 3
2.4576 MHz and Prescale = ÷ 4
3.072 MHz and Prescale = ÷ 5
*All baud rates are exact except for those in Table 9.

Table 9 : BAUD RATE % ERROR

Baud Rate	Actual	Percent Error
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.71	0.26%

Modem Control Register

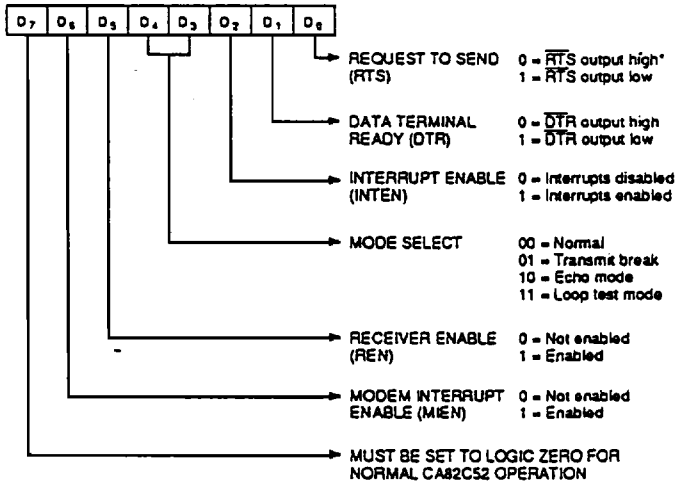
The MCR is a general purpose control register which can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low).

The Operating Mode bits configure the CA82C52 into one of four possible modes. "Normal" configures the CA82C52 for normal full or half duplex communications. "Transmit Break" enables the transmitter to only transmit break

characters (Start, Data and Stop bits are all logic zero). The Echo Mode causes any data that is receivedon the SDI input pin to be re-transmitted on the SDO output pin. Note that this output is a buffered version of the data seen on the SDI input and is not a resychronized output. Also note that normal UART transmission via the Transmitter Register is disabled when operating in the Echo mode (Figure 10). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is disabled from the SDO output pin.

The Receiver Enable (REN) bit gates off the input to the receiver circuitry when in the false state.

Modem Interrupt Enable will permit any change in modem status line inputs ($\overline{CTS}$, $\overline{DSR}$) to cause an interrupt when this bit is enabled. Bit D_7 must always be written to with a logic zero to ensure correct CA82C52 operation.



* See Modem Status Register description for a description of register flag images with respect to output pins.

Figure 9 : MCR

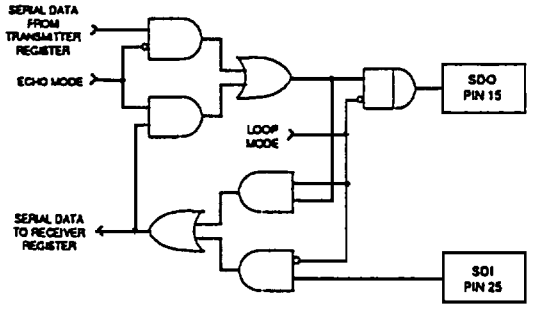


Figure 10 : LOOP and ECHO MODE FUNCTIONALITY

UART Status Register (USR)

The USR provides a single register that the controlling system can examine to determine if errors have occurred or if other status changes in the CA82C52 require attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the CA82C52.

Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that the last character received contained improper stop bits. This could be caused by the absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed parity of the receiver and the calculated parity of the received character data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever a transition is detected on any of the modem input lines ($\overline{CTS}$ or $\overline{DSR}$). A subsequent read of the Modem Status Register will show the state of these two signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the CA82C52 has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the INTEN bit in the MCR register is true.

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Assertion of the TBRE or DR bits do not affect the INTR logic and associated INTR output pin since the CA82C52 has been designed to provide separate requests via the DR and TBRE output pins. If a single interrupt for any status change in the CA82C52 is desired this can be accomplished by *'ORing'* DR, TBRE and INTR together.

Reading the USR clears all of the status bits in the USR register but does not affect associated output pins.

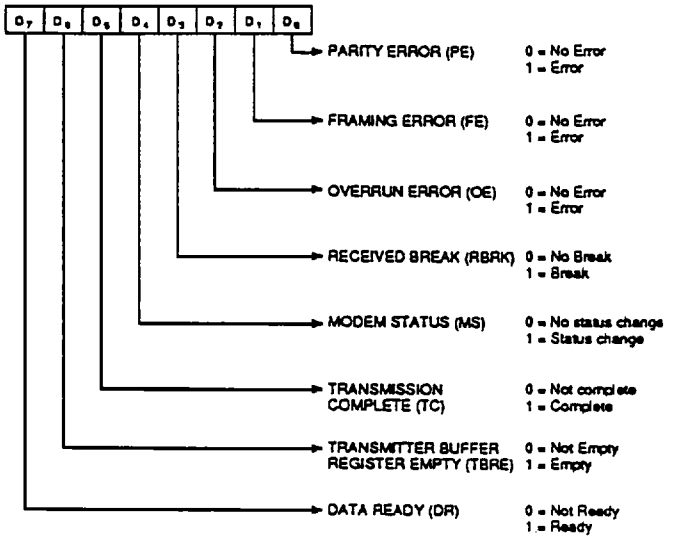


Figure 11 : USR

Modem Status Register (MSR)

The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the CA82C52. Like all of the register images of external pins in the CA82C52, true logic levels are represented by a high (1) signal level. By following this consistent definition, the system software need not be concerned with whether external signals are high or low true. In particular, the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state in any modem input signals will set the Modem Status (MS) bit in the USR register. When this happens, an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Data Set Ready ($\overline{DSR}$) input is a status indicator from the modem to the CA82C52 which indicates that the modem is ready to provide received data to the CA82C52 receiver circuitry.

Clear to Send ($\overline{CTS}$) is both a status and control signal from the modem that tells the CA82C52 that the modem is ready to receive transmit data from the CA82C52 transmitter output (SDO). A high (false) level on this input will inhibit the CA82C52 from beginning transmission and if asserted in the middle of a transmission will only permit the CA82C52 to finish transmission of the current character.

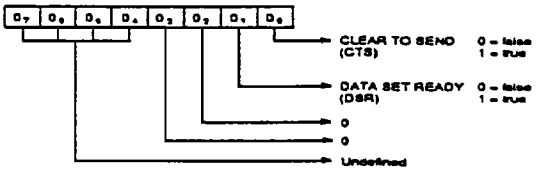


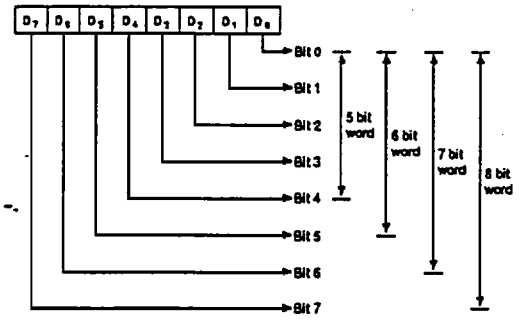
Figure 12 : MSR

Receiver Buffer Register (RBR)

The receiver circuitry in the CA82C52 is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the Least Significant Bit (LSB = D_0). Bit D_0 of a data word is always the first data bit received. The unused bits in a less than 8 bit word, at the parallel interface, are set to a logic zero (0) by the CA82C52.

Received data at the SDI input pin is shifted into the Receiver Register by an internal 1 x clock which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data.

While the Receiver Register is shifting a new character into the CA82C52, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.



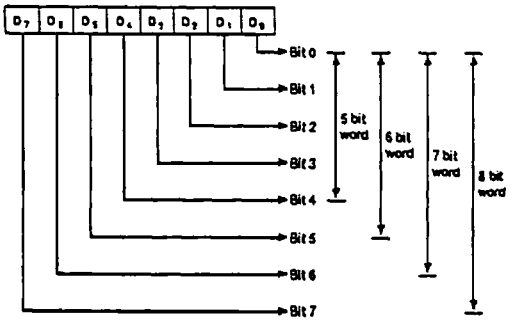
Note: The LSB, Bit 0 is the first serial data bit received.

Figure 13 : RBR

Transmitter Buffer Register (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the data bus (D_0-D_7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter.

Bit 0, which corresponds to D_0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC flag (USR register) indicates when both the TBR and TR are empty.



Note: The LSB, Bit 0 is the first serial data bit transmitted.

Figure 14 : TBR

INTERRUPT STRUCTURE

The CA82C52 has provisions for software masking of interrupts generated for the INTR output pin. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall CA82C52 interrupts respectively. Figure 15 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits. The output pins associated with these status bits are not affected by reading the USR register.

A hardware reset of the CA82C52 sets the TC status bit in the USR. When interrupts are subsequently enabled an interrupt can occur due to the fact that the positive edge detection circuitry in the interrupt logic has detected the setting of the TC bit. If this interrupt is not desired, the USR should be read prior to enabling interrupts. This action resets the positive edge detection circuitry in the interrupt control logic (Figure 15).

Note: For USR and MSR, the setting of status bits is inhibited during status register READ operations. If a status condition is generated during a READ operation, the status bit is not set until the trailing edge of the RD pulse.

If the bit was already set at the time of the READ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the RD pulse instead of being set again.

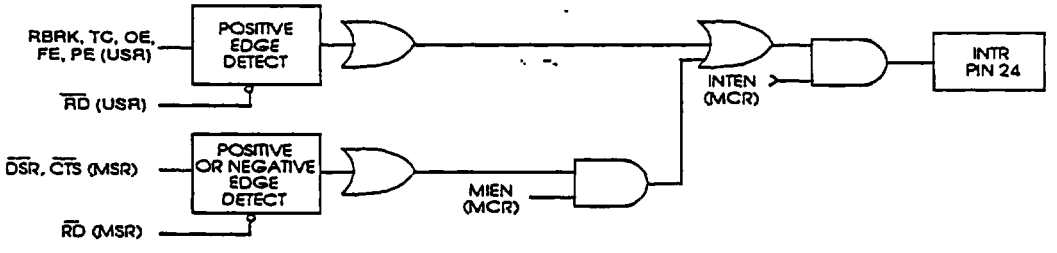


Figure 15 : INTERRUPT STRUCTURE

SOFTWARE RESET

A software reset of the CA82C52 is a useful method for returning to a completely known state without exercising a complete system reset. Such a reset would consist of writing to the UCR, BRSR and MCR registers. The USR an RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

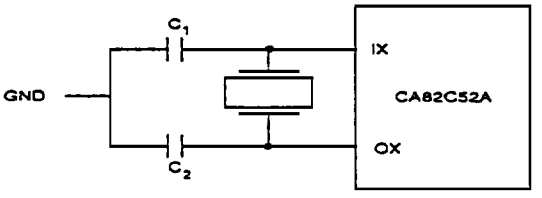
CRYSTAL OPERATION

The CA82C52 crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. To summarize, Table 10 and Figure 16 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source, the IX input is driven and the OX output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

Table 10 : CRYSTAL SPECIFICATIONS

Parameter	Typical Crystal Specs
Frequency	1.0 to 16 MHz
Type of Operation	Parallel resonant, Fundamental mode
Load Capacitance (C_L)	20 or 32 pF (typ.)
R_{series} (Max.)	100 Ω (f = 16 MHz, C_L = 32 pF) 200 Ω (f = 16 MHz, C_L = 20 pF)



$C_1 = C_2 = 20$ pF for $C_L = 20$ pF
$C_1 = C_2 = 47$ pF for $C_L = 32$ pF

* C1 = C2 = 20 pf for C_L = 20 pf
* C1 = C2 = 47 pf for C_L = 32 pf

Figure 16 : TYPICAL CRYSTAL CIRCUIT

APPLICATIONS

The following example (Figure 17) shows the interface for an CA82C52 in an 80C86 system.

Using of the Calmos™ Interrupt Controller (CA82C59A) is optional. It necessary only if an interrupt driven system is desired.

By using the Calmos™ CA82C84A clock generator, the system can be built with a single crystal providing both the processor clock and the clock for the CA82C52. The CA82C52 has special divider circuitry which is designed to supply industry standard baud rates with a 2.4576 MHz input frequency. Using a 15 MHz crystal as shown, results in less than a 2% frequency error which is adequate for many applications. For more precise baud rate requirements, a 14.7456 MHz crystal will drive the 80C86 at 4.9 MHz and provide the 82C52 with the standard baud rate input frequency of 2.4576 MHz. If baud rates above 156 Kbaud are desired, the OSC output can be used instead of the PCLK (÷6) output for asynchronous baud rates up to 1 Mbaud.

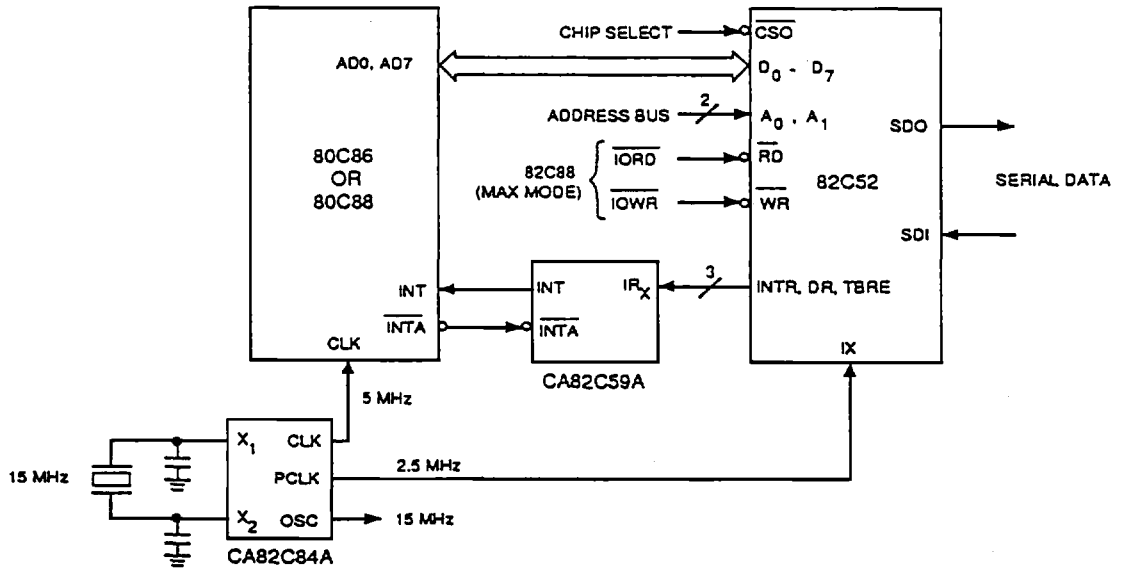


Figure 17 : 80C86/CA82C52 INTERFACE

MECHANICALS

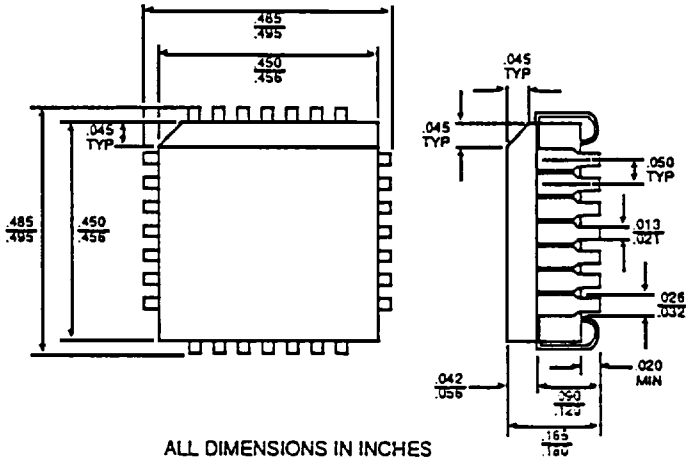


Figure 18 : 28 - LEAD PLCC PACKAGING

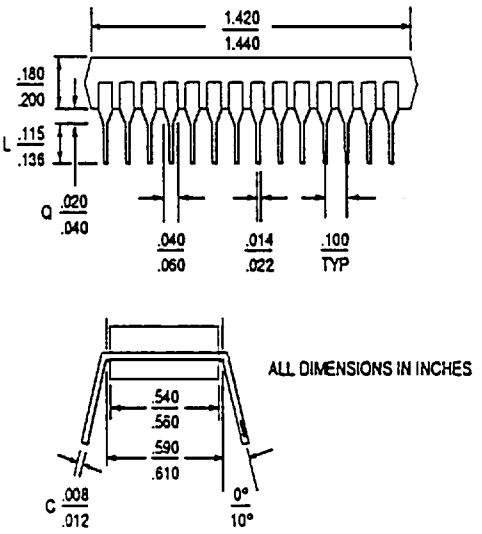
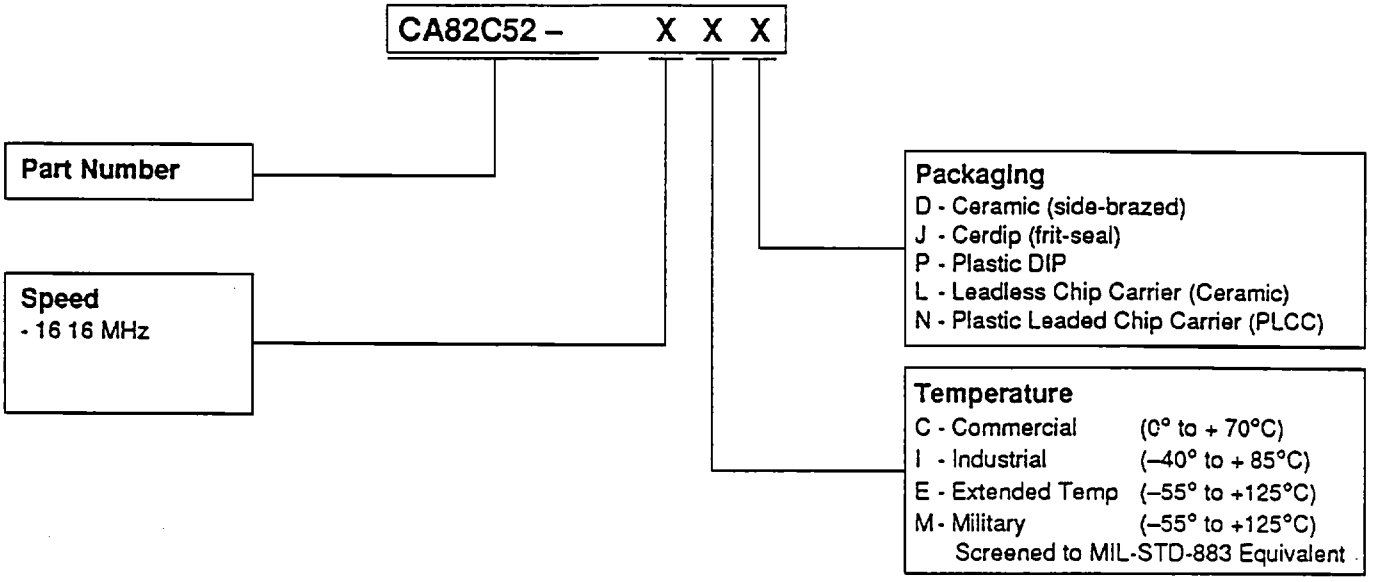


Figure 19 : 28 - PIN PDIP PACKAGING

ORDERING INFORMATION and PRODUCT CODE



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