



Integrated Device Technology, Inc.

**CMOS STATIC RAM  
64K (8K x 8-BIT)**

**IDT 7164S  
IDT 7164L**

T-46-23-12

**FEATURES:**

- Optimized for fast RISC processors including the IDT79R3000
- High-speed address/chip select access time
  - Military: 25/30/35/45/55/70/85/100/120/150/200ns (max.)
  - Commercial: 19/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7164S
    - Active: 300mW (typ.)
    - Standby: 100µW (typ.)
  - IDT7164L
    - Active: 250mW (typ.)
    - Standby: 30µW (typ.)
- Battery backup operation—2V data retention voltage (L Version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Available in standard 28-pin DIP (600 mil), 28-pin THINDIP (300 mil), 28-pin LCC, 32-pin LCC and PLCC and 28-pin SOIC
- Pin-compatible with standard 64K static RAM and EPROM
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-85525 is listed on this function. Refer to Section 2/page 2-2.

**DESCRIPTION:**

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. Timing parameters have been specified to meet the demands of the fastest IDT79R3000 RISC processors.

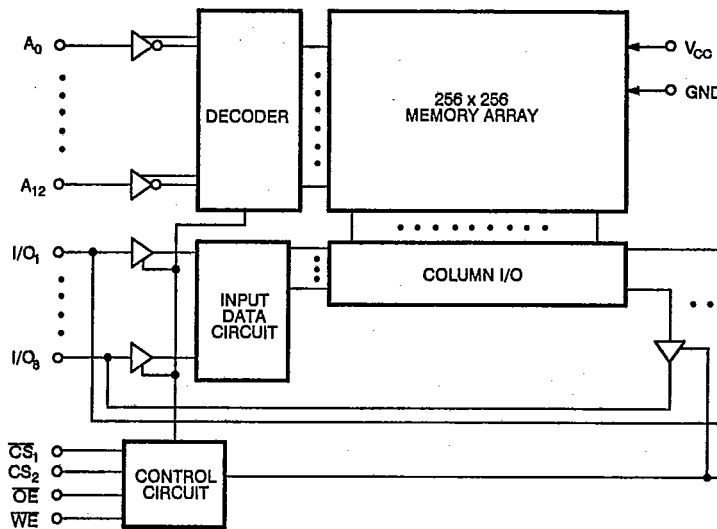
Address access times as fast as 19ns are available with typical power consumption of only 250mW. The circuit also offers a reduced power standby mode. When CS<sub>1</sub> goes high or CS<sub>2</sub> goes low, the circuit will automatically go to, and remain in, a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30µW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW operating off a 2V battery.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin, 300 mil THINDIP; 28-pin, 600 mil DIP; 32-pin LCC and PLCC and 28-pin LCC and SOIC (gull-wing and J-bend), providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

**FUNCTIONAL BLOCK DIAGRAM**



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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**JANUARY 1989**

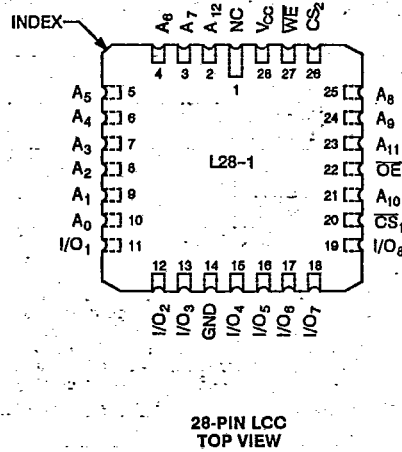
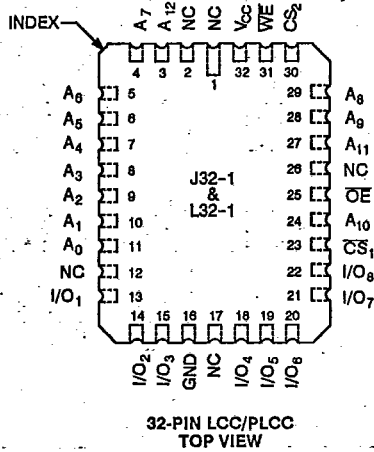
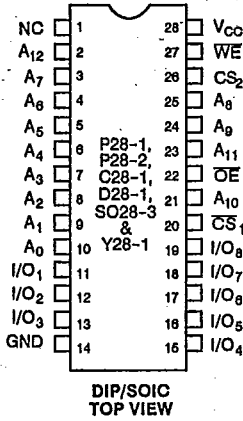
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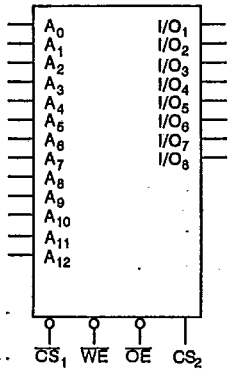
DSC-1002/2

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PIN CONFIGURATIONS



LOGIC SYMBOL



PIN NAMES

A <sub>0</sub> -A <sub>12</sub>	Address	WE	Write Enable
I/O <sub>1</sub> - I/O <sub>8</sub>	Data Input/Output	OE	Output Enable
CS <sub>1</sub>	Chip Select	GND	Ground
CS <sub>2</sub>	Chip Select	V <sub>CC</sub>	Power

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**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	-	0.8	V

**NOTE:**

1. V<sub>IL</sub> (min.) = -3.0V for pulse width less than 20ns.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

GRADE	AMBIENT TEMPERATURE	GND	V <sub>CC</sub>
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

**DC ELECTRICAL CHARACTERISTICS**

V<sub>CC</sub> = 5.0V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7164S			IDT7164L			UNIT
			MIN.	TYP. <sup>(1)</sup>	MAX.	MIN.	TYP. <sup>(1)</sup>	MAX.	
I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	MIL. COM'L	-	10	-	-	5	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., CS <sub>1</sub> = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>	MIL. COM'L	-	10	-	-	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 10mA, V <sub>CC</sub> = Min.	-	-	0.5	-	-	0.5	V
		I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.	-	-	0.4	-	-	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.	2.4	-	-	2.4	-	-	V

**NOTE:**

1. Typical limits are at V<sub>CC</sub> = 5.0V, +25°C ambient.

**DC ELECTRICAL CHARACTERISTICS <sup>(1)</sup>**

V<sub>CC</sub> = 5.0V ± 10%, V<sub>LO</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

SYMBOL	PARAMETER	POWER	7164S19/20	7164S25 <sup>(4)</sup>	7164S30	7164S35	7164S45	7164S55	7164S70	7164S85 <sup>(2)</sup>	UNIT
			7164L20	7164L25 <sup>(4)</sup>	7164L30	7164L35	7164L45	7164L55	7164L70	7164L85 <sup>(2)</sup>	
I <sub>CC1</sub>	Operating Power Supply Current, CS <sub>1</sub> = V <sub>IL</sub> , Outputs Open, CS <sub>2</sub> = V <sub>IH</sub> , V <sub>CC</sub> = Max., f = 0 <sup>(3)</sup>	S	100	90 110	90 100	90 100	90 100	- 100	- 100	- 100	mA
		L	90	80 100	80 90	80 90	80 90	- 90	- 90	- 90	
I <sub>CC2</sub>	Dynamic Operating Current, CS <sub>1</sub> = V <sub>IL</sub> , Outputs Open, CS <sub>2</sub> = V <sub>IH</sub> , V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(3)</sup>	S	190	170 190	160 170	150 160	150 160	- 160	- 160	- 160	mA
		L	170	150 170	140 150	130 140	120 130	- 125	- 120	- 120	
I <sub>SB</sub>	Standby Power Supply Current (TTL Level), f = f <sub>MAX</sub> <sup>(3)</sup> , CS <sub>1</sub> ≥ V <sub>IH</sub> , or CS <sub>2</sub> ≥ V <sub>IL</sub> , V <sub>CC</sub> = Max., Outputs Open	S	20	20 20	20 20	20 20	20 20	- 20	- 20	- 20	mA
		L	3	3 5	3 5	3 5	3 5	- 5	- 5	- 5	
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS Level) f = 0 <sup>(3)</sup> 1. CS <sub>1</sub> ≥ V <sub>HC</sub> and CS <sub>2</sub> ≥ V <sub>HC</sub> 2. CS <sub>2</sub> ≤ V <sub>LC</sub> , V <sub>CC</sub> = Max.	S	15	15 20	15 20	15 20	15 20	- 20	- 20	- 20	mA
		L	0.2	0.2 1.0	0.2 1.0	0.2 1.0	0.2 1.0	- 1.0	- 1.0	- 1.0	

**NOTES:**

- All values are maximum guaranteed values.
- Also available: 100, 120, 150 and 200ns military devices.
- At f = f<sub>MAX</sub> address and data inputs are cycling at the maximum frequency of read cycles of 1/t<sub>RC</sub>. f = 0 means no input lines change.
- Military values are preliminary only.

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DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

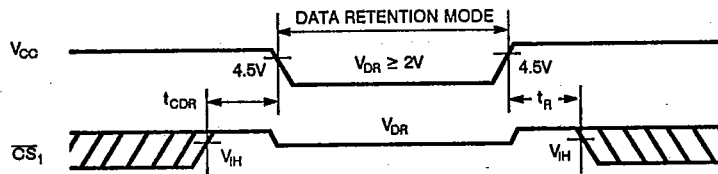
(L Version Only)  $V_{LO} = 0.2V$ ,  $V_{HO} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)		MAX.		UNIT	
				$V_{CC} @ 2.0V$	$V_{CC} @ 3.0V$	$V_{CC} @ 2.0V$	$V_{CC} @ 3.0V$		
$V_{DR}$	$V_{CC}$ for Data Retention	-	2.0	-	-	-	-	V	
$I_{CCDR}$	Data Retention Current	1. $\overline{CS}_1 \geq V_{HC}$ , $CS_2 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$	MIL.	-	10	15	200	300	$\mu A$
			COM'L.	-	10	15	60	90	
$t_{CDR}$	Chip Deselect to Data Retention Time		0	-	-	-	-	ns	
$t_R$	Operation Recovery Time		$t_{RO}^{(2)}$	-	-	-	-	ns	
$ I_{IL} ^{(3)}$	Input Leakage Current		-	-	-	2	-	$\mu A$	

NOTES:

- $T_A = +25^\circ C$
- $t_{RC}$  = Read Cycle Time
- This parameter is guaranteed but not tested.

LOW  $V_{CC}$  DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

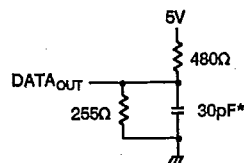


Figure 1. Output Load

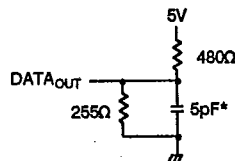


Figure 2. Output Load  
(for  $t_{CLZ1,2}$ ,  $t_{OLZ}$ ,  $t_{CHZ1,2}$ ,  $t_{OHZ}$ ,  $t_{OW}$ ,  $t_{WHZ}$ )

\* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5V ±10%, All Temperature Ranges)

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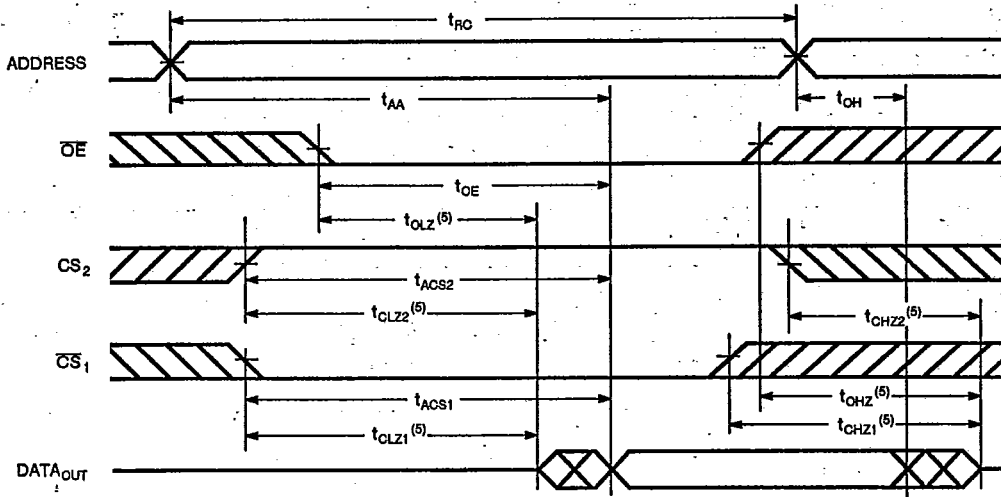
SYMBOL	PARAMETER	7164S19/20 <sup>(1)</sup>	7164S25	7164S30	7164S35	7164S45	7164S55 <sup>(2)</sup>	7164S70 <sup>(2)</sup>	7164S85 <sup>(2)</sup>	UNIT	
		7164L20 <sup>(1)</sup>	7164L25	7164L30	7164L35	7164L45	7164L55 <sup>(2)</sup>	7164L70 <sup>(2)</sup>	7164L85 <sup>(2)</sup>		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
t <sub>RO</sub>	Read Cycle Time	20	25	30	35	45	55	70	85	ns	
t <sub>AA</sub>	Address Access Time	19/20	25	29	35	45	55	70	85	ns	
t <sub>ACS1</sub>	Chip Select-1 Access Time <sup>(3)</sup>	20	25	30	35	45	55	70	85	ns	
t <sub>ACS2</sub>	Chip Select-2 Access Time <sup>(3)</sup>	25	30	35	40	45	55	70	85	ns	
t <sub>CLZ1,2</sub>	Chip Select-1, 2 to Output in Low Z <sup>(4)</sup>	5	5	5	5	5	5	5	5	ns	
t <sub>OE</sub>	Output Enable to Output Valid	10	12	15	18	25	30	35	40	ns	
t <sub>OLZ</sub>	Output Enable to Output in Low Z <sup>(4)</sup>	3	3	3	3	3	3	3	3	ns	
t <sub>CHZ1,2</sub>	Chip Select-1, 2 to Output in High Z <sup>(4)</sup>	9	13	13	15	20	25	30	35	ns	
t <sub>OHZ</sub>	Output Disable to Output in High Z <sup>(4)</sup>	8	10	12	15	20	25	30	35	ns	
t <sub>OH</sub>	Output Hold from Address Change	5	5	5	5	5	5	5	5	ns	
t <sub>PU</sub>	Chip Select to Power Up Time <sup>(4)</sup>	0	0	0	0	0	0	0	0	ns	
t <sub>PD</sub>	Chip Select to Power Down Time <sup>(4)</sup>	20	25	30	35	45	55	70	85	ns	

NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter guaranteed but not tested.

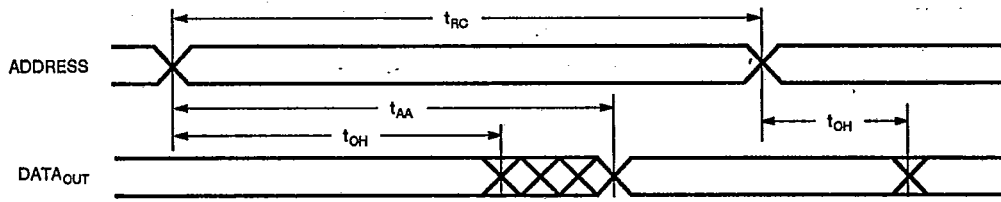
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TIMING WAVEFORM OF READ CYCLE NO. 1 <sup>(1)</sup>

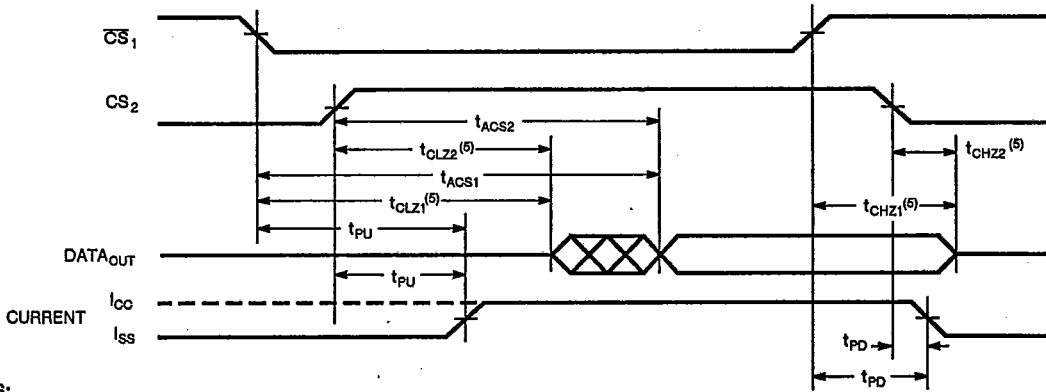


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TIMING WAVEFORM OF READ CYCLE NO. 2 <sup>(1, 2, 4)</sup>



TIMING WAVEFORM OF READ CYCLE NO. 3 <sup>(1, 2, 4)</sup>



NOTES:

1. WE is High for Read Cycle.
2. Device is continuously selected, CS<sub>1</sub> = V<sub>IL</sub>, CS<sub>2</sub> = V<sub>IH</sub>.
3. Address valid prior to or coincident with CS<sub>1</sub> transition low and CS<sub>2</sub> transition high.
4. OE = V<sub>L</sub>.
5. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5V ±10%, All Temperature Ranges)

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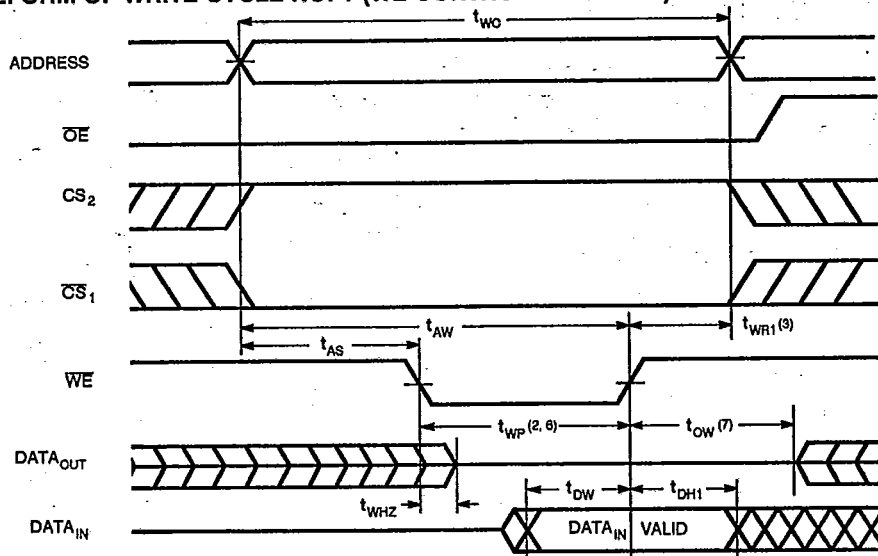
SYMBOL	PARAMETER	7164S19/20 <sup>(1)</sup>	7164S25	7164S30	7164S35	7164S45	7164S55 <sup>(2)</sup>	7164S70 <sup>(2)</sup>	7164S85 <sup>(2)</sup>	UNIT
		7164L20 <sup>(1)</sup>	7164L25	7164L30	7164L35	7164L45	7164L55 <sup>(2)</sup>	7164L70 <sup>(2)</sup>	7164L85 <sup>(2)</sup>	
		MIN. MAX.	MIN. MAX.	MIN. MAX.	MIN. MAX.	MIN. MAX.	MIN. MAX.	MIN. MAX.	MIN. MAX.	
t <sub>WC</sub>	Write Cycle Time	20 -	25 -	30 -	35 -	45 -	55 -	70 -	85 -	ns
t <sub>CW1,2</sub>	Chip Select to End of Write	15 -	18 -	22 -	25 -	33 -	50 -	60 -	75 -	ns
t <sub>AW</sub>	Address Valid to End of Write	15 -	18 -	22 -	25 -	33 -	50 -	60 -	75 -	ns
t <sub>AS</sub>	Address Set-up Time	0 -	0 -	0 -	0 -	0 -	0 -	0 -	0 -	ns
t <sub>WP</sub>	Write Pulse Width	15 -	21 -	23 -	25 -	25 -	50 -	60 -	75 -	ns
t <sub>WR1</sub>	Write Recovery Time (CS <sub>1</sub> , WE)	0 -	0 -	0 -	0 -	0 -	0 -	0 -	0 -	ns
t <sub>WR2</sub>	Write Recovery Time (CS <sub>2</sub> )	5 -	5 -	5 -	5 -	5 -	5 -	5 -	5 -	ns
t <sub>WHZ</sub>	Write Enable to Output High Z <sup>(3)</sup>	5 -	10 -	12 -	14 -	18 -	25 -	30 -	35 -	ns
t <sub>DW</sub>	Data to Write Time Overlap	10 -	13 -	13 -	15 -	20 -	25 -	30 -	35 -	ns
t <sub>DH1</sub>	Data Hold from Write Time (CS <sub>1</sub> , WE)	0 -	0 -	0 -	0 -	0 -	0 -	0 -	0 -	ns
t <sub>DH2</sub>	Data Hold from Write Time (CS <sub>2</sub> )	5 -	5 -	5 -	5 -	5 -	5 -	5 -	5 -	ns
t <sub>OW</sub>	Output Active from End of Write <sup>(3)</sup>	5 -	5 -	5 -	5 -	5 -	5 -	5 -	5 -	ns

NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. This parameter guaranteed but not tested.

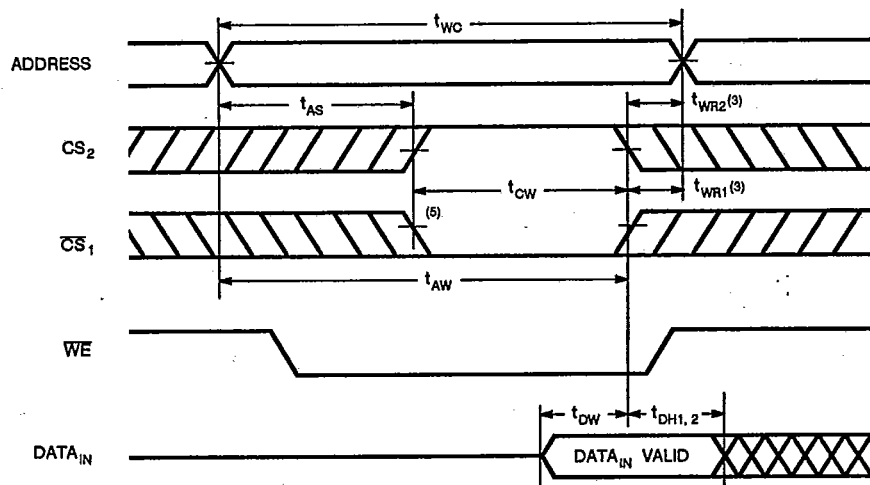
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1)</sup>

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TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}_1$  CONTROLLED TIMING)<sup>(1)</sup>



NOTES:

1.  $\overline{WE}$  must be high during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}_1$  and a high  $CS_2$ .
3.  $t_{WR1,2}$  is measured from the earlier of  $\overline{CS}_1$  or  $\overline{WE}$  going high or  $CS_2$  going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the  $\overline{CS}_1$  low transition or  $CS_2$  high transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
6. If  $\overline{OE}$  is low during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{WHZ} + t_{DW}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is high during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .
7.  $DATA_{OUT}$  is the same phase of write data of this write cycle.
8. If  $\overline{CS}_1$  is low and  $CS_2$  is high during this period, I/O pins are in the output state. Data input signals must not be applied.
9. Transition is measured  $\pm 200mV$  from steady state.



IDT7164S/IDT7164L CMOS STATIC RAM 64K (8K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

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**CAPACITANCE** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

SYMBOL	PARAMETER <sup>(1)</sup>	CONDITIONS	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	8	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	8	pF

**NOTE:**

- This parameter is determined by device characterization but is not production tested.

**TRUTH TABLE**

WE	$\overline{CS}_1$	$CS_2$	$\overline{OE}$	I/O	MODE
X	H	X	X	HIGH Z	Standby ( $I_{SB}$ )
X	X	L	X	HIGH Z	Standby ( $I_{SB}$ )
X	$V_{HC}$	$V_{HC}$ or $V_{LC}$	X	HIGH Z	Standby ( $I_{SB}$ )
X	X	$V_{LC}$	X	HIGH Z	Standby ( $I_{SB}$ )
H	L	H	H	HIGH Z	Output disable
H	L	H	L	$D_{OUT}$	Read
L	L	H	X	$D_{IN}$	Write

**NOTE:**

- $CS_2$  will power-down  $\overline{CS}_1$ , but  $\overline{CS}_1$  will not power-down  $CS_2$ .

**ORDERING INFORMATION**

