MAXIM

Precision Operational Amplifier

General Description

The LT1001 offers significant specification improvements over earlier precision operational amplifiers. Particular attention has been paid to the optimization of key parameters such as input offset voltage, common-mode rejection, and power supply rejection. In addition, the high-performance LT1001C commercial temperature device provides considerable cost savings when compared to equivalent grades of competing precision amplifiers.

The input offset voltage of all units is less than 60μV, allowing the premium Military device, the LT1001AM, to be specified at 15μV max. Power dissipation is close to half that of the industry-standard OP-07 precision op amp without sacrificing noise or speed performance. A useful by-product of lower dissipation is decreased warm-up drift.

Applications

- Thermocouple Amplifiers
- Low-Level Signal Processing
- Strain Gauge Amplifiers
- High-Accuracy Data Acquisition

Features

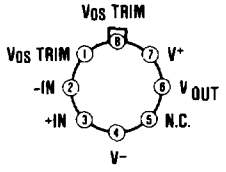
- **Guaranteed Low Offset Voltage**
  - LT1001AM ..... 15μV max
  - LT1001C ..... 60μV max
- **Guaranteed Low Drift**
  - LT1001AM ..... 0.6μV/°C max
  - LT1001C ..... 1.0μV/°C max
- **Guaranteed Low Bias Current**
  - LT1001AM ..... 2nA max
  - LT1001C ..... 4nA max
- **Guaranteed CMRR**
  - LT1001AM ..... 114dB min
  - LT1001C ..... 110dB min
- **Guaranteed PSRR**
  - LT1001AM ..... 110dB min
  - LT1001C ..... 106dB min
- **Low Power Dissipation**
  - LT1001AM ..... 75mW max
  - LT1001C ..... 80mW max
- **Low Noise: 0.3μV_{p-p}**

Ordering Information

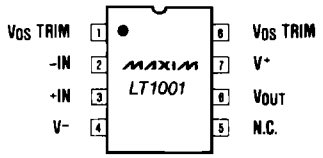
PART	TEMP. RANGE	PACKAGE*
LT1001AMH	-55°C to +125°C	8 Lead TO-99
LT1001MH	-55°C to +125°C	8 Lead TO-99
LT1001ACH	0°C to +70°C	8 Lead TO-99
LT1001CH	0°C to +70°C	8 Lead TO-99
LT1001ACN8	0°C to +70°C	8 Lead Plastic Dip
LT1001CN8	0°C to +70°C	8 Lead Plastic Dip
LT1001AMJ8	-55°C to +125°C	8 Lead Hermetic Dip
LT1001MJ8	-55°C to +125°C	8 Lead Hermetic Dip
LT1001ACJ8	0°C to +70°C	8 Lead Hermetic Dip
LT1001CJ8	0°C to +70°C	8 Lead Hermetic Dip
LT1001ACS8	0°C to +70°C	8 Lead Small Outline
LT1001CS8	0°C to +70°C	8 Lead Small Outline

Pin Configuration

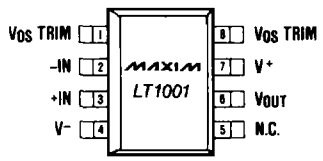
Top View



8 Lead TO-99

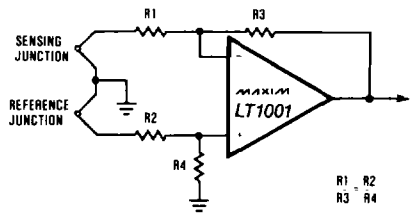


8 Lead Dip



8 Lead Small Outline

Typical Operating Circuit



High-Stability
Thermocouple Amplifier

Precision Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... ±22V
Internal Power Dissipation 500mW
TO-99(H) — derate at 7.1mW/°C above +80°C
Hermetic Dip(J) — derate at 6.7mW/°C above +75°C
Plastic Dip(P) — derate at 5.6mW/°C above +36°C
Small Outline(S) — derate at 5mW/°C above +55°C
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
LT1001AMH, LT1001AMJ8,
LT1001MH, and LT1001MJ8 ..... -55°C to +125°C
All Other Parts ..... 0°C to +70°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Duration of Output Short Circuit ..... Indefinite
Junction Temperature (T_J) ..... -65°C to +160°C

Note 1: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1001AM LT1001AC			LT1001M LT1001C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 2) LT1001AM LT1001AC		7 10	15 25		18	60	μV
Long Term Input Offset Voltage Stability	V_{OS}/Time	(Note 3)		0.2	1.0		0.3	1.5	μV/ Month
Input Offset Current	I_{OS}			0.3	2.0		0.4	3.8	nA
Input Bias Current	I_B			±0.5	±2.0		±0.7	±4.0	nA
Input Noise Voltage	$e_{N\ P-P}$	0.1Hz to 10Hz (Note 4)		0.3	0.6		0.3	0.6	μV_{P-P}
Input Noise Voltage Density	e_N	f_O = 10Hz (Note 4) f_O = 100Hz (Note 4) f_O = 1000Hz (Note 4)		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.0 9.8	18.0 13.0 11.0	nV/$\sqrt{Hz}$
Input Resistance Differential-Mode	R_{IN}	(Note 5)	30	100		15	80		MΩ
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	114	126		110	126		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	110	123		106	123		dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±12V $R_L \geq 1k\Omega$, V_O = ±10V	450 300	800 500		400 250	800 500		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±13.0 ±12.0	±14.0 ±13.5		±13.0 ±12.0	±14.0 ±13.5		V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/μS
Closed-Loop Bandwidth	BW	A_{VCL} = +1V (Note 4)	0.4	0.8		0.4	0.8		MHz
Power Consumption	P_D	V_S = ±15V, No Load V_S = ±3V, No Load		46 4	75 6		48 4	80 8	mW

Note 2: LT1001A grade V_{OS} is measured one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
Note 3: Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV. Parameter is sample tested
Note 4: Sample tested.
Note 5: Guaranteed by design.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1001AM			LT1001M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 6)		30	60		45	160	µV
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}			0.2	0.6		0.3	1.0	µV/°C
Input Offset Current	I_{OS}			0.8	4.0		1.2	7.6	nA
Input Bias Current	I_B			±1.0	±4.0		±1.5	±8.0	nA
Input Voltage Range	IVR		±13	±14		±13	14		V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±13V	110	122		106	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	104	117		100	117		dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	300	700		200	700		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.5	±13.5		±12.5	±13.5		V
Power Dissipation	P_D	No Load		55	90		60	100	mW

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1001AC			LT1001C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 6)		20	60		30	110	µV
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}			0.2	0.6		0.3	1.0	µV/°C
Input Offset Current	I_{OS}			0.5	3.5		0.6	5.3	nA
Input Bias Current	I_B			±0.7	±3.5		±1.0	±5.5	nA
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	110	124		106	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	106	120		103	120		dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	350	750		250	750		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.5	±13.8		±12.5	±13.8		V
Power Dissipation	P_D	No Load		50	85		55	90	mW

Note 6: LT1001A grade Offset Voltage is measured one minute after application of power. For all other grades V_{OS} is measured 0.5 seconds after power on.

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Applications Information

The LT1001 series devices are pin-compatible with the OP-07, OP-05, 725, 108A or 101A amplifiers. The LT1001 amplifiers can be used to upgrade older designs using these devices with or without removal of external frequency compensation or nulling components. The LT1001 can also be used in 741, LF156 or OP-15 applications provided the nulling circuitry is removed.

The LT1001 is specified over a wide supply voltage range from ±3V to ±18V. Operation with lower supplies is possible down to ±1.2V (two Ni-Cad batteries), however, at this level the device is stable only in closed-loop gains of +2 and above (or inverting gain of one or higher). Unless proper care is exercised, thermocouple effects, caused by temperature gradients across dissimilar metals at the input terminals connections, can exceed the inherent offset voltage drift of the amplifier. Air currents over the device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Offset Voltage Adjustment

The input offset voltage of the LT1001, and its temperature drift, are minimized by zener-zap trimming at the wafer level. If further nulling of V_{OS} is required, this can be performed using a 10k or 20k potentiometer with no degradation of V_{OS} drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300)\mu V/°C$, e.g. if V_{OS} is adjusted to 300uV, the change in drift will be 1uV/°C. The adjustment range with a 10k or 20k potentiometer is approximately ±2.5mV. If less adjustment range is needed, the sensitivity and resolution of the offset nulling can be improved by using a potentiometer of lower ohmic value in conjunction with fixed resistors.

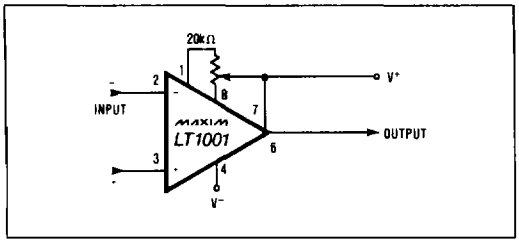
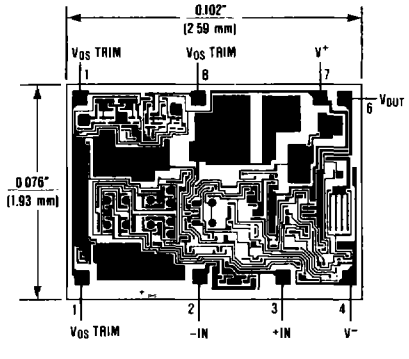


Figure 1. Optional Offset Nulling Circuit.

Chip Topography



Note: Substrate is connected to V-