C9915

Low EMI Clock Generator for Intel® 133-MHz/2-DIMM Chipset Systems

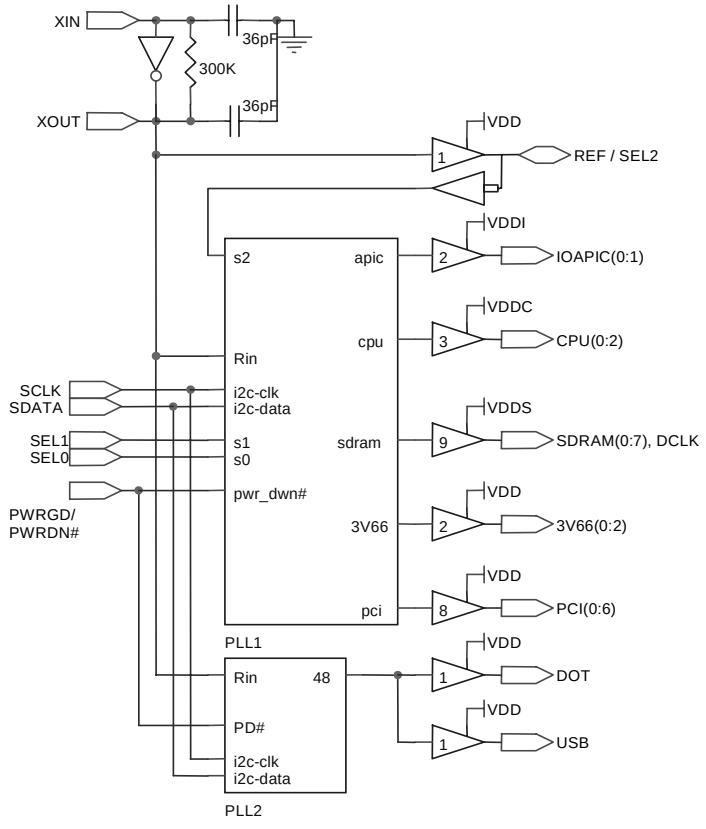
Features

- **Meets Intel® 133-MHz/SDRAM chipset specification**
- **Three copies of CPU clock (CPU[0:1] and CPU2_ITP)**
- **Nine copies of SDRAM clock (SDRAM[0:7] and DCLK)**
- **Seven copies of PCI clock**
- **Three copies of 3V66 clock**
- **Two copies of IOAPIC clock**
- **One REF clock**
- **One USB clock (non-SSC)**
- **One DOT clock (non-SSC)**
- **Cypress Spread Spectrum for best electromagnetic interference (EMI) reduction**
- **SMBus support with read back**
- **56-pin SSOP/TSSOP package**

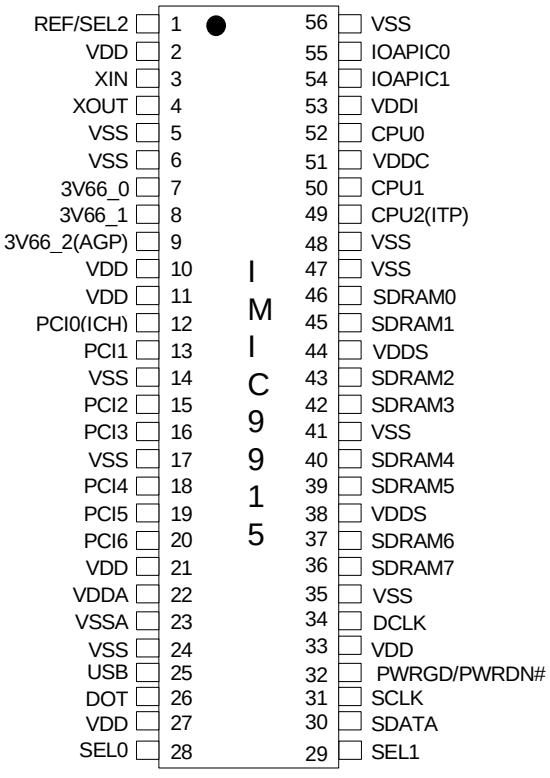
Table 1. Frequency Table (MHz) [1]

SEL2	SEL1	SEL0	CPU	SDRAM	PCI
X	0	0	Three-State	X	0
X	0	1	Test Mode	X	0
0	1	0	66.6 MHz	100 MHz[2]	33.3
0	1	1	100 MHz	100 MHz[2]	33.3
1	1	0	133.3 MHz	133.3 MHz	33.3
1	1	1	133.3 MHz	100 MHz[2]	33.3

Block Diagram



Pin Configuration



Notes:

1. The following clocks remain fixed frequencies except in Test Mode: 3V66 = 66.6 MHz, USB/DOT = 48 MHz, REF = 14.318 MHz, and IOAPIC = 33.3 MHz.
2. SMBus programmable to 133 MHz, Byte 3, Bit 0.

Pin Description[3]

Pin	Name	PWR	I/O	Description
1	SEL2/REF	VDD	I/O	**This is a bidirectional pin**. At power-up, it is an input pin Sel2 for selecting the CPU/SDRAM frequencies (see *Table 1*). When the power reaches the rail, the state of Sel2 is latched, and this pin becomes REF, a buffer output of the signal applied at Xin, typically 14.318 MHz. This pin has an Internal pull-down. Typical 50 KΩ (range 20 KΩ to 70 KΩ).
3	XIN	VDD	I	**On-chip Reference Oscillator Input Pin**. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
4	XOUT	VDD	O	**On-chip Reference Oscillator Pin**. Drives an external parallel resonant crystal. When an externally generated reference signal is used at Xin, this pin remains unconnected.
12,13,15, 16,18,19, 20	PCI0_ICH PCI(1..6)	VDD	O	**3.3V PCI Clock Outputs**. They are synchronous to CPU clocks. See *Figure 11*).
7, 8, 9	3V66(0:2)	VDD	O	**3.3V Fixed 66.6 MHz Clock Outputs**. See *Figure 11*.
25	USB	VDD	O	3.3V Fixed 48 MHz clock outputs.
26	DOT	VDD	O	3.3V Fixed 48 MHz clock outputs.
28, 29	SEL(0,1)	VDD	I	**3.3V LVTTL Inputs for Logic Selection**. This pin has an internal pull-up. Typical 250 KΩ (range 200 KΩ to 500 KΩ)
30	SDATA	VDD	I/O	**Serial Data Input Pin**. Conforms to the SMBus specification of a Slave Receive/Transmit device. This pin is an input when receiving data. It is an open drain output when acknowledging or transmitting data. See SMBus function description.
31	SCLK	VDD	I	**Serial Clock Input Pin**. Conforms to the SMBus specification.
32	PWRGD/PWRDN#	VDD	I	**This is a Dual Function Pin**. During power-up, it serves as a power-down control. After PWRGD has gone HIGH once, whenever pin 32 goes LOW, the device will go into power-down mode.
34	DCLK	VDD	O	**3.3V SDRAM Feedback Clock**. See *Table 1* for frequency selection. See *Figure 11* for timing relationship.
36,37,39,40, 42,43,45, 46	SDRAM(7..0)	VDDS	O	**3.3V SDRAM DIMM Clocks**. See *Table 1* for frequency selection. See *Figure 11* for timing relationship.
49, 50, 52	CPU(2)_ITP,CPU(1,0)	VDDC	O	**2.5V Host Clock Outputs**. See *Table 1* for frequency selection.
54, 55	IOAPIC(1,0)	VDDI	O	**2.5V IOAPIC Clock Outputs**. See *Figure 11* for timing relationship.
2,10, 11, 21, 27, 33	VDD			**3.3V Common Power Supply**
22	VDDA			**Analog Circuitry 3.3V Power Supply**
23	VSSA			**Analog Circuitry Power Supply Ground Pins**
51, 53	VDDC, VDDI			**2.5V Power Supply**
5, 6,14, 17, 24, 35, 41, 47, 48, 56	VSS			**Common Ground Pins**
38, 44	VDDS			**3.3V Power Support for SDRAM Clock Output Drivers**

Note:

3. A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Two-Wire SMBus Control Interface

The two-wire control interface implements a Read/Write slave-only interface, according to SMBus specification. (See *Figure 1* and *Figure 2,* below). The device can be read back by using standard SMBus command bytes. Subaddressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The two-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A HIGH-to-LOW transition on SDATA while SCLK is HIGH is used to indicate the start of a data transfer cycle. A LOW-to-HIGH transition on SDATA while SCLK is HIGH indicates the end of a data transfer cycle. Data is always sent as complete eight-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is an eight-bit address. The LSB address Byte = 0 in write mode.

The device will respond to transfers of 10 bytes (max) of data. The device will generate an acknowledge (LOW) signal on the SDATA wire following reception of each byte. Data is transferred MSB first at a max. rate of 100kbits/S. This device will also respond to a D3 address which sets it in a read mode. It will not respond to any other control interface conditions, and previously set control registers are retained.

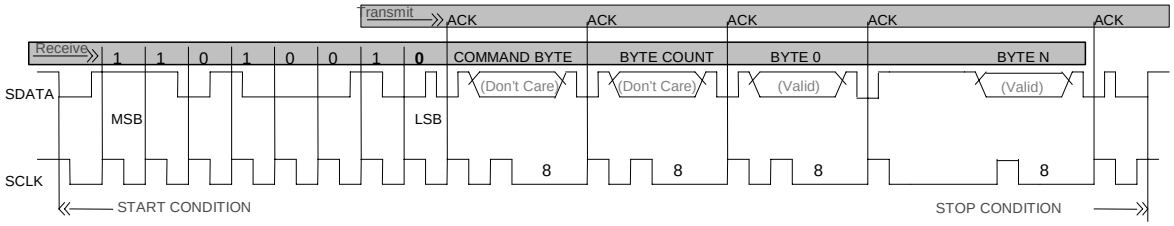


Figure 1. SMBus Communication Waveform (Write)

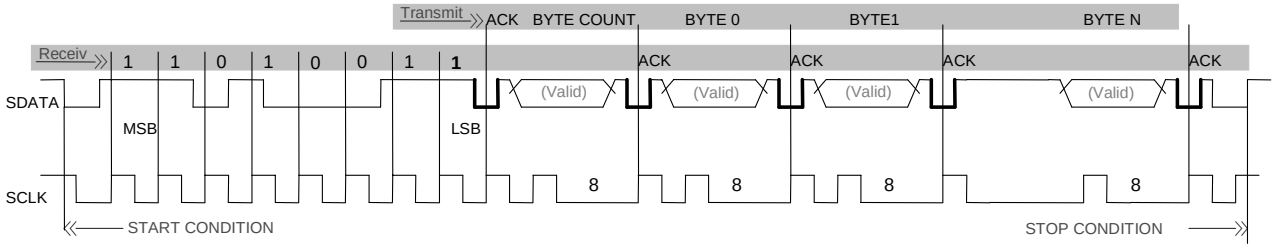


Figure 2. SMBus Communication Waveform (Read)

Serial Control Registers

Byte 4: CPU Clock Register

Bit	@Pup	Pin#	Name	Description
7	H/W Setting	14	FS3	For selecting frequencies in *Table 1*
6	H/W Setting	4	FS2	For selecting frequencies in *Table 1*
5	H/W Setting	3	FS1	For selecting frequencies in *Table 1*
4	H/W Setting	2	FS0	For selecting frequencies in *Table 1*
3	0			0 = HW, 1 = SW Frequency Selection
2	H/W Setting	15	FS4	For selecting frequencies in *Table 1*
1	1		SSCG	Spread Spectrum Enable. 0 = Spread Off, 1 = Spread On This is a Read and Write control bit.
0	0			0 = running; 1= three-state all outputs

Byte 5: CPU Clock Register (All bits are Read-only)

Bit	@Pup	Pin#	Name	Description
7	0			Reserved
6	0			Reserved
5	X	26	MULTO	MULT0 (pin 26) value. This bit is Read-only.
4	X	15	FS4	FS4 read back. This bit is Read-only.

Byte 5: CPU Clock Register (All bits are Read-only) (continued)

Bit	@Pup	Pin#	Name	Description
3	X	14	FS3	FS3 read back. This bit is Read-only.
2	X	4	FS2	FS2 read back. This bit is Read-only.
1	X	3	FS1	FS1 read back. This bit is Read-only.
0	X	2	FS0	FS0 read back. This bit is Read-only.

Byte 6: CPU Clock Register

Bit	@Pup	Pin#	Name	Description
7	0			Function Test Bit, always program to 0.
6	0			Reserved.
5	0	14	PCI_F0	PCI_STP# control of PCI_F0. 0 = Free Running, 1 = Stopped when PCI_STP# is LOW.
4	0	15	PCI_F1	PCI_STP# control of PCI_F1. 0 = Free Running, 1 = Stopped when PCI_STP# is LOW.
3	1	40,39	CPU0T/C	Controls CPU0T and CPU0C functionality when CPU_STP# is asserted LOW 0 = Free Running, 1 + Stopped with CPU_STP# asserted LOW. This is a Read- and Write-Control bit.
2	0	44,43	CPU1T/C	Controls CPU1T and CPU1C functionality when CPU_STP# is asserted LOW 0 = Free Running, 1 Stopped with CPU_STP# asserted LOW. This and Read- and Write-control Bit.
1	1	40,39	CPU0T/C	CPU0T, CPU0C Output Control, 1= enabled, 0 = disabled. This is a Read- and Write-control bit.
0	1	44,43	CPU1T/C	CPU1T, CPU1C Output Control, 1= enabled, 0 = disabled. This is a Read- and Write-control bit.

Byte 7: PCI Clock Register (All bits are Read and Write functional)

Bit	@Pup	Pin#	Name	Description
7	1	15	PCI_F0	PCI_F0 Output Control 1 = enabled, 0 = forced LOW
6	1	14	PCI_F1	PCI_F1 Output Control 1 = enabled, 0 = forced LOW
5	1	23	PCI5	PCI5 Output Control 1 = enabled, 0 = forced LOW
4	1	22	PCI4	PCI4 Output Control 1 = enabled, 0 = forced LOW
3	1	21	PCI3	PCI3 Output Control 1 = enabled, 0 = forced LOW
2	1	20	PCI2	PCI2 Output Control 1 = enabled, 0 = forced LOW
1	1	17	PCI1	PCI1 Output Control 1 = enabled, 0 = forced LOW
0	1	16	PCI0	PCI0 Output Control 1 = enabled, 0 = forced LOW

Byte 8: Silicon Signature Register

Bit	@Pup	Description
7	1	Vendor ID 1000 = Cypress
6	0	
5	0	
4	0	
3	0	Revision ID
2	0	
1	0	
0	0	

Byte 9: Peripheral Control Register (All bits are Read-only)

Bit	@Pup	Pin#	Name	Description
7	1	33	PD#	PD# Enable. 0 = enable, 1 = disable
6	0			0 = when PD# asserted LOW, CPU(0:1)T stop in a high state, CPU(0:1)C stop in a low state. 1 = when PD# asserted LOW, CPU(0:1)T and CPU(0:1)C stop in H-Z.
5	1	27	48M	48M Output Control 1 = enabled, 0 = forced LOW
4	1	26	48M_24M	48M_24M Output Control 1 = enabled, 0 = forced LOW
3	1	26	48M_24M	48M_24M, 0 = pin28 output is 24 MHz, 1= pin28 output is 48 MHz.
2	0			SS2 Spread Spectrum control bit (0 = down spread, 1= Center spread)
1	0			SS1 Spread Spectrum control bit. See *Table 6*.
0	0			SS0 Spread Spectrum control bit. See *Table 6*.

Byte 10: Peripheral Control Register (All bits are Read-only)

Bit	@Pup	Pin#	Name	Description
7	1	47	SDCLK	SDCLK Output Enable 1 = enabled, 0 = disabled
6	1	4	REF2	REF2 Output Control 1 = enabled, 0 = forced LOW
5	1	3	REF1	REF1 Output Control 1 = enabled, 0 = forced LOW
4	1	2	REF0	REF0 Output Control 1 = enabled, 0 = forced LOW
3	1	10	ZCLK1	ZCLK1 Output Enable 1 = enabled, 0 = disabled
2	1	9	ZCLK0	ZCLK0 Output Enabled 1 = enabled, 0 = disabled
1	1	30	AGP1	AGP1 Output Enabled 1 = enabled, 0 = disabled
0	1	31	AGP0	AGP0 Output Enabled 1 = enabled, 0 = disabled

Byte 11: Dial-a-Skew™ and Dial-a-Ratio™ Control Register

Bit	@Pup	Name	Description
7	0	DARSD2	Programming these bits allow modifying the frequency ratio of the SDCLK clock relative to the VCO. See *Table 2*.
6	0	DARSD1	
5	0	DARSD0	
4	0	DARAG2	Programming these bits allow modifying the frequency ratio of the AGP(1:0), PCI(5:0) and PCIF(0:1) clocks relative to the VCO. See *Table 3*.
3	0	DARAG1	
2	0	DARAG0	
1	0	DASSD1	Programming these bits allow shifting skew between CPU and SDCLK signals. See *Table 4*.
0	0	DASSD0	

Table 2. Dial-a-Ratio SDCLK

DARSD (2:0)	VC0/SDCLK Ratio
000	Frequency Selection Default
001	2
010	3
011	4
100	5
101	6
110	8
111	9

Table 3. Dial-a-Ratio AGP(0:1)[4]

DARAG (2:0)	VC0/AGP ratio
000	Frequency Selection Default
001	6
010	7
011	8
100	9
101	10
110	10
111	10

Table 4. Dial-a-Skew SDCLK CPU

DASSD (1:0)	SDCLK-CPU Skew
00	0 ps (Default)[5]
01	+150 ps (CPU lag)*
10	+300 ps (CPU lag)*
11	+450 ps (CPU lag)*

Byte 12: Watchdog Time Stamp Register

Bit	@Pup	Name	Description
7	1		**SRESET#/PCI_STP#**. 1 = Pin 12 is the input pin as PCI_STP# signal. 0 = Pin 12 is the output pin as SRESET# signal.
6	0		**Frequency Revert**. This bit allows setting the Revert Frequency once the system is rebooted due to Watchdog time out only.0 = selects frequency of existing H/W setting1 = selects frequency of the second to last S/W setting. (the software setting prior to the one that caused a system reboot).
5	0		**WDTEST**. For WD-Test, ALWAYS program to “0.”
4	0		**WD Alarm**. This bit is set to “1” when the Watchdog times out. It is reset to “0” when the system clears the WD time stamps (WD3:0).
3	0	WD3	This bits selects the Watchdog Time Stamp Value. See *Table 5*.
2	0	WD2	
1	0	WD1	
0	0	WD0	

Table 5. Watchdog Time Stamp Table

WD(3:0)	FUNCTION
0000	Off
0001	1 second
0010	2 seconds
0011	3 seconds
0100	4 seconds
0101	5 seconds
0110	6 seconds
0111	7 seconds

Notes:
4. The ratio of AGP to PCI is retained at 2:1.
5. See *Figure 10* for CPU measurement point. See *Figure 11* for SDCLK measurement point.

Table 5. Watchdog Time Stamp Table (continued)

WD(3:0)	FUNCTION
1000	8 seconds
1001	9 seconds
1010	10 seconds
1011	11 seconds
1100	12 seconds
1101	13 seconds
1110	14 seconds
1111	15 seconds

Byte 13: Dial-a-Frequency™ Control Register N (All bits are Read and Write functional)[6]

Bit	@Pup	Description
7	0	Reserved
6	0	N6, MSB
5	0	N5
4	0	N4
3	0	N3
2	0	N2
1	0	N3
0	0	N0, LSB

Byte 14: Dial-a-Frequency Control Register R (All bits are Read and Write functional)[6]

Bit	@Pup	Description
7	0	Reserved
6	0	R5 MSB
5	0	R4
4	0	R3
3	0	R2
2	0	R1
1	0	R0, LSB
0	0	R and N register load gate 0 = gate closed (data is latched), 1 = gate open (data is loading from SMBus registers into R and N.)#

Note:
6. Byte 13 and Byte 14 should be Write together in every case.

Dial-a-Frequency Feature

SMBus Dial-a-Frequency feature is available in this device via Byte13 and Byte14. P is a large value PLL constant that depends on the frequency selection achieved through the hardware selectors (FS4, FS0). P value may be determined from the following table.

FS(4:0)	P
00110, 01000, 01010, 01100, 11001, 11011, 01101	32005333
00100, 00101, 10000, 10001, 10101, 10111, 11000, 11010, 11100, 11101, 11110, 11111	38406400
00000, 00001, 00010, 00111, 01001, 01011, 01110, 01111, 10010, 10100, 10110	48008000
00011, 10011	64010667

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique used to minimizing EMI radiation generated by repetitive digital signals. A clock presents the greatest EMI energy at the center frequency it is generating. Spread Spectrum distributes this energy over a specific and controlled frequency bandwidth therefore causing the average energy at any one point in this band to decrease in value. This technique is achieved by modulating the clock away from its resting frequency by a certain percentage (which also determines the amount of EMI reduction). In this device, Spread Spectrum is enabled by setting specific register bits in the SMBus control Bytes. See the SMBus register section of this data sheet for the exact bit and byte functionally. *Table 6* is a listing of the modes and percentages of Spread Spectrum modulation that this device incorporates.

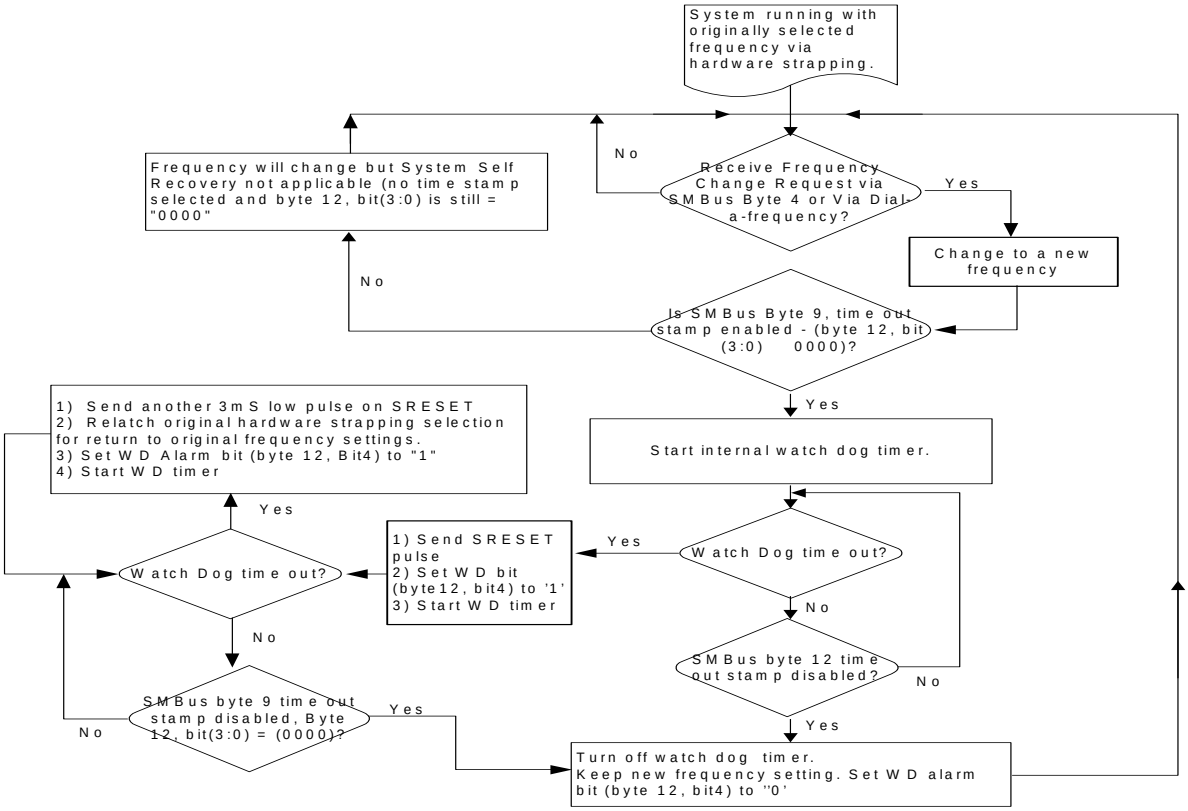
System Self Recovery Clock Management

This feature is designed to allow the system designer to change frequency while the system is running and reboot the operation of the system in case of a hang up due to the frequency change.

When the system sends an SMBus command requesting a frequency change through Byte 4 or through bytes 13 and 14, it must have previously sent a command to byte 12, for selecting which time out stamp the Watchdog must perform, otherwise the System Self Recovery feature will not be applicable. Consequently, this device will change frequency and then the Watchdog timer starts timing. Meanwhile, the system BIOS is running its operation with the new frequency. If this device receives a new SMBus command to clear the bits originally programmed in Byte 12, bits (3:0) (reprogram to 0000), before the Watchdog times out, then this device will keep operating in its normal condition with the new selected frequency. If the Watchdog times out the first time before the new SMBus reprograms Byte 12, bits (3:0) to (0000), then this device will send a low system reset pulse, on SRESET# (see byte12, bit7), and changes WD alarm (Byte12, Bit4) status to “1” then restarts the Watchdog timer again. If the Watchdog times out a second time, then this device will send another low pulse on SRESET#, will relatch original hardware strapping frequency (or second to last software selected frequency, see byte12, bit6) selection, set WD alarm bit (Byte12, bit4) to “1,” then start WD timer again. The above-described sequence will keep repeating until the BIOS clears the SMBus byte12 bits (3:0). Once the BIOS sets Byte 12 bits (3:0) = 0000, then the Watchdog timer is turned off and the WD alarm bit (Byte 12, bit4) is reset to “0.”

Table 6. Spread Spectrum

SS2	SS1	SS0	Spread Mode	Spread %
0	0	0	Down	0, -0.50
0	0	1	Down	+0.12, -0.62
0	1	0	Down	+0.25, -0.75
0	1	1	Down	+0.50, -1.00
1	0	0	Center	+0.25, -0.25
1	0	1	Center	+0.37, -0.37
1	1	0	Center	+0.50, -0.50
1	1	1	Center	+0.75, -0.75



CPU_STP# Clarification

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function.

CPU_STP# Assertion

When CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped after being sampled by two falling CPU clock edges. The final state of the stopped CPU signals is CPU = HIGH and CPU0# = LOW. There is no change to the output drive current values during the stopped state. The CPU is driven HIGH with a current value equal to (Mult 0 “select”) x (Iref), and the CPU# signal will not be driven. Due to external pull-down circuitry CPU# will be LOW during this stopped state.

CPU_STP# Deassertion

The de-assertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the de-Assertion to active outputs is no more than 2 CPU clock cycles.

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{setup}). (See *Figure 5*.) The PCI_F (0:2) clocks will not be affected by this pin if their control bits in the SMBus register are set to allow them to be free running.

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal will cause all PCI(0:6) and stoppable PCI_F(0:2) clocks to resume running in a synchronous manner within 2 PCI clock periods after PCI_STP# transitions to a HIGH level.

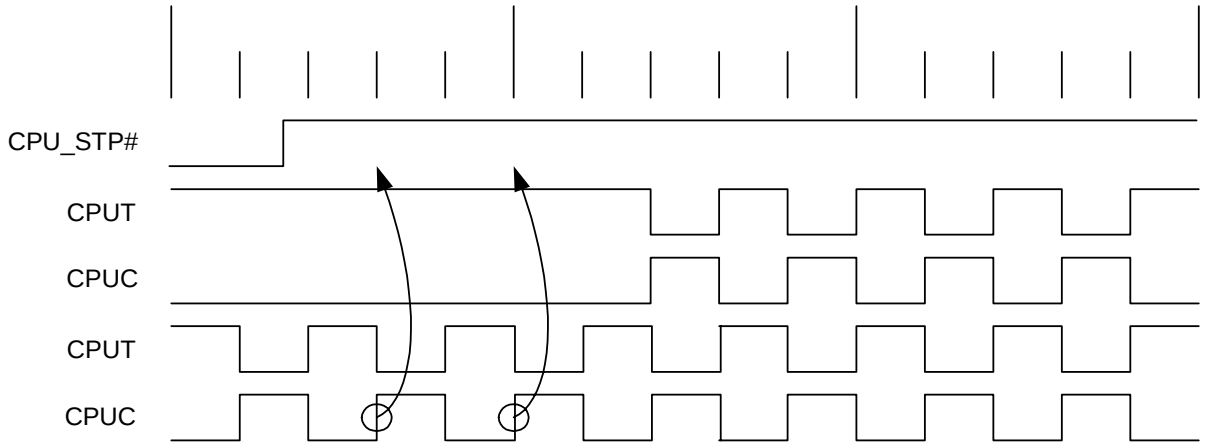


Figure 3. Deassertion CPU_STP# Waveform

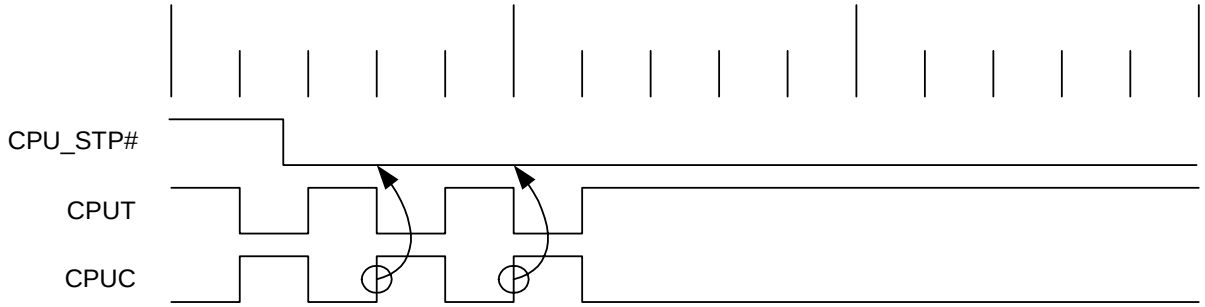


Figure 4. Assertion CPU_STP# Waveform

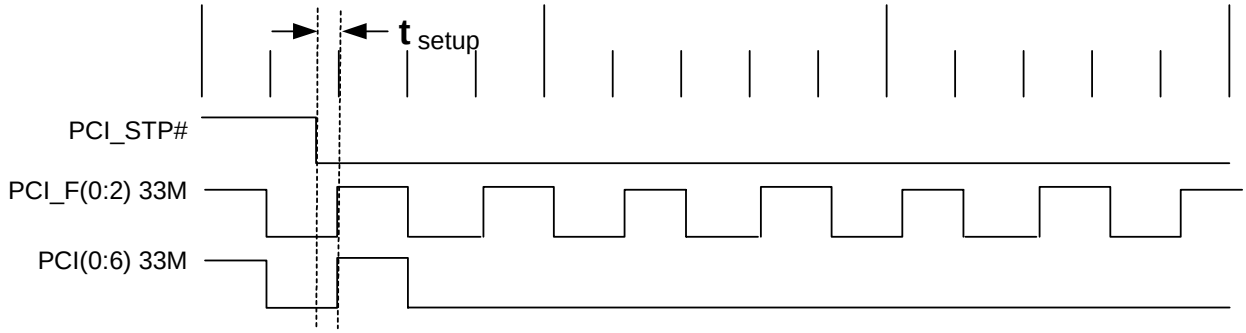


Figure 5. Assertion PCI_STP# Waveform

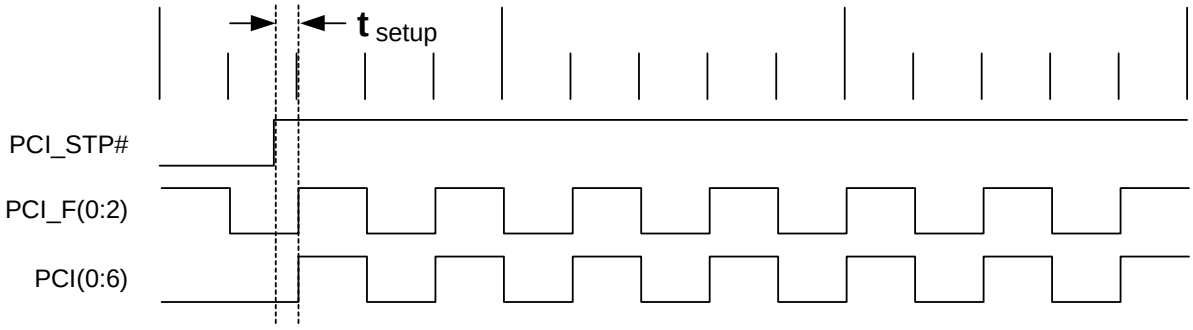


Figure 6. Deassertion PCI_STP# Waveform[7]

Note:

7. The PCI STOP function is controlled by two inputs. One is the device PCI_STP# pin number 34 and the other is SMBus Byte 0,Bit 3. These two inputs are logically ANDed. If either the external pin or the internal SMBus register bit is set LOW, the stoppable PCI clocks will be stopped in a logic LOW state. Reading SMBus Byte 0,Bit 3 will return a 0 value if either of these control bits are set LOW, thereby indicating that the device's stoppable PCI clocks are not running.

PD# (Power-down) Clarification

The PD# pin is used to shut off ALL clocks prior to shutting off power to the device. PD# is an asynchronous active LOW input. This signal is synchronized internally to the device powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. When PD# is LOW, all clocks are driven to a LOW value and held there; the VCO and PLLs are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the LOW “stopped” state.

PD# – Assertion (Transition from Logic “1” to Logic “0”)

When PD# is sampled LOW by two consecutive rising edges of CPUC clock, all clock outputs (except CPUT) clocks must be held LOW on their next HIGH-to-LOW transition. CPUT clocks must be hold with CPUT clock pin driven high with a value of 2× Iref and CPUC undriven.

Due to the state of internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

PD# – Deassertion (Transition from Logic “0” to Logic “1”)

The power-up latency between PD# rising to a valid logic “1” level and the starting of all clocks is less than 3.0 ms.

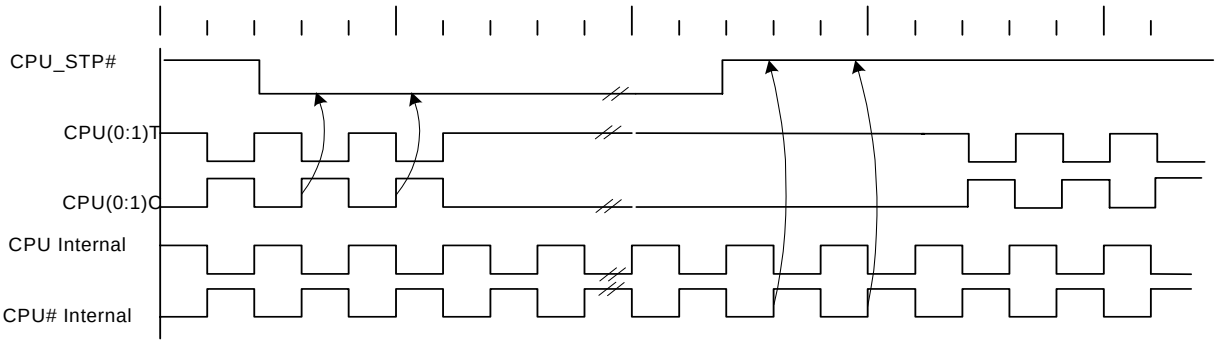


Figure 7. Power-down Assertion/Deassertion Timing Waveforms – Nonbuffered Mode

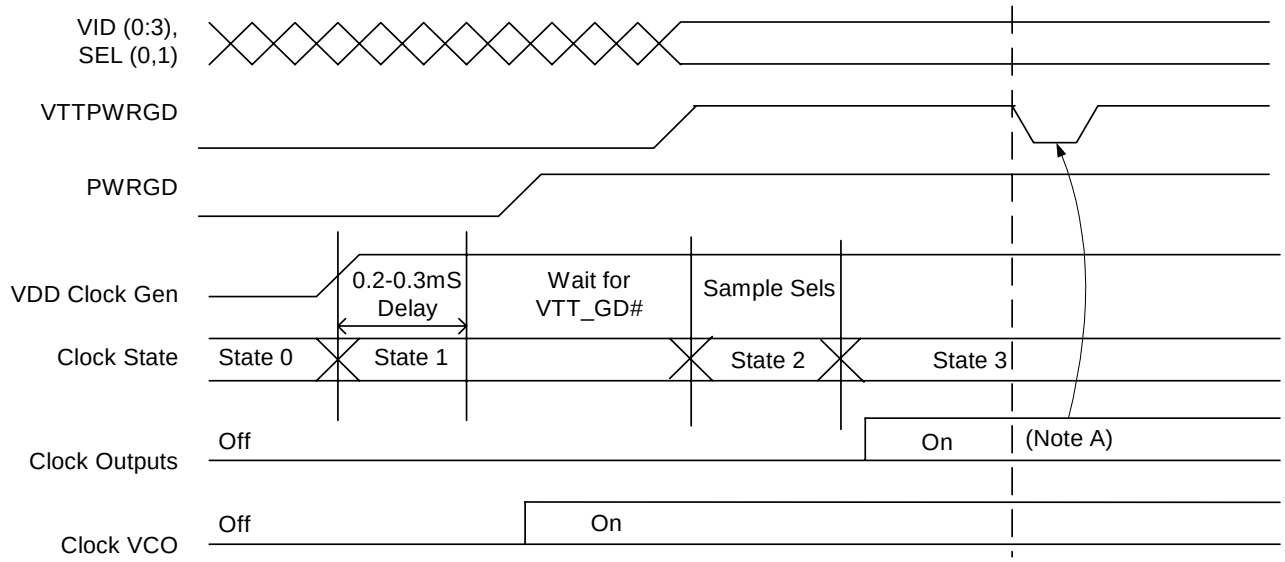


Figure 8. VTTPWRGD Timing Diagram[8]

Note:
8. Device is not affected, VTTPWRGD is ignored.

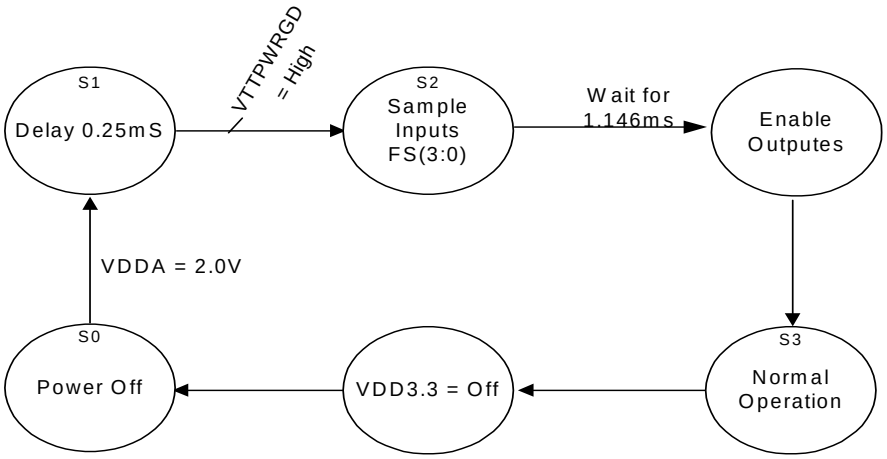


Figure 9. Clock Generator Power Up/Run State Diagram

Maximum Ratings[9.]

Input Voltage Relative to V_{SS}:.....V_{SS} – 0.3V
Input Voltage Relative to V_{DDQ} or AV_{DD}: ..... V_{DD} + 0.3V
Storage Temperature: .....–65°C to + 150°C
Operating Temperature: ..... 0°C to +70°C
Maximum Power Supply:..... 3.5V

DC Characteristics

Current Accuracy[10]

Parameter	Description	Conditions	Min.	Max.	Load
Iout	V_{DD} = nominal (3.30V)	M0 = 0 or 1 and Rr shown in table	–7% Inom	+7% Inom	Nominal test load for given configuration
Iout	V_{DD} = 3.30 ±5%	All combinations of M0 or 1 and Rr shown in table	–12% Inom	+12% Inom	Nominal test load for given configuration

DC Component Parameters (V_{DD} = 3.3V±5%, TA = 0°C to 70°C)

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Idd3.3V	Dynamic Supply Current	All frequencies at maximum values[11]			280	mA
Ipd3.3V	Power-down Supply Current	PD# Asserted			*See Note 11*	mA
Cin	Input Pin Capacitance				5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Cxtal	Crystal Pin Capacitance	Measured from the X_{IN} or X_{OUT} pin to Ground	30	36	42	pF

Table 7. Maximum Lumped Capacitive Output Loads

Clock	Max. Load	Unit
PCI(0:5), PCI_F(0:1)	30	pF
AGP (0:1), SDCLK	30	pF
ZCLK (0:1)	30	pF
48M_24, 48M Clock	20	pF
REF (0:2)	30	pF
CPU(0:1)T CPU(0:1) C	2	pF

Notes:
9. **Multiple Supplies** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
10. Inom refers to the expected current based on the configuration of the device.
11. Absolute value = (Programmed CPU Iref 97) +10 mA.

AC Parameters[12]

Parameters	Description	100 MHz		133 MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
Crystal							
TDC	X_{IN} Duty Cycle	47.5	52.5	47.5	52.5	%	13,21
TPeriod	X_{IN} Period	69.841	71.0	69.841	71.0	ns	13,14,16,21
VHIGH	X_{IN} HIGH Voltage	$0.7V_{DD}$	V_{DD}	$0.7V_{DD}$	V_{DD}	V	
VLOW	X_{IN} LOW Voltage	0	$0.3V_{DD}$	0	$0.3V_{DD}$	V	
Tr/Tf	X_{IN} Rise and Fall Times		10.0		10.0	ns	
TCCJ	X_{IN} Cycle-to-Cycle Jitter		500		500	ps	14,17,21
CPU at 0.7V Timing							
TSKEW	Any CPU to CPU Clock Skew		150		150	ps	17, 24, 28
TCCJ	CPU Cycle-to-Cycle Jitter		150		150	ps	17, 24, 28
TDC	CPU and CPUC Duty Cycle	45	55	45	55	%	17, 24, 28
TPeriod	CPU and CPUC Period	9	10.2	7.35	7.65	ns	17, 24, 28
Tr / Tf	CPU and CPUC Rise and Fall Times	175	700	175	700	ps	17, 18
	Rise/Fall Matching		20%		20%		18, 27, 28
DeltaTr	Rise Time Variation		125		125	ps	18, 28
DeltaTf	Fall Time Variation		125		125	ps	18, 28
Vcross	Crossing Point Voltage at 0.7V Swing	280	430	280	430	mV	18, 24, 28
AGP							
TDC	AGP Duty Cycle	45	55	45	55	%	14, 16
TPeriod	AGP Period	15.0	15.3	15.0	15.3	ns	14, 16
THIGH	AGP HIGH Time	5.25	–	5.25		ns	25
TLOW	AGP LOW Time	5.05	–	5.05		ns	26
Tr / Tf	AGP Rise and Fall Times	0.5	1.6	0.5	1.6	ns	14, 15
Tskew Unbuffered	Any AGP to Any AGP Clock Skew		175		175	ps	14, 16
TCCJ	AGP Cycle-to-Cycle Jitter		250		250	ps	14, 16
ZCLK							
TDC	ZCLK(0:1) Duty Cycle	45	55	45	55	%	14, 16
Tr / Tf	ZCLK(0:1) Rise and Fall Times	0.5	1.6	0.5	1.6	ns	14, 15
TSKEW	Any ZCLK(0:1) to Any ZCLK(0:1) Skew		175		175	ps	14, 16
TCCJ	ZCLK(0:1)Cycle-to-Cycle Jitter		250		250	ps	14,16
PCI							
TDC	PCI_F(0:1) PCI (0:5) Duty Cycle	45	55	45	55	%	14, 16
TPeriod	PCI_F(0:1) PCI (0:5) Period	30.0		30.0		nS	13,14,16
THIGH	PCI_F(0:1) PCI (0:5) HIGH Time	12.0		12.0		nS	25
TLOW	PCI_F(0:1) PCI (0:5) LOW Time	12.0		12.0		nS	26
Tr / Tf	PCI_F(0:1) PCI (0:5) Rise and Fall Times	0.5	2.0	0.5	2.0	nS	14, 15
TSKEW	Any PCI Clock to Any PCI Clock Skew		500		500	pS	14, 16
TCCJ	PCI_F(0:1) PCI (0:5) Cycle-to-Cycle Jitter		250		250	ps	14, 16
SDCLK							
TDC	SDCLK Duty Cycle	45	55	45	55	%	14, 16
TPeriod	SDCLK Period	7.4	15	7.4	15	ns	14, 16
THIGH	SDCLK HIGH Time	3.0		1.87		ns	25

AC Parameters[12] (continued)

Parameters	Description	100 MHz		133 MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
TLOW	SDCLK LOW Time	2.8		1.67		ns	26
Tr / Tf	SDCLK Rise and Fall Times	0.4	1.6	0.4	1.6	ns	14, 15
TCCJ	SDCLK Cycle-to-Cycle Jitter	-	250	-	250	ps	14, 15
48M							
TDC	48M Duty Cycle	45	55	45	55	%	14, 16
TPeriod	48M Period	20.829	20.834	20.829	20.834	ns	14, 16
Tr / Tf	48M Rise and Fall Times	1.0	2.0	1.0	2.0	ns	14, 15
TCCJ	48M Cycle-to-Cycle Jitter		350		350	ps	14, 16
24M							
TDC	24MHz Duty Cycle	45	55	45	55	%	14, 16
TPeriod	24MHz Period	41.66	41.67	41.66	41.67	ns	14, 16
Tr / Tf	24MHz Rise and Fall Times	1.0	4.0	1.0	4.0	ns	14, 15
TCCJ	24MHz Cycle-to-Cycle Jitter		500		500	ps	14, 16
REF							
TDC	REF Duty Cycle	45	55	45	55	%	14, 16
TPeriod	REF Period	69.8413	71.0	69.8413	71.0	ns	14, 16
Tr / Tf	REF Rise and Fall Times	1.0	4.0	1.0	4.0	ns	14, 15
TCCJ	REF Cycle-to-Cycle Jitter		1000		1000	ps	14, 16
ENABLE/DISABLE and SETUP							
tpZL, tpZH	Output Enable Delay (all outputs)	1.0	10.0	1.0	10.0	ns	
tpLZ, tpZH	Output Disable Delay (all outputs)	1.0	10.0	1.0	10.0	ns	
tstable	All Clock Stabilization from Power-up		1.5		1.5	ms	19
tss	Stopclock Set-up Time	10.0		10.0		ns	
tsh	Stopclock Hold Time	0		0		ns	20

Notes:

12. All outputs loaded as per maximum capacitive load table. See *Table 7*.
13. This parameter is measured as an average over 1µs duration with a crystal center frequency of 14.318 MHz.
14. All outputs loaded per *Table 7*, below.
15. Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals (see test and measurement set-up section of this data sheet).
16. Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals (see test and measurement set-up section of this data sheet).
17. This measurement is applicable with Spread On or Spread OFF.
18. Measured from V_{OL} = 0.175 to V_{OH} = 0.525V.
19. The time specified is measured from when all V_{DD}s reach their supply rail (3.3V) until the frequency output is stable and operating within the specifications.
20. CPU_STP# and PCI_STP# set-up time with respect to any PCI_F clock to guarantee that the effected clock will stop or start at the next PCI_F clock's rising edge.
21. When X_{IN} is driven from an external clock source.
22. When crystal meets minimum 40-ohm device series resistance specification.
23. This is required for the duty cycle on the REF clock out to be as specified. The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within data sheet specifications.
24. Measured at crossing point (Vx) or where subtraction of CLK–CLK# crosses 0V.
25. THIGH is measured at 2.4V for all non-host outputs.
26. TLOW is measured at 0.4V for all non-host outputs.
27. Determined as a fraction of 2*(Trise-Tfall)/ (Trise+Tfall).
28. For CPU load. See *Figure 10*.

Test and Measurement Set-up

For Differential CPU Output Signals

The following diagram shows lumped test load configurations for the differential host clock outputs.

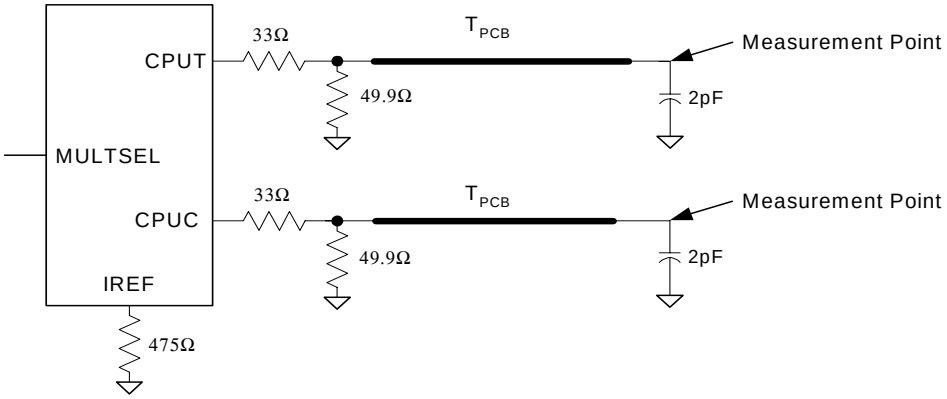
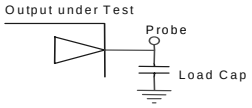


Figure 10. 0.7V Configuration



3.3V signals

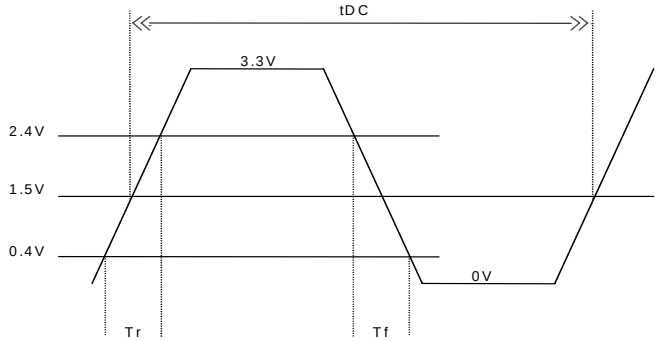


Figure 11. Lumped LoadFor Single-Ended Output Signals (for AC Parameters Measurement)

Table 8. CPU Clock Current Select Function

Mult0	Board Target Trace/Term Z	Reference R, Iref – Vdd (3*Rr)	Output Current	V_{OH} @ Z
0	50 ohms (not used)	Rr = 221 1%, Iref = 5.00 mA	Ioh = 4*Iref	1.0V @ 50
1	50 ohms	Rr = 475 1%, Iref = 2.32 mA	Ioh = 6*Iref	0.7V @ 50

Table 9. Group Timing Relationship and Tolerances

	Offset	Tolerance (or Range)	Conditions	Notes
CPU to SDCLK	TypicaL 0 ns	±2 ns	CPU leads	Note 29
CPU to AGP	TypicaL 2 ns	1–4 ns	CPU leads	Note 29
CPU to ZCLK	TypicaL 2 ns	1–4 ns	CPU leads	Note 29
CPU to PCI	Typical 2 ns	1–4 ns	CPU leads	Note 29

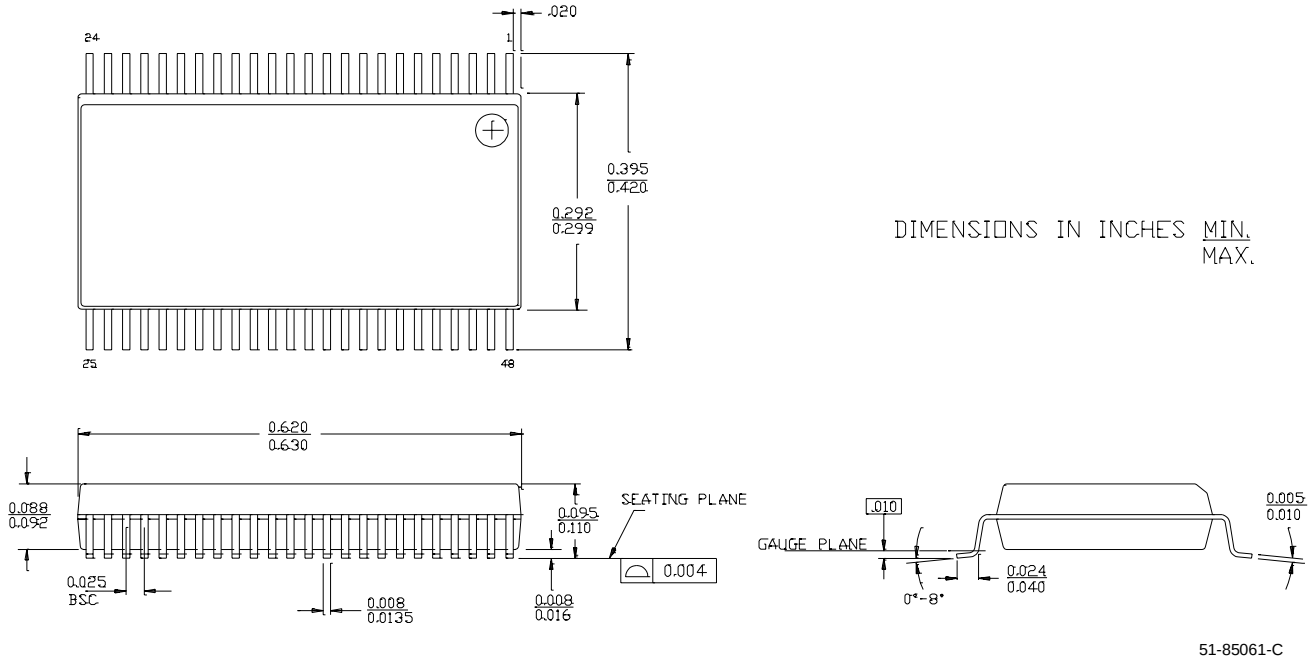
Note:
29. See *Figure 10* for CPU clocks measurement point. See*Figure 11* for SDCLK, AGP, ZCLK and PCI Outputs measurement point.

Ordering Information

Part Number	Package Type	Product Flow
IMIC9915AY	48-Pin Shrunk Small Outline package (SSOP)	Commercial, 0° to 70°C
IMIC9915AYT	48-Pin Shrunk Small Outline package (SSOP) – Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

48-lead Shrunk Small Outline Package O48



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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	112009	03/01/02	DMG	New Data Sheet
*A	117409	08/20/02	RGL	Corrected the Ordering Information to match the Dev Master
*B	122792	12/14/02	RBI	Add Power up Requirements to Operating Conditions Information