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ECL Products	

10176
Flip-Flop

Hex D-Type Master-Slave Flip-Flop

FEATURES

- **Typical propagation delay: 150MHz**
- **Typical supply current ($-I_{EE}$): 88mA**

DESCRIPTION

The 10176 includes six high-speed master-slave D-type flip-flops with one common input Clock for all six. Data enters into the master during the Low-State of the clock and is transferred to the slave during the positive-going Clock transition. Due to the master-slave structure of the device, a change in the information present at the data (D_n) input will not modify the output information at any other time. All unused inputs must be tied Low to V_{IL} or V_{EE}.

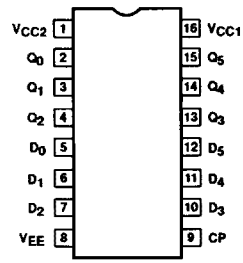
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic DIP	10176N
16-Pin Ceramic DIP	10176F

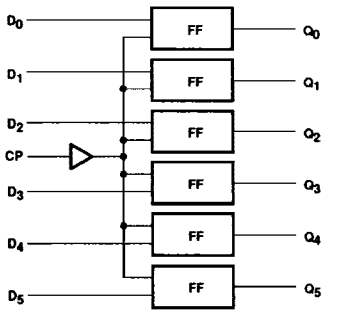
PIN DESCRIPTION

PINS	DESCRIPTION
D_0 - D_5	Data Inputs
CP	Clock Input
Q_0 - Q_5	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
CP	D_n	Q_{n+1}
L	X	Q_n
H	L	L
H	H	H

H = High Voltage Level = 1
L = Low Voltage Level = 0
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

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DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{ILMIN} to CP input with V_{IHMAX}	−1060		−890	mV
			$T_A = +25°C$	applied to all other inputs. Raise CP from	−960		−810	mV
			$T_A = +85°C$	V_{ILMIN} to V_{IHMAX} and measure V_{OH}.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{ILMIN} to CP input with V_{IHMAX}	−1080			mV
			$T_A = +25°C$	applied to all other inputs. Raise CP from	−980			mV
			$T_A = +85°C$	V_{ILMIN} to V_{IHT} and measure V_{OHT}.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{ILMIN} to all inputs. Raise			−1655	mV
			$T_A = +25°C$	CP input from V_{ILMIN} to			−1630	mV
			$T_A = +85°C$	V_{IHT} and measure V_{OLT}.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	Apply V_{ILMIN} to all inputs. Raise	−1890		−1675	mV
			$T_A = +25°C$	CP input from V_{ILMIN} to	−1850		−1650	mV
			$T_A = +85°C$	V_{IHMAX}. Measure V_{OL}.	−1825		−1615	mV
I_{IH}	High level input current	Other inputs	$T_A = -30°C$	Apply V_{IHMAX} to each D_n input under			350	µA
			$T_A = +25°C$	test, one at a time, with V_{ILMIN}			220	µA
			$T_A = +85°C$	applied to all other inputs.			220	µA
		CP input	$T_A = -30°C$	Apply V_{IHMAX} to CP input			495	µA
			$T_A = +25°C$	with V_{ILMIN} applied to all			310	µA
			$T_A = +85°C$	other inputs.			310	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				121	mA
			$T_A = +25°C$			88	101	mA
			$T_A = +85°C$				121	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

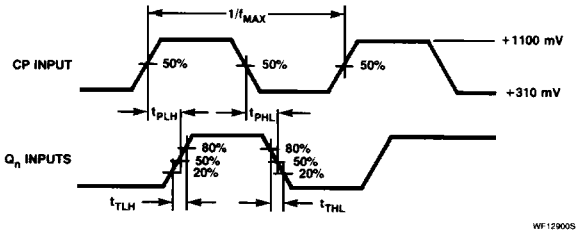
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

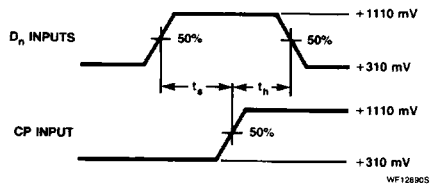
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency	Waveform 1	125		125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1.60 1.60	4.60 4.60	1.60 1.60		4.50 4.50	1.60 1.60	5.00 5.00	ns ns
t_s	Setup time D_n to CP	Waveform 2	2.50		2.50			2.50		ns
t_h	Hold time D_n to CP	Waveform 2	1.50		1.50			1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	4.10 4.10	1.10 1.10		4.00 4.00	1.10 1.10	4.40 4.40	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for CP to Q_n



Waveform 2. Setup and Hold Times for D_n to CP