High-Speed CMOS 32Kx8 SRAM with Common I/O

QS83280
ADVANCE INFORMATION

FEATURES/BENEFITS

- Equal access and cycle times
- 12ns/15ns/20ns/25ns/30ns Commercial
- JEDEC standard pinout
- TTL compatible I/O
- Available in 28-pin 300/600-mil DIP, SOJ, PLCC, LCC
- 6-Transistor cell for high reliability
- 15ns/20ns/25ns/30ns Military
- Military product compliant to MIL-STD-883
- Low power, high-speed QCMOS™ technology

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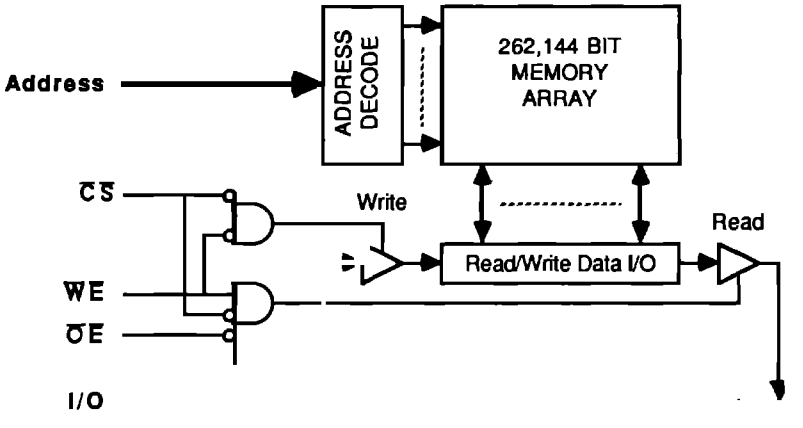
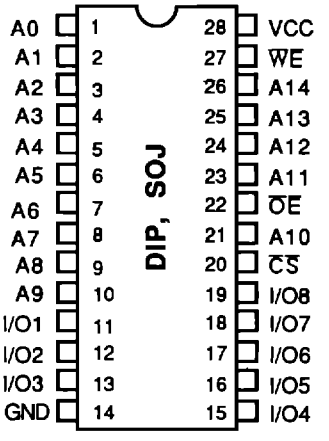
DESCRIPTION

The QS83280 is a high-speed 256K SRAM organized as 32K words of 8 bits. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS83280 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

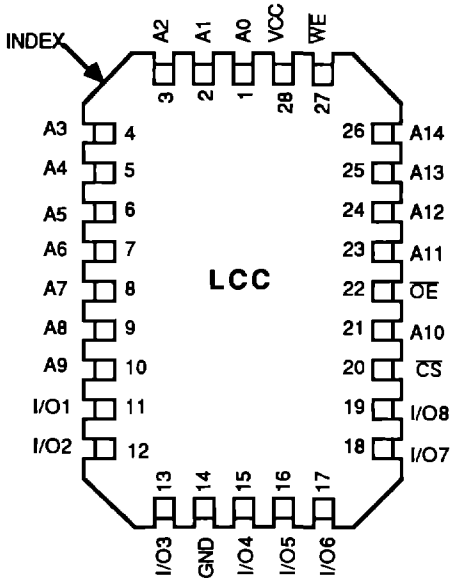
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



ALL PINS TOP VIEW



PIN DESCRIPTION

Pin Name	I/O	Function
A	I	Address
I/O1 - I/O8	I/O	Data
$\overline{CS}$	I	Chip Select
$\overline{WE}$	I	Write Enable
$\overline{OE}$	I	Output Enable

FUNCTION TABLE

Function	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Deselect	H	X	X	High Z	Standby
Read	L	H	L	Data out	Active
Write	L	L	X	Data In	Active
Output Disable	L	H	H	High Z	Active

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to V_{CC} + 0.5V
DC Input Voltage V_I ..... -0.5V to V_{CC} + 0.5V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Output Current Max. sink current/pin..... 50 mA
DC Output Current Max. source current/pin..... 30 mA
T_{BIAS} Temperature Under Bias, COM..... -65° to +125°C
T_{STG} Storage Temperature, COM..... -65° to +125°C
T_{BIAS} Temperature Under Bias, MIL..... -65° to +135°C
T_{STG} Storage Temperature, MIL..... -65° to +155°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

Ta=+25°C, f=1 MHz

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	Vin = 0 V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	Vout = 0 V PDIP Pkg.		7	pF
Cout	Output Capacitance	Vout = 0 V SOJ Pkg.		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
|Ili|	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	µA
|Ilo|	Output Leakage	Vcc = MAX, Vout = GND to Vcc Chip deselcted		5		10	

Notes:
1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-12		-15		-20		-25/-30		Unit
		C	M	C	M	C	M	C	M	
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	100	120	100	120	100	120	100	120	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	180	190	170	180	160	170	150	160	
Isb	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	90	100	90	100	90	100	90	100	
Isb1	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	15	20	15	20	15	20	15	20	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	12ns(3)		15ns(3)		20ns		25ns		30ns	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE											
t RC	Read Cycle Time	12	-	15	-	20	-	25	-	30	-
t AA	Address Access Time	-	12	-	15	-	20	-	25	-	30
t ACS	Chip Select Access Time	-	12	-	15	-	20	-	25	-	30
t OH	Output Hold from Address Change	2	-	2	-	2	-	2	-	2	-
t CLZ	Chip Select to Output in Low Z (2)	2	-	2	-	2	-	2	-	2	-
tCHZ	Chip Select to Output in High Z (2)	-	6	-	7	-	8	-	10	-	12
tOE	Output Enable Access Time		7		8		10		12		15
tOHZ	Output enable to output in High Z (2)	-	6	-	7	-	8	-	10	-	12
tOLZ	Output enable to output in Low Z (2)	0	-	0	-	0	-	0	-	0	-
tPU	Chip select to Power-Up time(2)	0	-	0	-	0	-	0	-	0	-
tPD	Chip select to Power-Down time	-	12	-	15	-	20	-	25	-	30

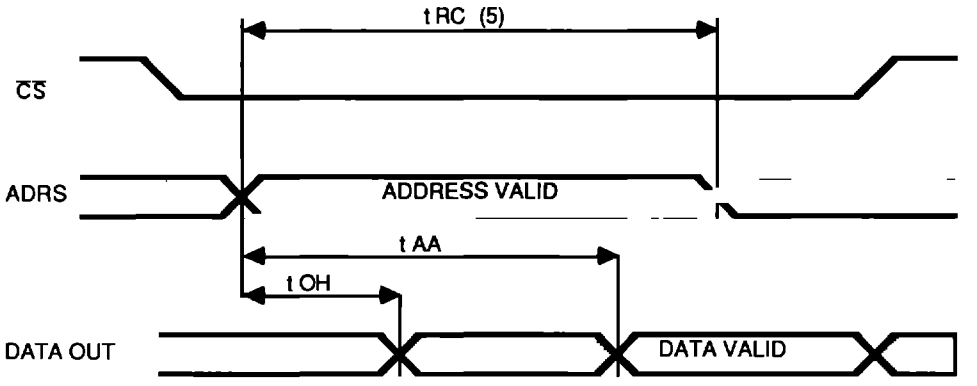
Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) For Vcc±5% Commercial Only-Preliminary Data

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

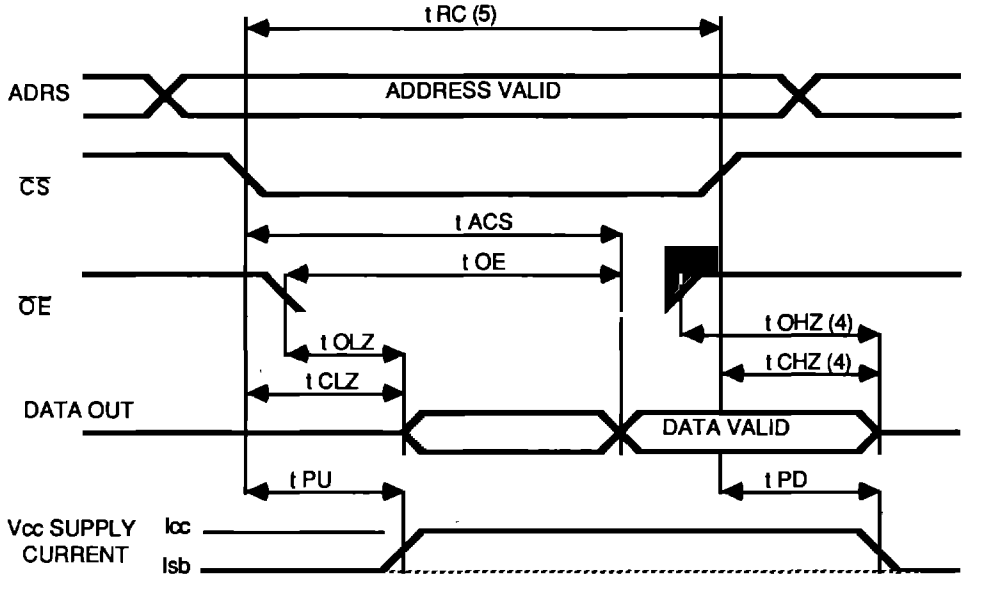
Symbol	Parameter (1)	-12ns (3)		-15ns(3)		-20ns		-25ns		-30ns	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE											
t WC	Write Cycle Time	12	-	15	-	20	-	25	-	30	-
t CW	Chip Select Valid to End of Write	10	-	13	-	17	-	20	-	25	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-	0	-
t WP	Write Pulse width	10	-	12	-	16	-	20	-	25	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	7	-	8	-	10	-	15	-	20	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in High Z (2)	-	6	-	7	-	8	-	10	-	12
t OW	Output Active from End of Write (2)	0	-	0	-	0	-	0	-	0	-
t AW	Address Valid to End of Write	10	-	13	-	17	-	20	-	25	-

Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) For Vcc±5% Commercial Only-Preliminary Data

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2,3)

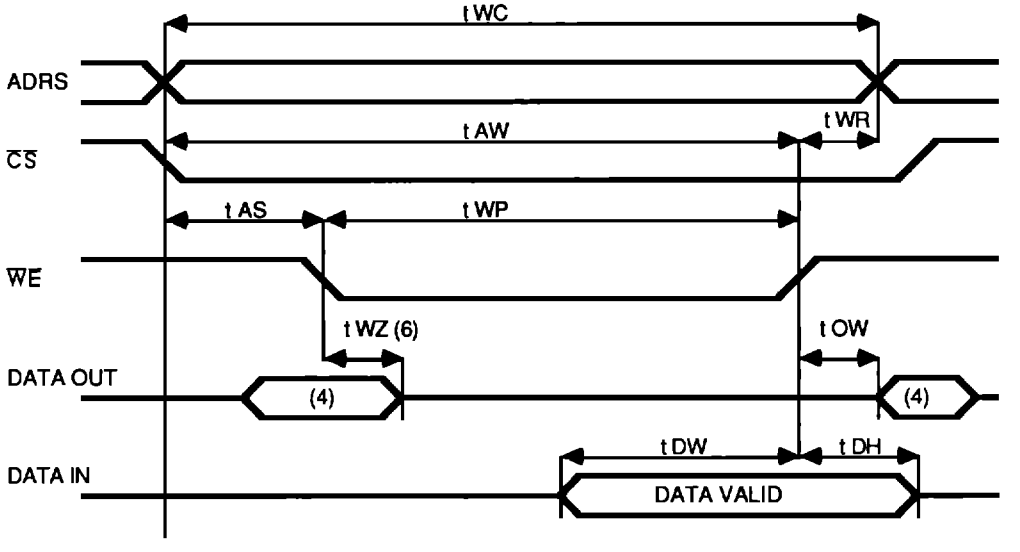


TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)

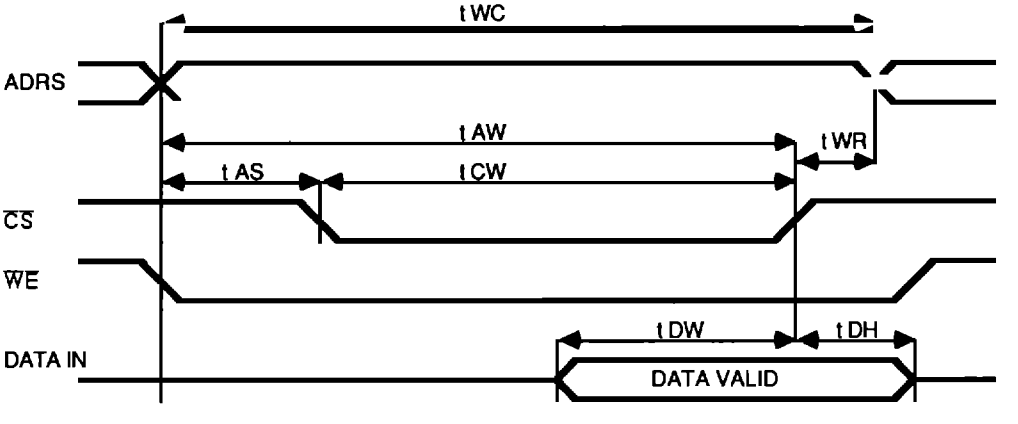


Notes:
1. $\overline{WE}$ is high for Read cycle.
2. $\overline{CS}$ is low for Read cycle #1.
3. Address is valid to or coincident with $\overline{CS}$ transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 $\overline{WE}$ controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 $\overline{CS}$ controlled timing)



Notes:
1. $\overline{WE}$ or $\overline{CS}$ must be high during address transitions.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t WR is measured from the earlier of $\overline{CS}$ and $\overline{WE}$ going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.