

TENTATIVE

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1,048,576-WORD × 16-BIT FAST PAGE DYNAMIC RAM

DESCRIPTION

The TC51V16160CJ/CFT is a fast page dynamic RAM organized as 1,048,576 words by 16 bits. The TC51V16160CJ/CFT utilizes TOSHIBA's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC51V16160CJ/CFT to be packaged in a 42-pin plastic SOJ or a 50-pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. Other features include a single power supply of 3.3 V ± 0.3 V tolerance and direct interfacing with high performance logic families such as LVTTTL.

FEATURES

- 1,048,576-word by 16-bit organization
- Fast access time and cycle time
- Single power supply of 3.3 V ± 0.3 V with a built-in V_{BB} generator
- Low-power dissipation (max)
 - Operating: 432 mW (50 ns type)
 - : 360 mW (60 ns type)
 - Stand by : 1.8 mW (both devices)
- Unlatched outputs at cycle end allows two-dimensional chip selection
- Read-Modify-Write, CAS-before-RAS refresh, RAS-Only refresh, Hidden refresh and Fast Page mode capability
- 4096 refresh cycles per 64 ms
- Package
 - CJ : SOJ42-P-400-1.27, 1.66 grams
 - CFT: TSOP II 50/44-P-400-0.80, 0.53 grams

		TC51V16160CJ/CFT	
		-50	-60
t _{RAC}	RAS Access Time	50 ns	60 ns
t _{AA}	Column Address Access Time	25 ns	30 ns
t _{CAC}	CAS Access Time	13 ns	15 ns
t _{RC}	Cycle Time	90 ns	110 ns
t _{PC}	Fast Page Mode Cycle Time	35 ns	40 ns

PIN ASSIGNMENT (TOP VIEW)

Plastic SOJ				Plastic TSOP			
V _{CC}	1	42	V _{SS}	V _{CC}	1	50	V _{SS}
I/O1	2	41	I/O16	I/O1	2	49	I/O16
I/O2	3	40	I/O15	I/O2	3	48	I/O15
I/O3	4	39	I/O14	I/O3	4	47	I/O14
I/O4	5	38	I/O13	I/O4	5	46	I/O13
V _{CC}	6	37	V _{SS}	V _{CC}	6	45	V _{SS}
I/O5	7	36	I/O12	I/O5	7	44	I/O12
I/O6	8	35	I/O11	I/O6	8	43	I/O11
I/O7	9	34	I/O10	I/O7	9	42	I/O10
I/O8	10	33	I/O9	I/O8	10	41	I/O9
NC	11	32	NC	NC	11	40	NC
NC	12	31	LCAS	NC	15	36	NC
WE	13	30	UCAS	NC	16	35	LCAS
RAS	14	29	OE	WE	17	34	UCAS
A11R	15	28	A9R	RAS	18	33	OE
A10R	16	27	A8R	A11R	19	32	A9R
A0	17	26	A7	A10R	20	31	A8R
A1	18	25	A6	A0	21	30	A7
A2	19	24	A5	A1	22	29	A6
A3	20	23	A4	A2	23	28	A5
V _{CC}	21	22	V _{SS}	A3	24	27	A4
				V _{CC}	25	26	V _{SS}

PIN NAMES

A0 to A11	Address Inputs
RAS	Row Address Strobe
UCAS	Column Address Strobe / Upper Byte Control
LCAS	Column Address Strobe / Lower Byte Control
WE	Write Enable
OE	Output Enable
I/O1 to I/O16	Data I/O
V _{CC}	Power (+ 3.3 V)
V _{SS}	Ground
N.C.	No Connection

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BLOCK DIAGRAM

