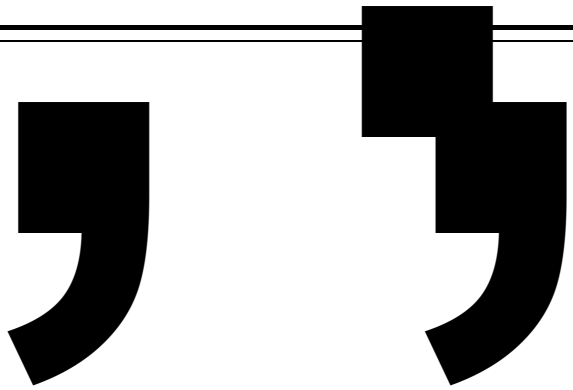
36Mb NtRAM™ Specification

100TQFP / 165FBGA with Pb only



1. For updates or additional information about Samsung products, contact your nearest Sa

2. Samsung products are not intended for use in life support, critical care, medical, safet
   lar applications where Product failure couldresult in loss of life or personal or physica
   or defense application, or any governmental procurement to which special terms or p

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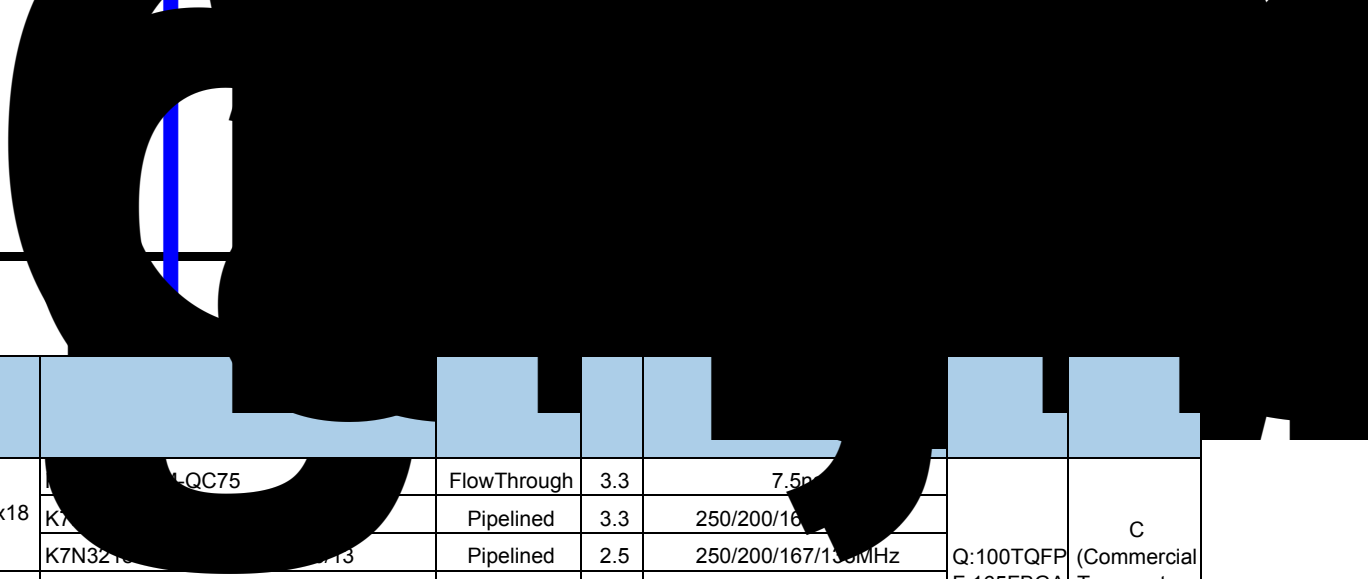
0.0	1. Initial document.	May. 10. 2001	Preliminary
0.1	1. Add 165FBGA package	Aug. 29. 2001	Preliminary
0.2	1. Update JTAG scan order 2. Speed bin merge. From K7N3236(18)09M to K7N3236(18)01M 3. AC parameter change. tOH(min)/tLZC(min) from 0.8 to 1.5 at -25 tOH(min)/tLZC(min) from 1.0 to 1.5 at -22 tOH(min)/tLZC(min) from 1.0 to 1.5 at -20	Dec. 31. 2001	Preliminary
0.3	1. Change pin out for 165FBGA - x18/x36 ; 11B => from A to NC , 2R ==> from NC to A	Feb. 14. 2002	Preliminary
0.4	1. Insert pin at JTAG scan order of 165FBGA in connection with pin out change - x18/x36 ; insert Pin ID of 2R to $\overline{BIT}$ number of 69	Apr. 20. 2002	Preliminary
0.5	1. Add Icc, Isb, Isb1 and Isb2 values.	May. 10. 2002	Preliminary
1.0	1. Final datasheet release.	Sep. 26. 2002	Final
1.1	1. Change the Stand-by current (Isb) Before After Isb - 25 : 120 170 - 22 : 110 160 - 20 : 100 150 - 16 : 90 140 - 15 : 90 140 - 13 : 90 140 Isb1 : 90 110 Isb2 : 80 100	Oct. 17. 2003	Final
2.0	1. Delete the 119BGA package 2. Delete the 225MHz and 150MHz speed bin	Nov. 18. 2003	F
3.0	1. Add the overshoot timing	Feb. 16. 2	



2Mx18	[illegible]-QC75	FlowThrough	3.3	7.5n[illegible]	Q:100TQFP F:165FBGA	C (Commercial Temperature Range)
	K7[illegible]	Pipelined	3.3	250/200/16[illegible]		
	K7N321[illegible]/13	Pipelined	2.5	250/200/167/13[illegible]MHz		
1Mx36	K7M323625M-QC75	FlowThrough	3.3	7.5ns		
	K7N323601M-Q(F)C25/20/16/13	Pipelined	3.3	250/200/167/133MHz		
	K7N323645M-Q(F)C25/20/16/13	Pipelined	2.5	250/200/167/133MHz		

[redacted]

t

t

• 3.3V+0.16[redacted]23601M an[redacted]801M are 37,748,736-bits
• I/O Supply[redacted]tic SRA[redacted]
or 2.5V+0.4[redacted]o Tur[redacted]ndom Access Memory uti-
• Byte Writa[redacted]ith in [redacted]ration of operating cycles.
• Enable clo[redacted]its, a[redacted]rol signals except output
• Single RE[redacted]urst o[redacted]rchronized to input clock.
• Self-Timed[redacted]l must [redacted] or Low".
• Three Chip[redacted]uts incl[redacted]p mode enable(ZZ).
contention[redacted]trols th[redacted]any given time.
• A interleav[redacted]nall[redacted]and initiated by the rising
• Asynchron[redacted]
• Power Dow[redacted]liminates complex off-chip
• 100-TQFP[redacted]
• 165FBGA([redacted]

Cycle Time	tC
Clock Access Time	tC
Output Enable Access Time	tO

A [0:19]or
A [0:20]

CLK
K
CKE

$\overline{CS_1}$
CS_2
$\overline{CS_2}$
ADV
$\overline{WE}$
$\overline{BW_x}$
(x=a,b,c,d or

$\overline{OE}$
ZZ

DQa0 ~ DQd7
DQPa ~ DQP

36 or 18

[redacted] Access Memory

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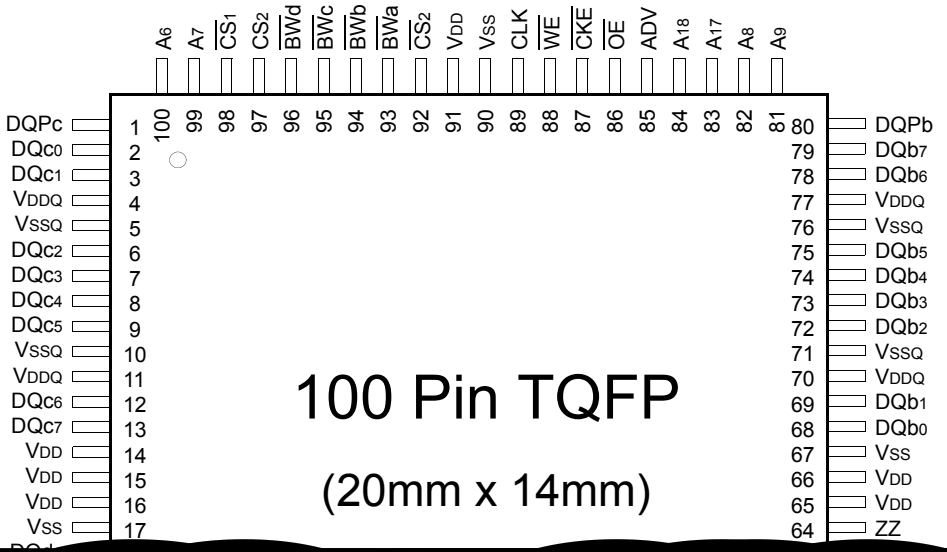
(TOP VIEW)



[redacted]

A0 -	Address Inputs	32,33,34,35,36,37,43, 44,45,46,47,48,49,50, 81,82,83,84,99,100	VDD	Power Supply(+3.3	15,16 17,40
ADV	ress Advance/	85	N.C.	No Connect	3
WE	Contro	88			
CLK		89	DQa0~a7	Data Inputs/Outputs	
CKE		87	DQb0~b7	Data Inputs/Outputs	
CS1		98	DQc0~c7	Data Inputs/Outputs	
CS2	Ch	97	DQd0~d7	Data Inputs/Output	
CS2	Chi	92	DQPa~Pd	Data Inputs/Output	
BWx		93,94,95,96			
OE		86	VDDQ	Output Power Sup	
ZZ	Power Si	64		(3.3V or 2.5V)	
LBO	Burst Mod	31	VSSQ	Output Ground	

[redacted] (LSB) of the address field and set the internal burst counter if burst is

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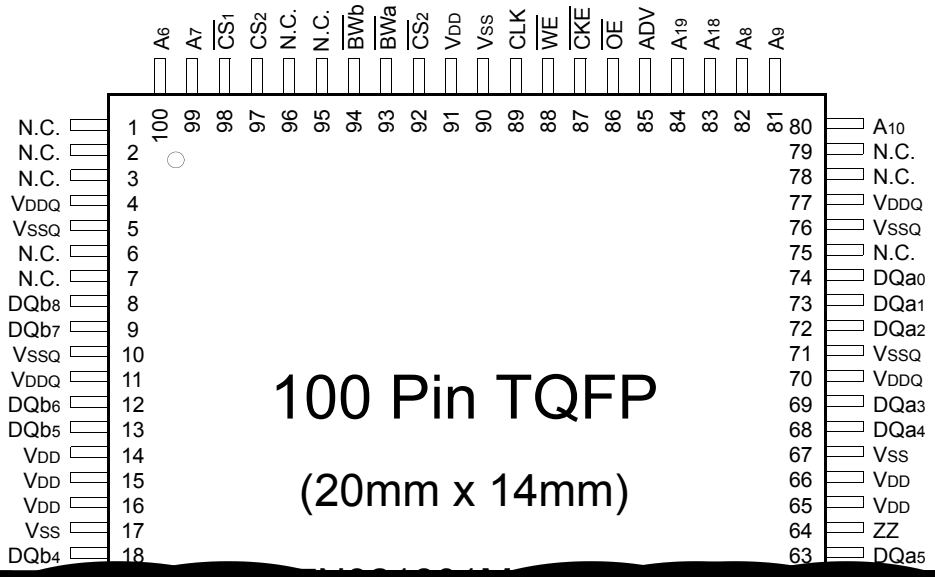
(TOP VIEW)



[redacted]

A0 -	ress Inputs	33,34,35,36,37,43 45,46,47,48,49,50, 81,82,83,84,99,100	VDD VSS	Power Supply(+3. Ground	,15,1 17,4
AD WE CLK CK CS CS CS BW OE ZZ LBO	Contro ep Co	4	N.C. DQa0~a8 DQb0~b8 VDDQ VSSQ	No Connect Data Inputs/Outputs Data Inputs/Outputs Output Power Supply (3.3V or 2.5V) Output Ground	1

[redacted]

SB) of the address field and set the internal burst counter if burst is d

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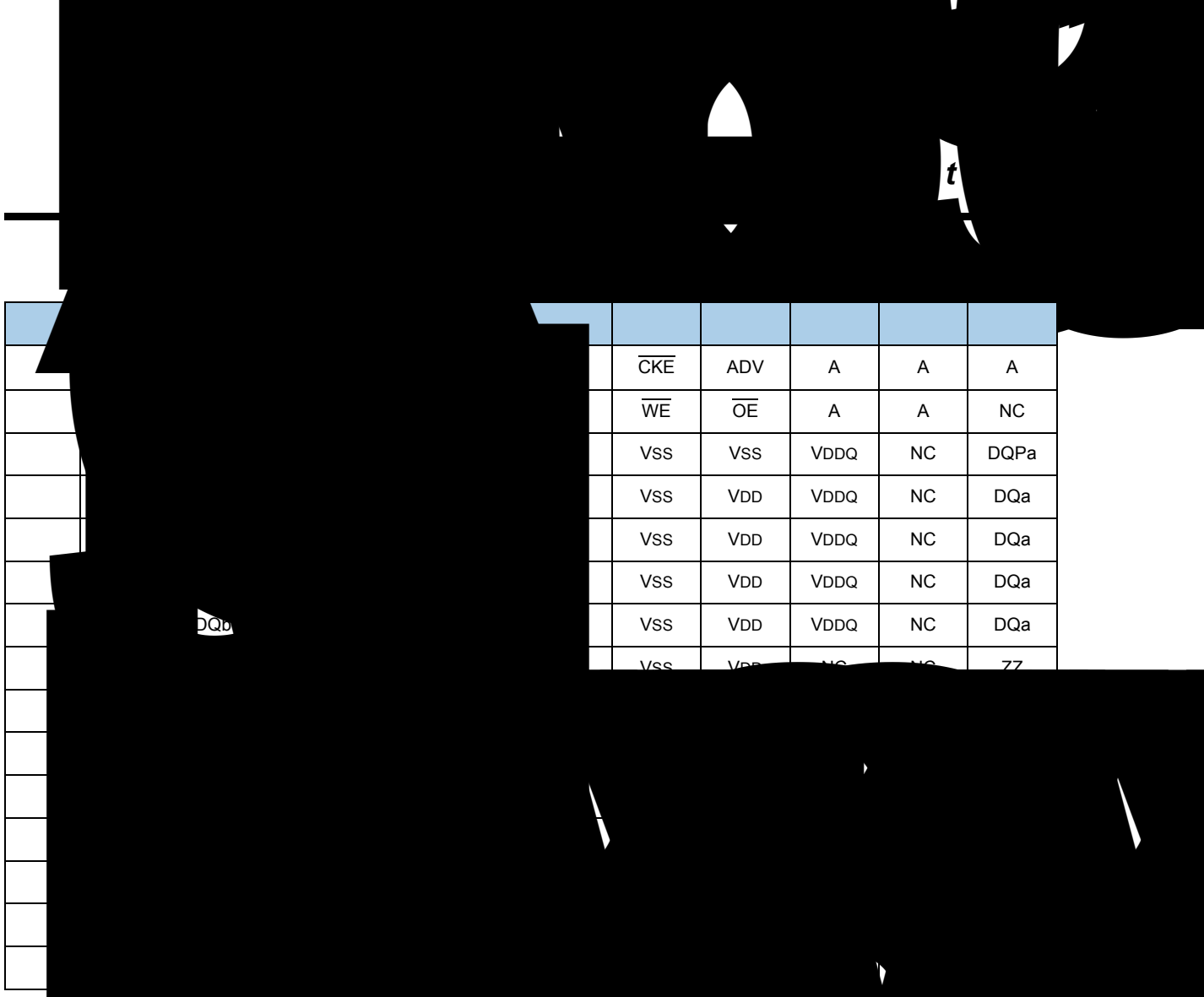
	$\overline{CKE}$	ADV	A	A	NC
	$\overline{WE}$	$\overline{OE}$	A	A	NC
	VSS	VSS	VDDQ	NC	DQPb
	VSS	VDD	VDDQ	DQb	DQb
	VSS	VDD	VDDQ	DQb	DQb
	VSS	VDD	VDDQ	DQb	DQb
	VSS	VDD	VDDQ	DQb	DQb
	VSS	VDD	NC	NC	ZZ

A	Address Inputs	VDD	Power Supply
		VSS	Ground
A_0,A_1	Burst Address Inputs		
$\overline{ADV}$	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
$\overline{CLK}$	Clock	DQa	Data Inputs/Outputs
$\overline{CKE}$	Clock Enable	DQb	Data Inputs/Outpu
$\overline{CS_1}$	Chip Select	DQc	Data Inputs/Outp
$\overline{CS_2}$	Chip Select	DQd	Data Inputs/Ou
$\overline{CS_2}$	Chip Select	DQPa~Pd	Data Inputs/O
$\overline{BW}$x	Byte Write Inputs		
(x=a,b,c,d)		VDDQ	Output Powe
$\overline{OE}$	Output Enable		
$\overline{ZZ}$	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		



	$\overline{CKE}$	ADV	A	A	A
	$\overline{WE}$	$\overline{OE}$	A	A	NC
	VSS	VSS	VDDQ	NC	DQPa
	VSS	VDD	VDDQ	NC	DQa
	VSS	VDD	VDDQ	NC	DQa
	VSS	VDD	VDDQ	NC	DQa
DQb	VSS	VDD	VDDQ	NC	DQa
	VSS				ZZ

A	Address Inputs	V_{DD}	Power Supply
		V_{SS}	Ground
A_0,A_1	Burst Address Inputs		
ADV	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
CLK	Clock		
$\overline{CKE}$	Clock Enable	DQa	Data Inputs/Outpu
$\overline{CS_1}$	Chip Select	DQb	Data Inputs/Outp
$\overline{CS_2}$	Chip Select	DQPa, Pb	Data Inputs/Ou
$\overline{CS_2}$	Chip Select		
$\overline{BW}$x (x=a,b)	Byte Write Inputs	V_{DDQ}	Output Powe
$\overline{OE}$	Output Enable		
$\overline{ZZ}$	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

[redacted]

The K7N323601M and K7N321801M are N*t*RAM[TM] designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.
All inputs (with the exception of OE, LBO and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable(CKE) pin allows the operation of the chip to be suspended as long as necessary. When CKE is high, all synchronous inputs are ignored and the internal [redacted] values.

N*t*RAM[TM] [redacted] ip enables(CS1, CS2, CS2) are activ[redacted]
Output E[redacted]

Read op[redacted] s inputs are latched in the address[redacted] nput signals WE are driven high, an[redacted] ge of the clock and the data is latche[redacted] g read operation OE must be drive[redacted]

Write op[redacted] byte write [redacted]
lined N*t*[redacted]
At the fi[redacted] address i[redacted]
later.

Subsequ[redacted] t of the [redacted]
provided[redacted] n.
The burs[redacted] selected.
And whe[redacted]

During [redacted] Mode[redacted]
this tim[redacted] fter 2 [redacted]
time.

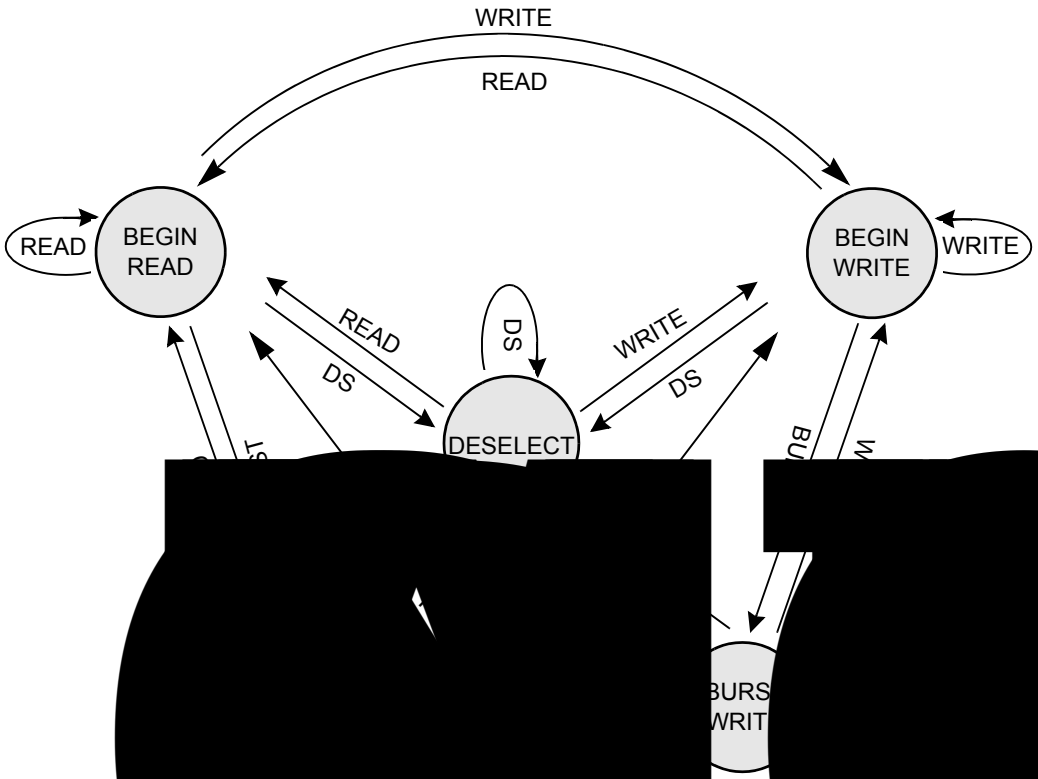
[redacted]

[redacted]								
[redacted]				1	0	[redacted]		
				1	1			
				0	0			
				0	1			

[redacted]

[redacted]										
First Address ↓ Fourth Address	0	0	0	1	1	[redacted]				
	0	1	1	0	1					
	1	0	1	1	0					
	1	1	0	0	0					

: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



	DESELECT
	BEGIN READ
	BEGIN WRITE
	BEGIN READ BEGIN WRITE CONTINUE DESELECT

own is the above diagram. This is because CKE HIGH only blo

not change the state of the device.

2. States change on the rising edge of the clock(CLK)

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H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X		X	L	X		X	L	↑	N/A	Not Selected
X			L	X		X	L	↑	N/A	Not Selected
X			H	X		X	L	↑	N/A	Not Selected Continue
L									al Address	Begin Burst Read Cycle
X									Address	Continue Burst Read Cycle
L									al Address	NOP/Dummy Read
X										
L										
X										
L									N/A	
X										
X										

3.
4.

		X	R
		H	WRIT
		L	WRIT
		L	WRITE
		H	WRITE A

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

Sleep Mode
Read
Write
Deselected

Volta
Volta
Powe
Stora
Oper
Stora

and functio
implied. E

Supply Voltage
Ground

Supp					
Gr					

Inpu			V_{IN}=0V	-	
Outp			V_{OUT}=0V	-	7

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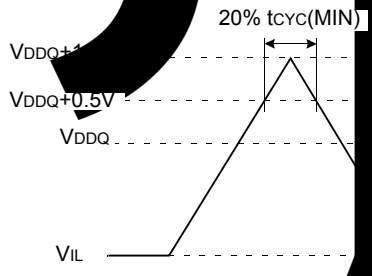
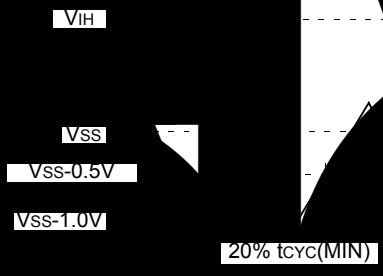
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	μA	
Output Leakage Current	I_{OL}	Output Disabled, V_{out}=V_{SS} to V_{DDQ}		-2	+2	μA	
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, ZZ≤V_{IL} , Cycle Time ≥ t_{CYC} Min	-25	-	460	mA	1,2
			-20	-	410		
			-16	-	360		
			-13	-	310		
Standby Cu		ce deselected, I_{OUT}=0mA, IL, f=Max, All Inputs≤0.2V or 0.2V	-25	-	170		
Standby Cu		ce deselected, I_{OUT}=0mA, 0.2V, All Inputs=fixed (V_{DD}-0.2V or			1		
		ce deselected, I_{OUT}=0mA, 0.2V, f=Max, All Inputs≤V_{IL}					
Outp				-	0.4		
Outp				2.4	-		
Outp							
Outp							
Inpu							
Inpu	V I/			2.0	V_{DD}+0.3**	V	3
Inpu	I/O			-0.3*	0.7		
Inpu							

2. D
3. I





(V_{DD}=3.3V+0.165V/-0.165V,V_{DDQ}=3.3

Input Pulse Level(for 3.3V I/O)	
Input Pulse Level(for 2.5V I/O)	
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	
Input and Output Timing Reference Levels for 3.3V I/O	
Input and Output Timing Reference Levels for 2.5V I/O	V
Output Load	See

Cycle Time	t_{CYC}	4.0	-	5.0	-	6.0	-	7.5	-	ns
Clock Access Time	t_{CD}	-	2.6	-	3.2	-	3.5	-	4.2	ns
Output Enable to Data Valid	t_{OE}	-	2.6	-	3.2	-	3.5	-	4.2	ns
Clock High to Output Low-Z	t_{LZC}	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Hold from Clock High	t_{OH}	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	2.6	-	3.0	-	3.0	-	3.5	ns
Clock High to Output High-Z	t_{HZC}	-	2.6	-	3.0	-	3.0	-	3.5	ns
Clock High Pulse Width	t_{CH}	1.7	-	2.0	-	2.2	-	3.0	-	ns
Clock Low Pulse Width	t_{CL}	1.7	-	2.0	-	2.2	-	3.0	-	ns
Address Setup to Clock High	t_{AS}	1.2	-	1.4	-	1.5	-	1.5	-	
$\overline{CKE}$ Setup to Clock High	t_{CES}	1.2	-	1.4	-	1.5	-	1.5	-	
Data Clock High	t_{DS}	1.2	-	1.4	-	1.5	-	1.5	-	
Writ ock High ($\overline{WE}$, $\overline{BW}$	t_{WS}	1.2	-	1.4	-	1.5	-	1.5	-	
Add etup to Clock H	t_{ADVS}	1.2	-	1.4	-	1.5	-	1.5	-	
Chip k High	t_{CSS}	1.2	-	1.4	-	1.5	-	1.5	-	
Add	t_{AH}	0.3	-	0.4	-	0.5	-	0.5	-	
CKE	t_{CEH}	0.3	-	0.4	-	0.5	-	0.5		
Data Clo	t_{DH}	0.3	-	0.4	-	0.5	-	0		
Writ	t_{WH}	0.3	-	0.4	-	0.5	-			
Add	t_{ADVH}	0.3	-	0.4	-	0.5	-			
Chip ld from Clo	t_{CSH}	0.3	-	0.4	-	0.5	-			
ZZ H wn	t_{PDS}	2	-	2	-	2	-			
ZZ L	t_{PUS}	2	-	2	-	2	-			

setup and hold times for all rising clock(CLK) edges when ADV
low. All other synchronous inputs must meet the specified setup and hold times whenever this device is cl
2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
3. A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low, A Read cycle is d
Both cases must meet setup and hold times.
4. To avoid bus contention, At a given voltage and temperature t_{LZC} is more than t_{HZC}.
The specs as shown do not imply bus contention because t_{LZC} is a Min. parameter that is worst case a
(0°C,3.465V) than t_{HZC}, which is a Max. parameter(worst case at 70°C,3.135V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

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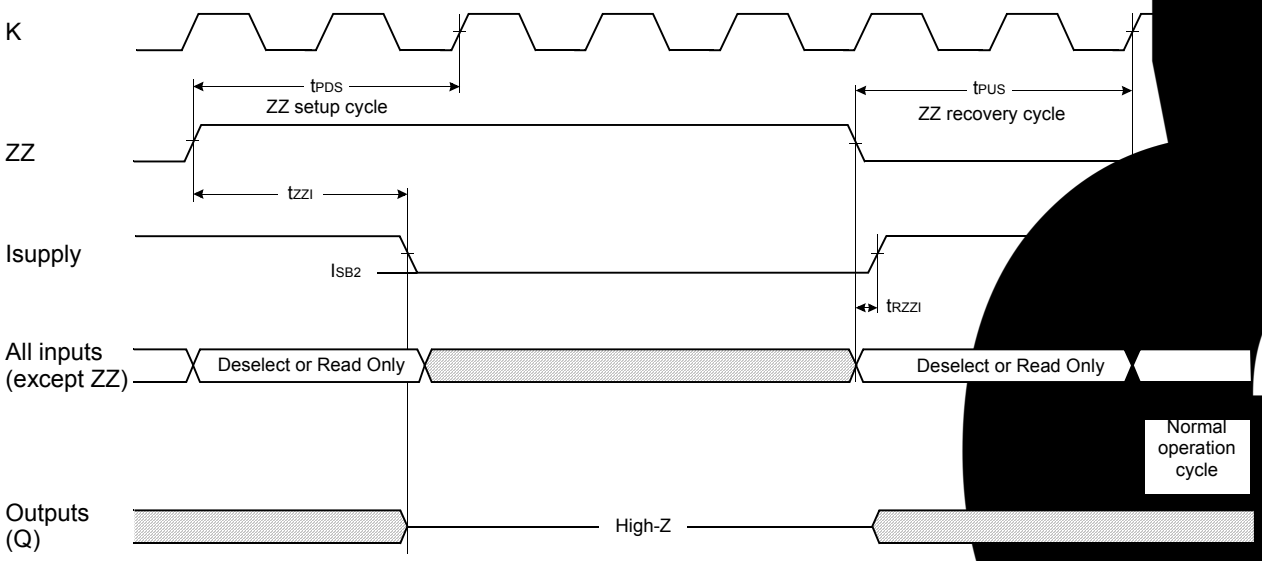
SLEEP MODE is a low curre
SLEEP MODE is dictated by
After entering SLEEP MODE
The ZZ pin is an asynchronou
When the ZZ pin becomes a
MODE is not guaranteed to s
ing operations are completed
while the SRAM is transitioni

Current during SLEEP MODE	ZZ ≥ V_{IH}	I_{SB2}		60	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		



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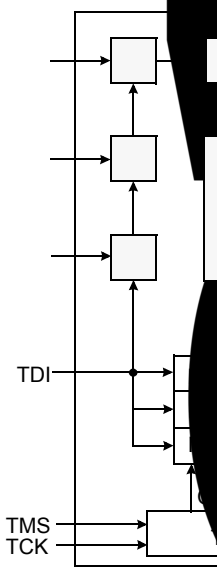
This part contains a
circuitry when in tes
driven out of the SR
ister, Bypass Regist
therefore, TRST signa
interfacing with norma
undriven input will prod
tied to VDD through a resis



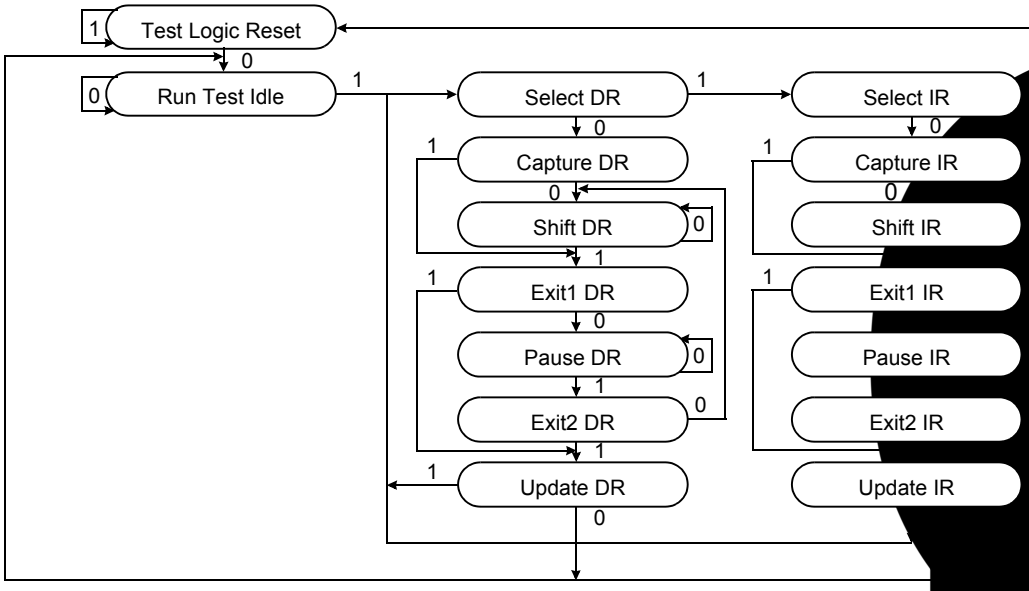
Bo	gister	1
	er	3
	ister	2
By		4
	gister	5
		6
		4
	er	4

o sample all input data regardless of other
s not IEEE 1149.1 compliant.
o sample all input data regardless of other

he first ID register to allow for the serial shift

s when BYPASS instruction is invoked. The
rially loaded TDI when exiting the Shift DR

aces DQs in Hi-Z.
uture use.



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[redacted]

1Mx3					
2Mx1					

1Mx36							
2Mx18							

1	6N	6N
2	8P	8P
3	8R	8R
4	9R	9R
5	9P	9P
6	10P	10P
7	10R	10R
8	11R	11R
9	11P	11P
10	11H	11H
11	11N	11N
12	11M	11M
13	11L	11L
14	11K	11K
15	11J	11J
16	10M	10M
17	10L	10L
18	10K	10K
19	10J	10J
20	11G	11G
21	11F	11F
22	11E	11E
23	11D	11D
24	11C	10G
[redacted]	10F	10F
[redacted]	10E	10E
[redacted]	10D	10D
[redacted]	10G	11C
[redacted]	11A	11A
[redacted]		11B
[redacted]		10A
[redacted]		10B
[redacted]		9A
[redacted]		9B
[redacted]		8A
[redacted]		8B
[redacted]		7A
[redacted]		7B
[redacted]		6B

40	6A	6A
41	5B	5B
42	5A	5A
43	4A	4A
44	4B	4B
45	3B	3B
46	3A	3A
47	2A	2A
48	2B	2B
49	1B	1B
50	1A	1A
51	1C	1C
52	1D	1D
53	1E	1E
54	1F	1F
55	1G	1G
56	2D	2D
57	2E	2E
58	2F	2F
59	2G	2G
60	1J	1J
61	1K	1K
62	1L	1L
63	1M	
64	1N	
65	2K	
66	2L	
67	2M	
68	2J	
69	2R	
70	1R	
71	3P	
72	3R	
73	4R	
74	4P	
75	6P	
76	6R	

[redacted]

: [redacted] der are read as "X" (i.e. don't care).

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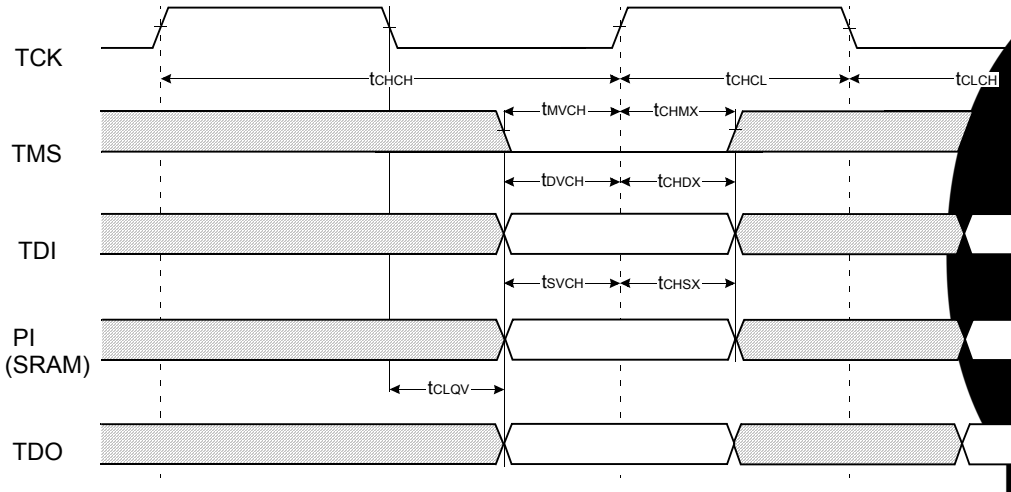
[redacted]

Pow					
Inpu					
Inpu					
Out					
Out					

Input High/Low Level(2				V	
Input Rise/Fall Time(1					
Input and Output Tim					

TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	



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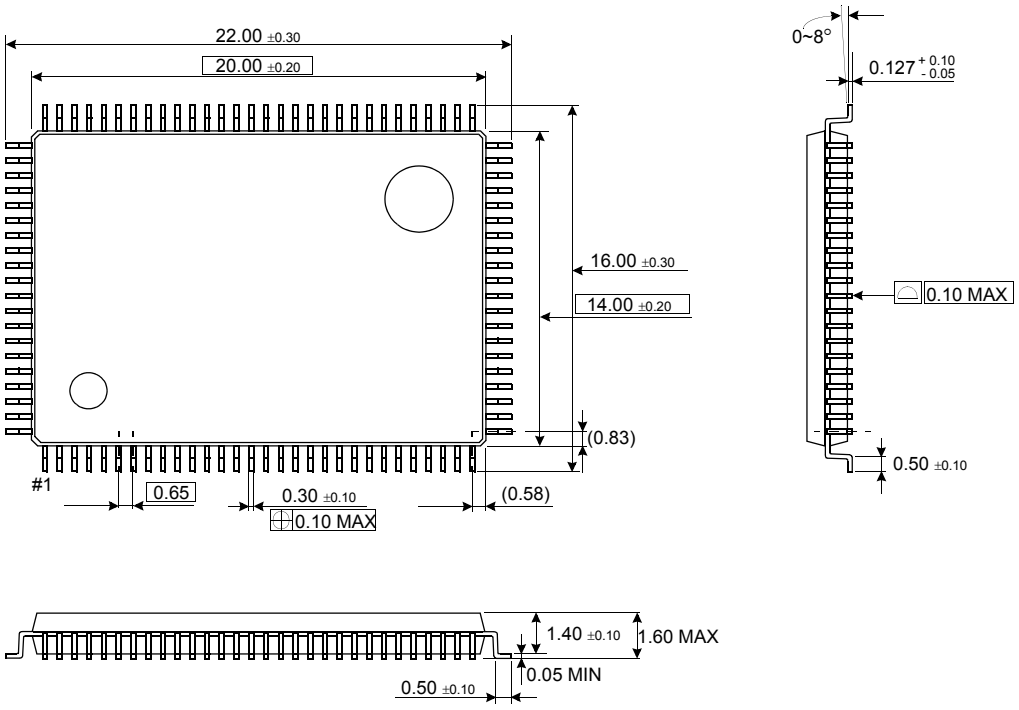
Units ; millimeters/Inches



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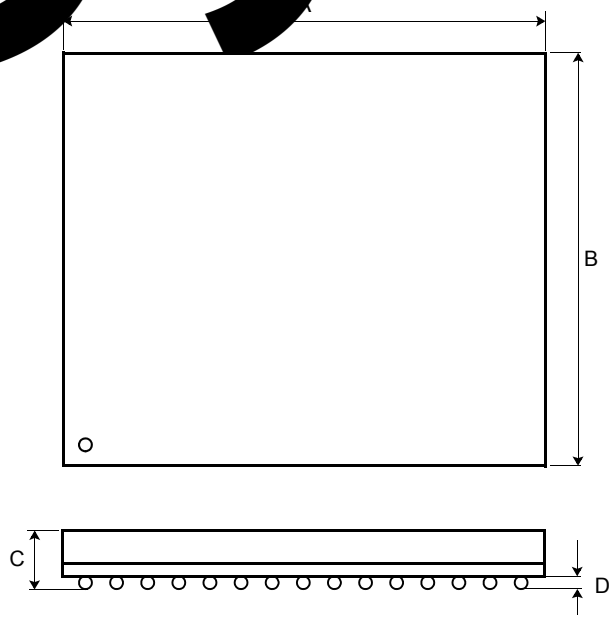

.0

0.05

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