

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

32,768-WORD BY 8-BIT STATIC RAM

DESCRIPTION

The TC55257DPL/DFL/DFTL/DTRL is a 262,144-bit static random access memory (SRAM) organized as 32,768 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5 V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 5 mA/MHz (typ) and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 0.3 μA standby current (typ) when chip enable (CE) is asserted high. There are two control inputs. CE is used to select the device and for data retention control, and output enable (OE) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC55257DPL/DFL/DFTL/DTRL is available in a standard plastic 28-pin dual-in-line package (DIP), plastic 28-pin small-outline package (SOP) and normal and reverse pinout plastic 28-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 27.5 mW/MHz (typical)
- Standby current of 2 μA (maximum) at Ta = 25°C
- Single power supply voltage of 5 V ± 10%
- Power down features using CE.
- Data retention supply voltage of 2 to 5.5 V
- Direct TTL compatibility for all inputs and outputs

● Access Times (maximum):

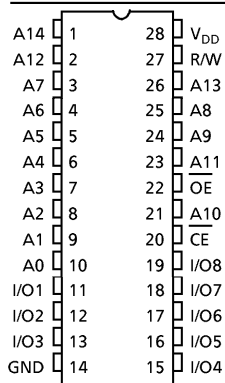
	TC55257DPL/DFL/DFTL/DTRL		
	-55L	-70L	-85L
Access Time	55 ns	70 ns	85 ns
CE Access Time	55 ns	70 ns	85 ns
OE Access Time	30 ns	35 ns	45 ns

Packages:

- DIP28-P-600-2.54 (DPL) (Weight: 4.42 g typ)
- SOP28-P-450-1.27 (DFL) (Weight: 0.79 g typ)
- TSOP I 28-P-0.55 (DFTL) (Weight: 0.22 g typ)
- TSOP I 28-P-0.55A (DTRL) (Weight: 0.22 g typ)

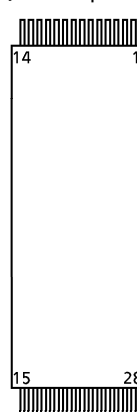
PIN ASSIGNMENT (TOP VIEW)

○ 28 PIN DIP & SOP

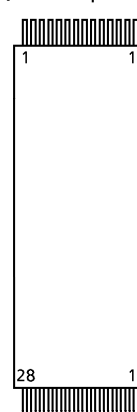


○ 28 PIN TSOP

(Normal pinout)



(Reverse pinout)



PIN NAMES

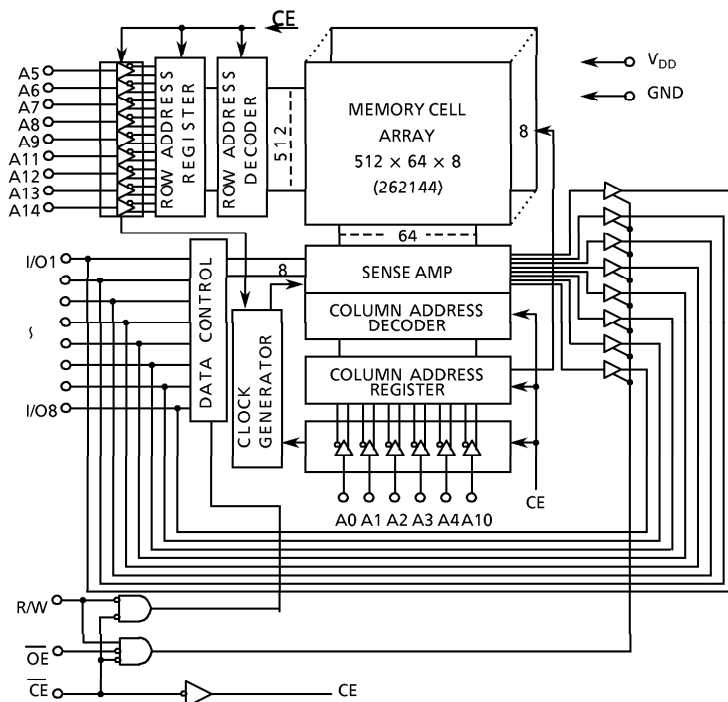
A0 to A14	Address Inputs
R/W	Read/Write Control
OE	Output Enable
CE	Chip Enable
I/O1 to I/O8	Data Input/Output
V _{DD}	Power (+ 5 V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	OE	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE	A ₁₀

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BLOCK DIAGRAM



OPERATION MODE

MODE	\overline{CE}	\overline{OE}	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DDO}
Write	L	x	L	D _{IN}	I _{DDO}
Outputs Disabled	L	H	H	High-Z	I _{DDO}
Standby	H	x	x	High-Z	I _{DDS}

Note: x = don't care. H = logic high. L = logic low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.3 to 7.0	V
V _{IN}	Input Voltage	- 0.3* to 7.0	V
V _{I/O}	Input/Output Voltage	- 0.5* to V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{solder}	Soldering Temperature (10s)	260	°C
T _{strg}	Storage Temperature	- 55 to 150	°C
T _{opr}	Operating Temperature	0 to 70	°C

* - 3.0 V when measured at a pulse width of 50 ns
 ** SOP

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.3	
V _{IL}	Input Low Voltage	- 0.3*	-	0.8	
V _{DH}	Data Retention Supply Voltage	2.0	-	5.5	

* - 3.0 V when measured at a pulse width of 50 ns

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}	-	-	± 1.0	μA	
I _{OH}	Output High Current	V _{OH} = 2.4 V	- 1.0	-	-	mA	
I _{OL}	Output Low Current	V _{OL} = 0.4 V	4.0	-	-	mA	
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$ V _{OUT} = 0 V to V _{DD}	-	-	± 1.0	μA	
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ R/W = V _{IH} , I _{OUT} = 0 mA Other Inputs = V _{IH} /V _{IL}	t _{cycle} = 1 μs	-	10	-	mA
			t _{cycle} = min	-	-	70	
I _{DDO2}	Operating Current	$\overline{CE} = 0.2$ V R/W = V _{DD} - 0.2 V, I _{OUT} = 0 mA Other Inputs = V _{DD} - 0.2 V/0.2 V	t _{cycle} = 1 μs	-	5	-	mA
			t _{cycle} = min	-	-	60	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		-	-	3	mA
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2$ V V _{DD} = 2.0 to 5.5 V	Ta = 0° to 70°C	-	-	20	μA
		Ta = 25°C	-	0.3	2		

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = 0° to 70°C, V_{DD} = 5 V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL/DTRL						UNIT
		-55L		-70L		-85L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	55	-	70	-	85	-	ns
t _{ACC}	Address Access Time	-	55	-	70	-	85	
t _{CO}	Chip Enable Access Time	-	55	-	70	-	85	
t _{OE}	Output Enable Access Time	-	30	-	35	-	45	
t _{COE}	Chip Enable Low to Output Active	10	-	10	-	10	-	
t _{OEE}	Output Enable Low to Output Active	5	-	5	-	5	-	
t _{OD}	Chip Enable High to Output High-Z	-	20	-	25	-	30	
t _{ODO}	Output Enable High to Output High-Z	-	20	-	25	-	30	
t _{OH}	Output Data Hold Time	10	-	10	-	10	-	

WRITE CYCLE

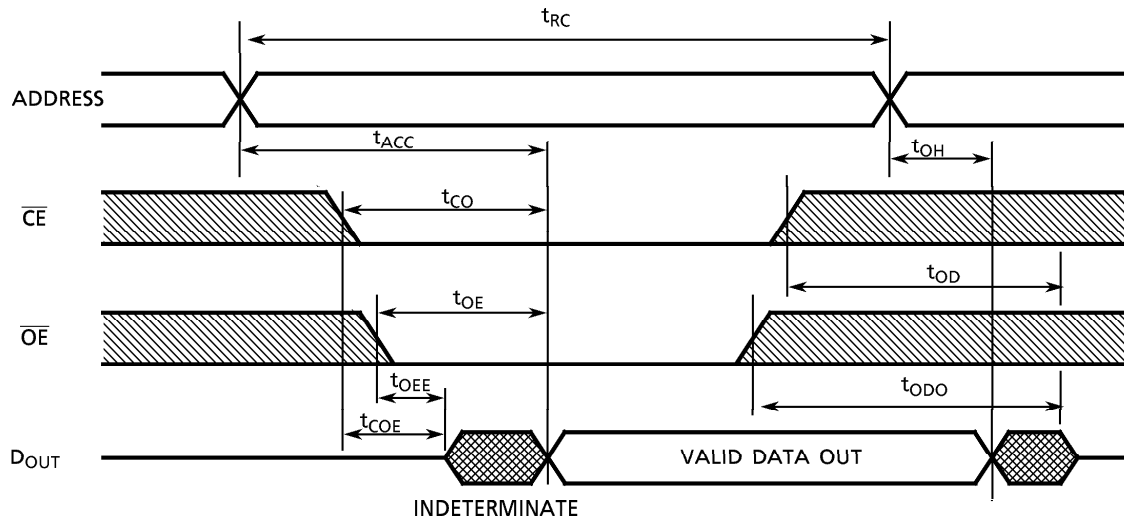
SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL/DTRL						UNIT
		-55L		-70L		-85L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	55	-	70	-	85	-	ns
t _{WP}	Write Pulse Width	45	-	50	-	60	-	
t _{CW}	Chip Enable to End of Write	50	-	60	-	65	-	
t _{AS}	Address Setup Time	0	-	0	-	0	-	
t _{WR}	Write Recovery Time	0	-	0	-	0	-	
t _{ODW}	R/W Low to Output High-Z	-	20	-	25	-	30	
t _{OEW}	R/W High to Output Active	5	-	5	-	5	-	
t _{DS}	Data Setup Time	25	-	30	-	40	-	
t _{DH}	Data Hold Time	0	-	0	-	0	-	

AC TEST CONDITIONS

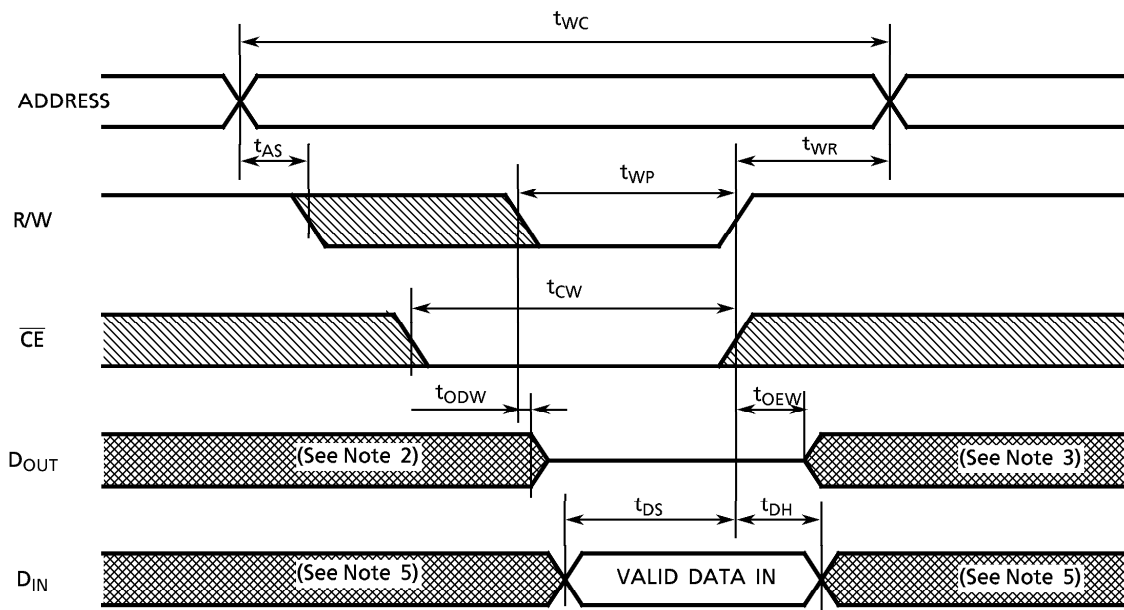
Output load: 30 pF + one TTL gate (-55L)
 100 pF + one TTL gate (-70L, -85L)
 Input pulse level: 0.6 V, 2.4 V
 Timing measurements: 1.5 V
 Reference level: 1.5 V
 t_R, t_F: 5 ns

TIMING DIAGRAMS

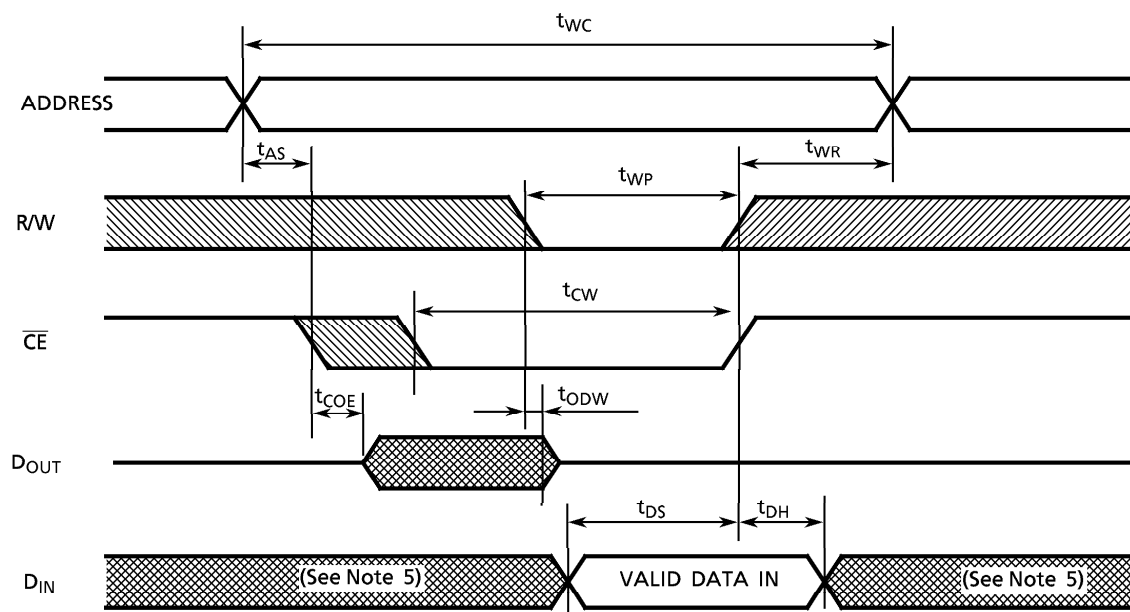
READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 4)



Note: (1) R/W remains HIGH for the read cycle.

- (2) If \overline{CE} goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If \overline{CE} goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

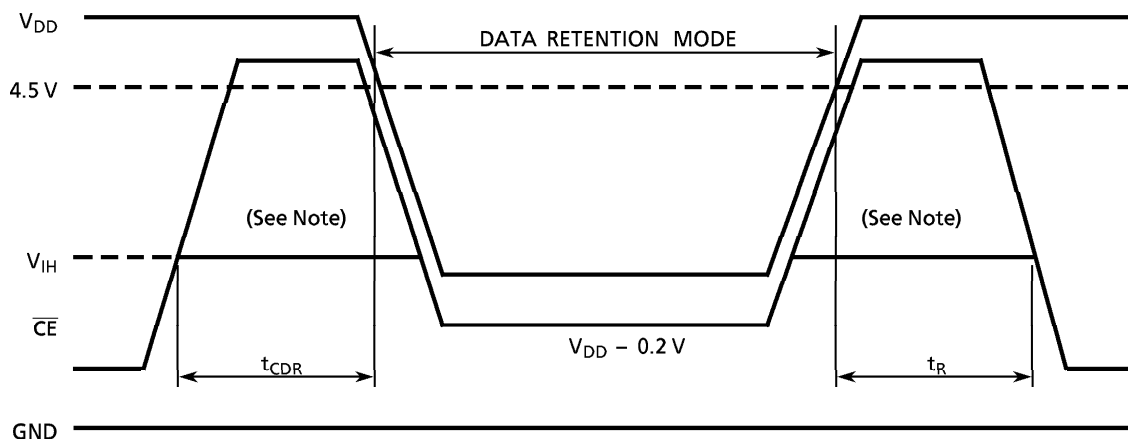
DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage	2.0	-	5.5	V
I _{DDS2}	Standby Current	V _{DH} = 3.0 V	-	10*	μA
		V _{DH} = 5.5 V	-	20	
t _{CDR}	Chip Deselect to Data Retention Mode Time	0	-	-	ns
t _R	Recovery Time	t _{RC} (See Note)	-	-	

* 2 μA (max) at Ta = 0° to 40°C

Note: Read cycle time.

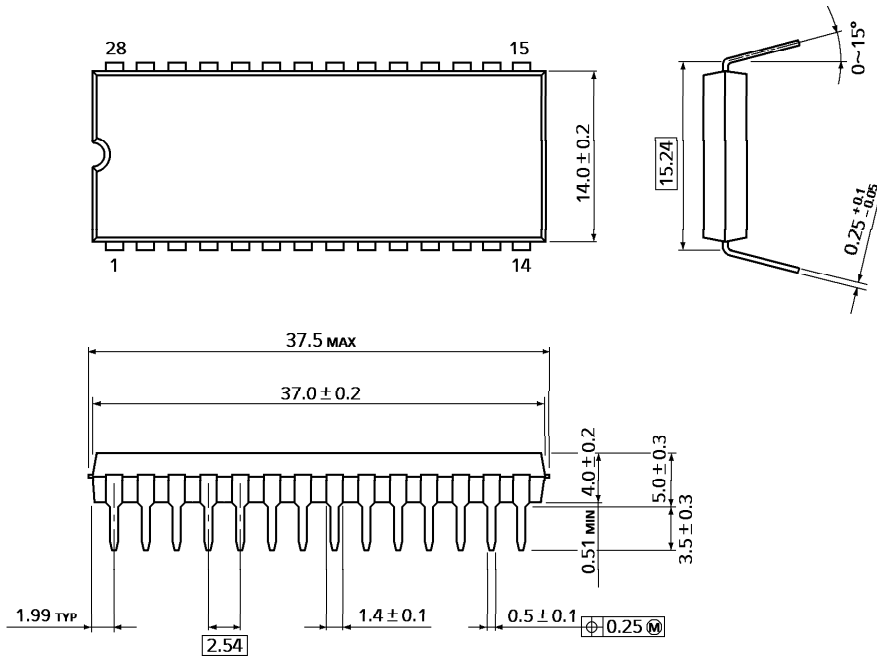
CE CONTROLLED DATA RETENTION MODE



Note: When \overline{CE} is operating at the V_{IH} level (2.2 V), the standby current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.4 V.

PACKAGE DIMENSIONS (DIP28-P-600-2.54)

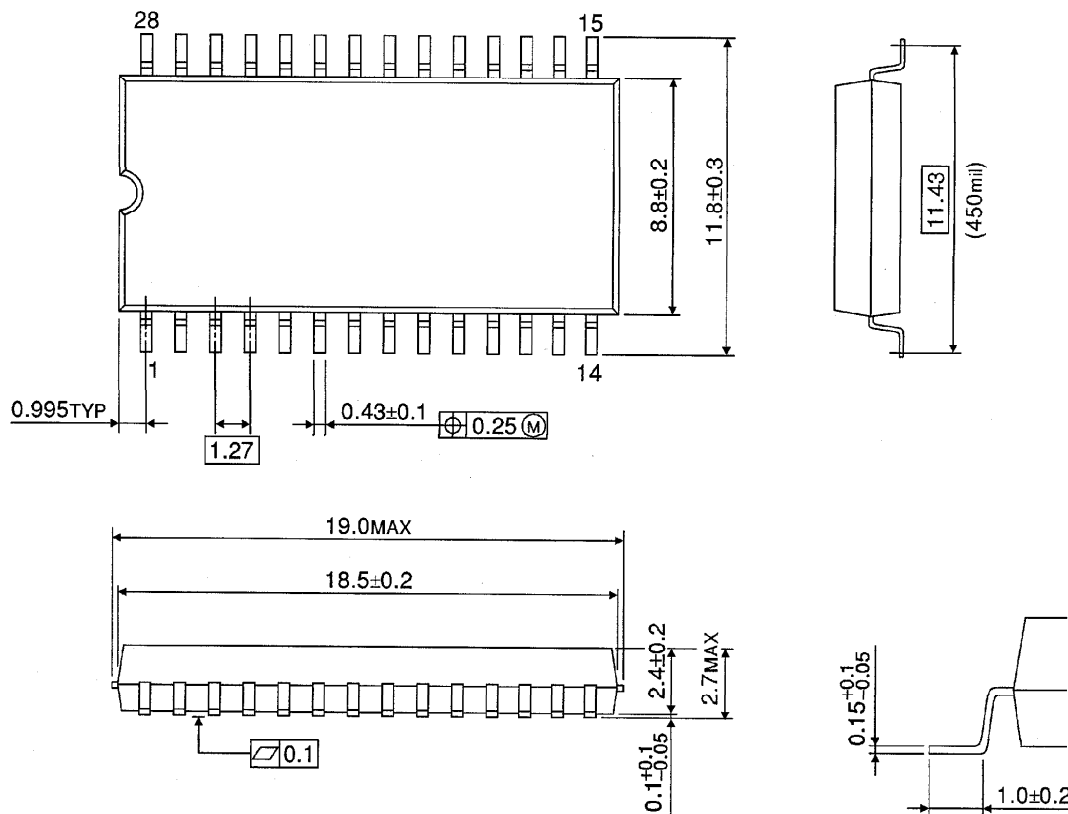
Units in mm



Weight: 4.42 g (typ)

PACKAGE DIMENSIONS (SOP28-P-450-1.27)

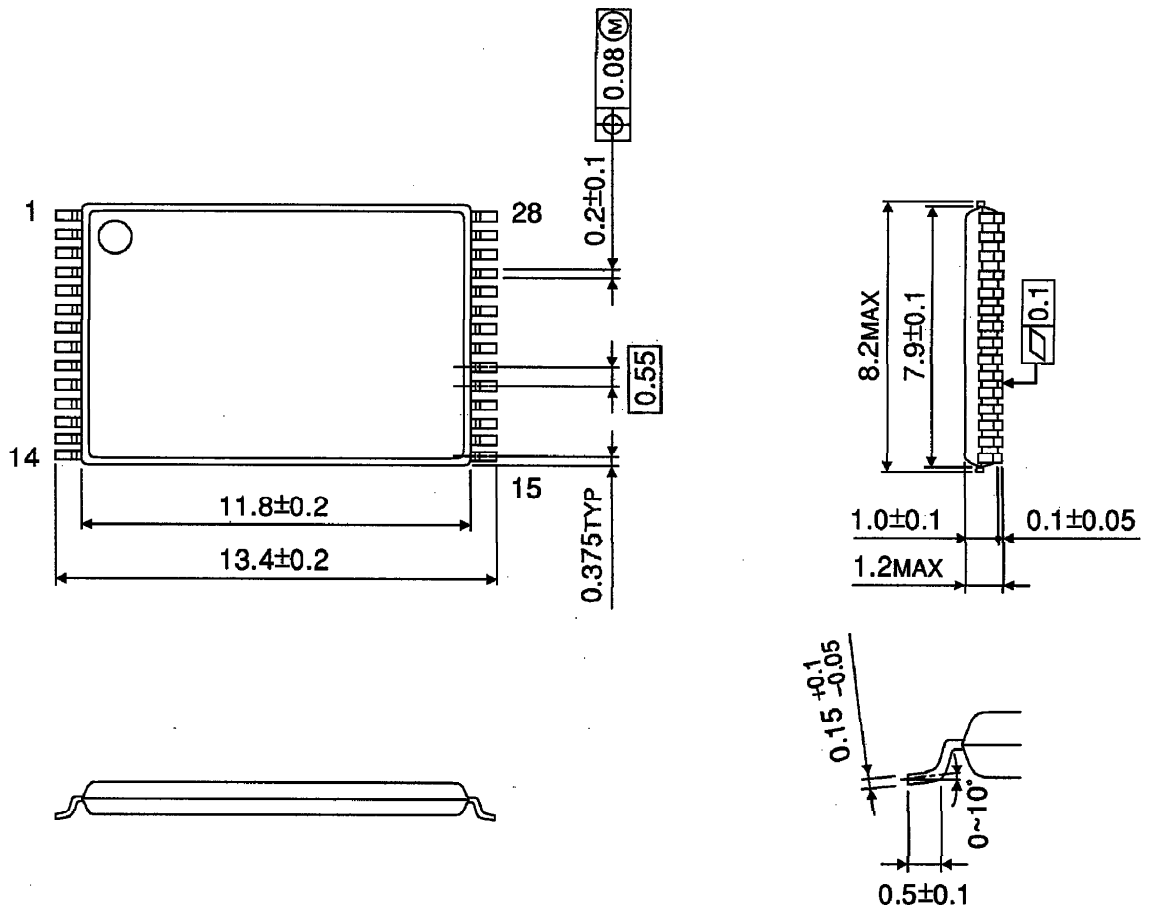
Units in mm



Weight: 0.79 g (typ)

PACKAGE DIMENSIONS (TSOP I 28-P-0.55)

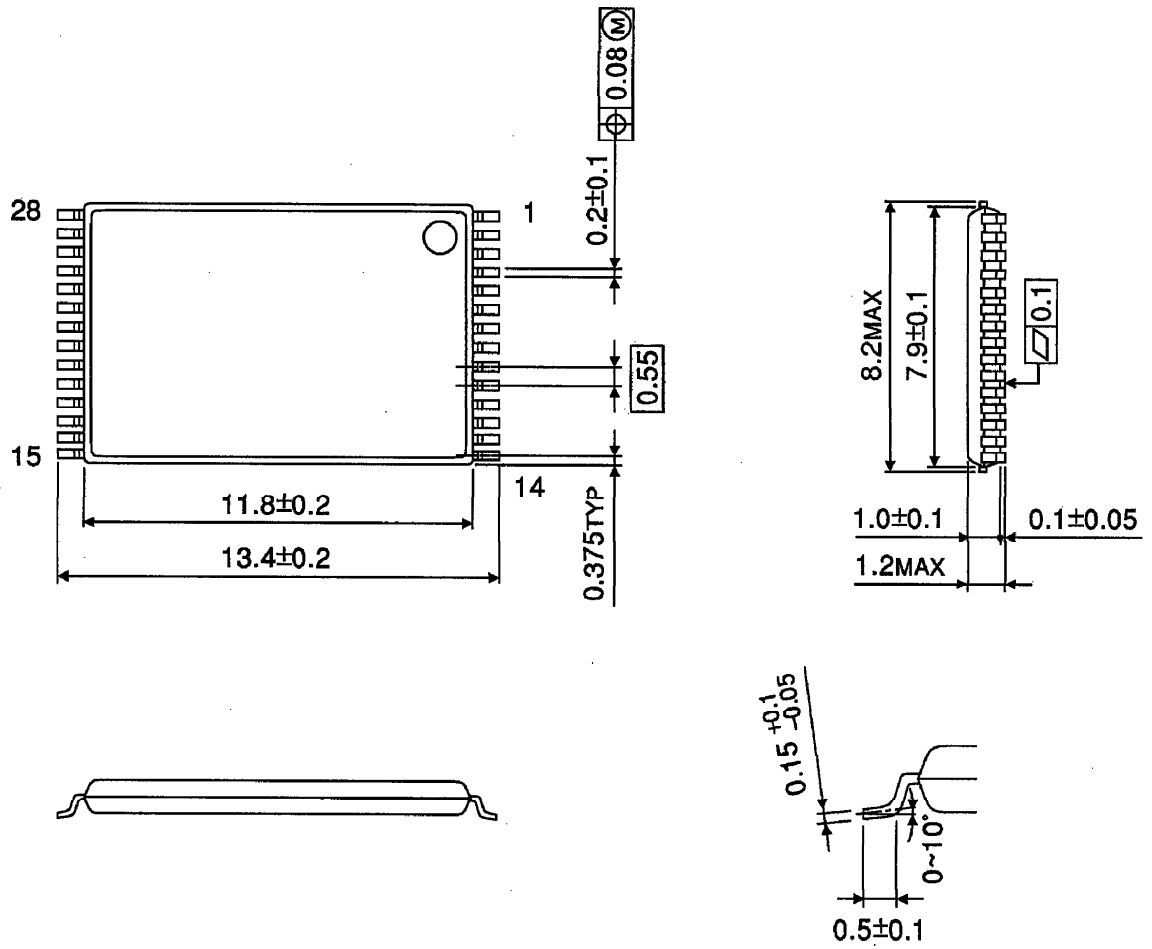
Units in mm



Weight: 0.22 g (typ)

PACKAGE DIMENSIONS (TSOP I 28-P-0.55A)

Units in mm



Weight: 0.22 g (typ)